3 Ha f-Br Ga -Dr IC

FAN7888

SOIC−20, 300 mils
CASE 751BJ−01

Description

The FAN7888 is a monolithic three half−bridge gate−drive IC designed for high−voltage, high−speed driving MOSFETs and IGBTs operating up to +200 V.

’s high−voltage process and common−mode noise canceling technique provide stable operation of high−side drivers under high−dv/dt noise circumstances.

An advanced level−shift circuit allows high−side gate driver operation up to V_S = −9.8 V (typical) for V_{BS} = 15 V.

The UVLS1Ft nt al mf9DÔ RCá9ZS’ bmU0phAwAbphase halfbridge applications in Indoor drive systems.Features Floating Capability for All Channels

MARKING DIAGRAM

$Y = Logo
&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
FAN7888 = Specific Device Code
EBIKE = 3rd Line Marking

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

- 3 Half−Bridge Gate Driver
- Extended Allowable Negative V_S Swing to −9.8 V for Signal Propagation at V_{BS} = 15 V
- Matched Propagation Delay Time Maximum: 50 ns
- 3.3 V and 5 V Input Logic Compatible
- Built−in Shoot−Through Prevention Circuit for All Channels with 270 ns Typical Dead Time
- Built−in Common Mode dv/dt Noise Canceling Circuit
- Built−in UVLO Functions for All Channels
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

- Battery Based Motor Applications (E−bike, Power Tool)
- 3−Phase Motor Inverter Driver

Related Resources

- AN−6076 − Design and Application Guide of Bootstrap Circuit for High−Voltage Gate−Drive IC
- AN−9052 − Design Guide for Selection of Bootstrap Components
- AN−8102 − Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications

© Semiconductor Components Industries, LLC, 2008

INTERNAL BLOCK DIAGRAM

PIN CONFIGURATION

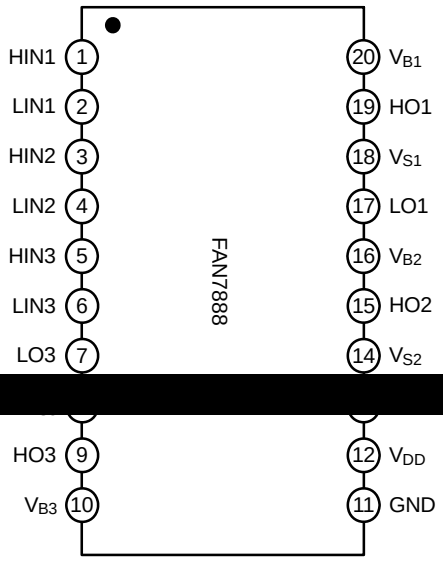


Figure 3. Pin Configuration (Top View)

.00265Tc(High)Tj/TT3 1 Tf2.046270 TD0 Tc<00ef>Tj/TT4 1 Tf.581450 TD-.00265Tc(side driver 3 gloating supply ooltag

PIN DEFINITIONS

Pin No.	Name	Description
1	HIN1	Logic input 1 for high−side gate 1 driver
2	LIN1	Logic input 1 for low−side gate 1 driver
3	HIN2	Logic input 2 for high−side gate 2 driver
4	LIN2	Logic input 2 for low−side gate 2 driver
5	HIN3	Logic input 3 for high−side gate 3 driver
6	LIN3	Logic input 3 for low−side gate 3 driver
7	LO3	Low−side gate driver 3 output
8	V_{S3}	High−side driver 3 floating supply offset voltage
9	HO3	High−side driver 3 gate driver output
10	V_{B3}	
71		Low−side gate driver 31output

Unit
V
V
V
V
V

V Tw[Side Output599.1

TYPICAL CHARACTERISTICS

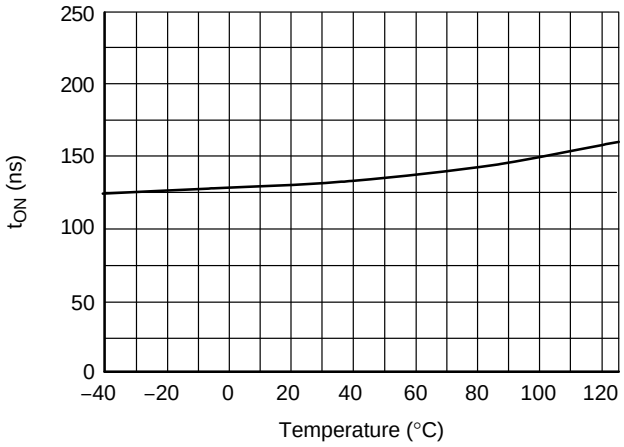


Figure 4. Turn−on Propagation Delay vs. Temperature

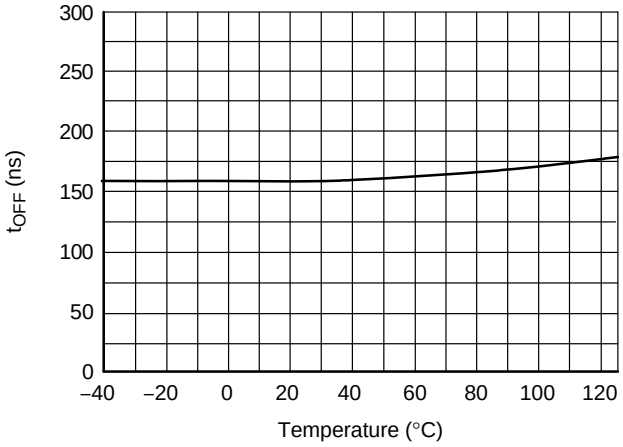


Figure 5. Turn−off Propagation Delay vs. Temperature

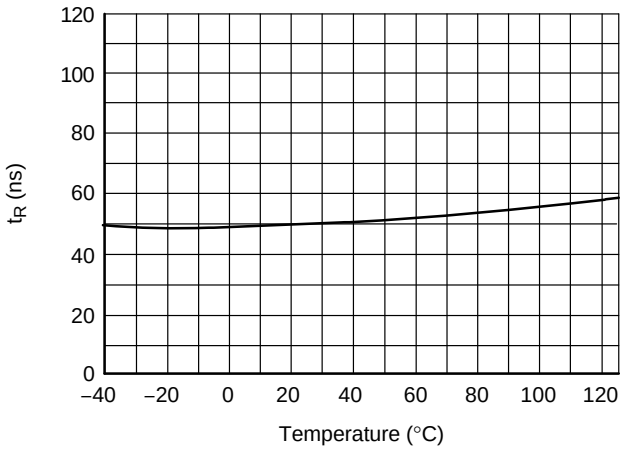


Figure 6. Turn−on Rise Time vs. Temperature

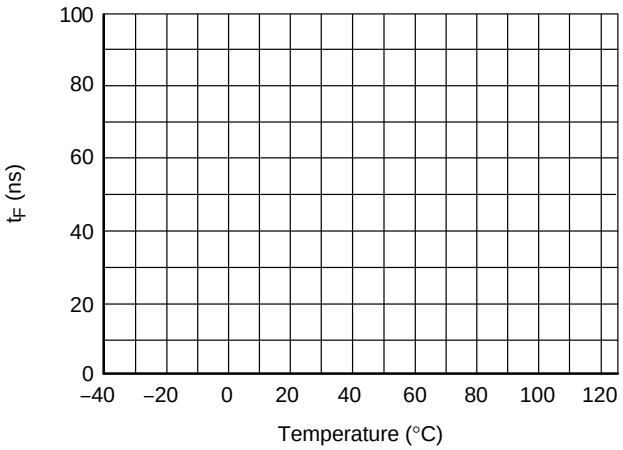


Figure 7. Turn−off Fall Time vs. Temperature

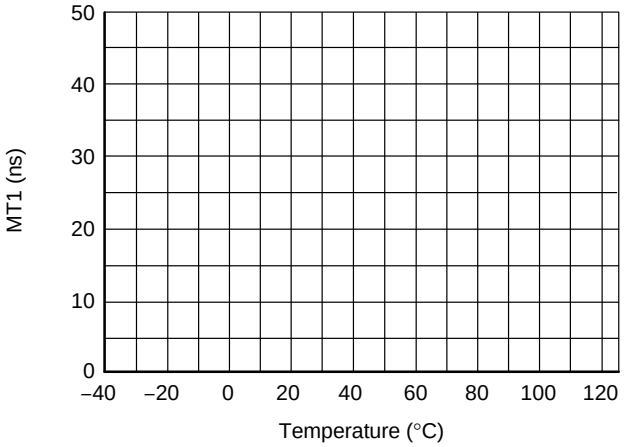


Figure 8. Turn−on Delay Matching vs. Temperature

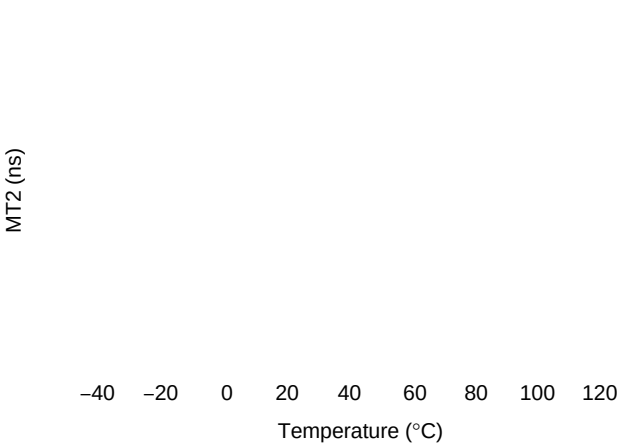


Figure 9. Turn−off Delay Matching vs. Temperature

TYPICAL CHARACTERISTICS (continued)

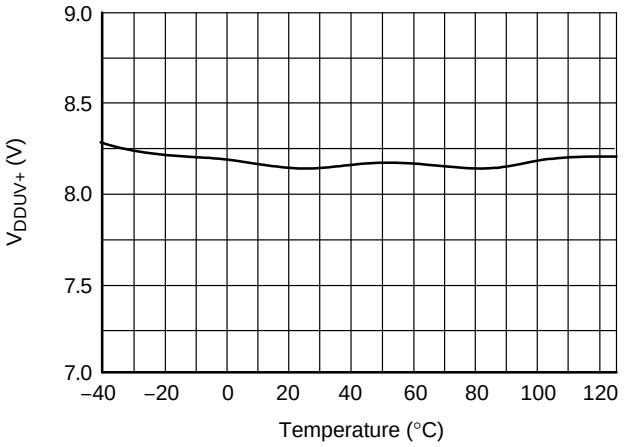


Figure 16. V_{DD} UVLO+ vs. Temperature

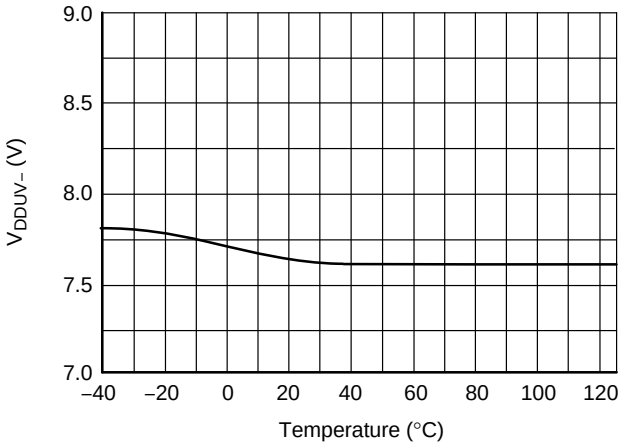


Figure 17. V_{DD} UVLO− vs. Temperature

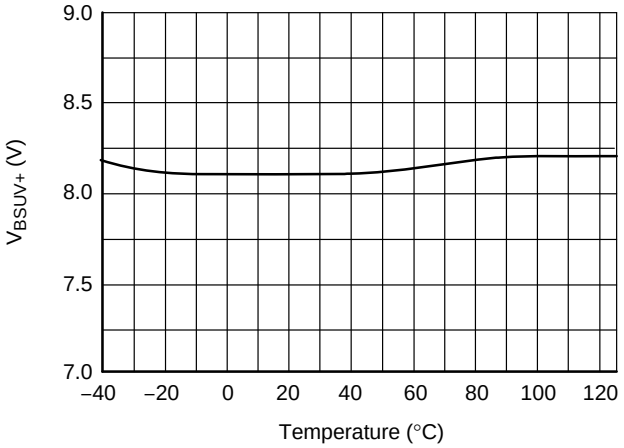


Figure 18. V_{BS} UVLO+ vs. Temperature

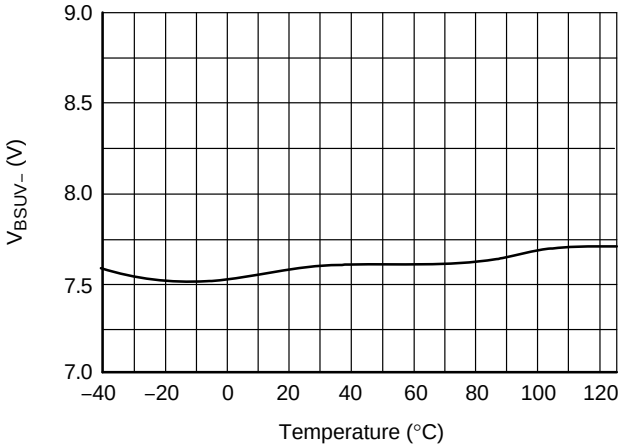


Figure 19. V_{BS} UVLO− vs. Temperature

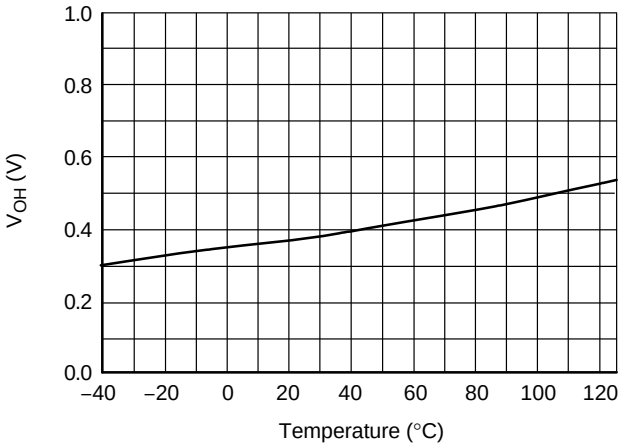


Figure 20. High−Level Output Voltage vs. Temperature

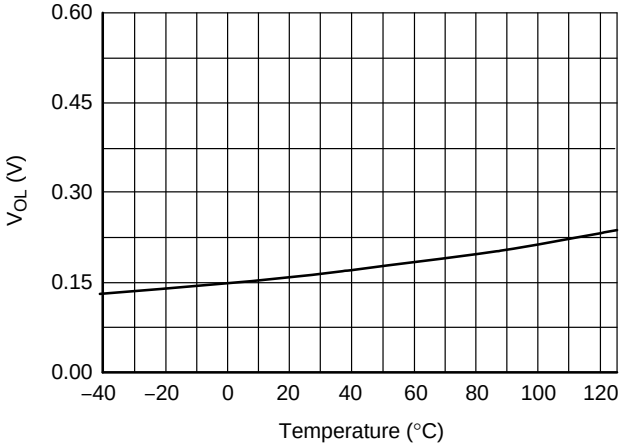


Figure 21. Low−Level Output Voltage vs. Temperature

TYPICAL CHARACTERISTICS (continued)

V_{IH}

Figure 22. Logic High Input Voltage vs. Temperature

Figure 23. Logic Low Input Voltage vs. Temperature

Figure 24. Logic Input High Bias Current vs. Temperature

Figure 25. Allowable Negative V_S Voltage vs. Temperature

Figure 26. Input Pull−down Resistance vs. Temperature

APPLICATION INFORMATION

Protection Function

Under−Voltage Lockout (UVLO)

The high− and low−side drivers include under−voltage lockout (UVLO) protection circuitry for each channel that monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage ($V_{BS1,2,3}$) independently. It can be designed prevent malfunction when V_{DD} and $V_{BS1,2,3}$ are lower than the specified threshold voltage. The UVLO hysteresis prevents chattering during power supply transitions.

Shoot−Through Prevention Function

The FAN7888 has shoot−through prevention circuitry monitoring the high− and low−side control inputs. It can be designed to prevent outputs of high and low side from turning on at same time, as shown Figure 27 and 28.

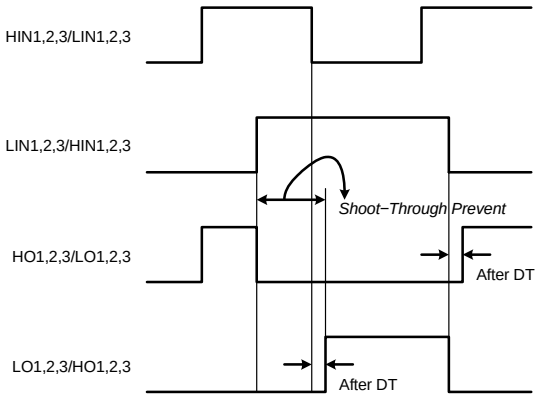


Figure 27. Waveforms for Shoot−Through Prevention

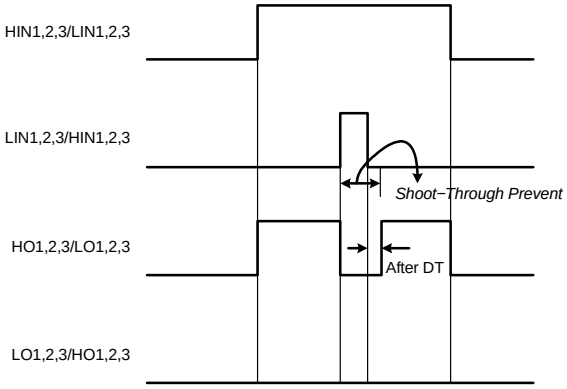


Figure 28. Waveforms for Shoot−Through Prevention

Operational Notes

The FAN7888 is a three half−bridge gate driver with internal, typical 270 ns dead−time for the three−phase brushless DC (BLDC) motor drive system, as shown in Figure 1.

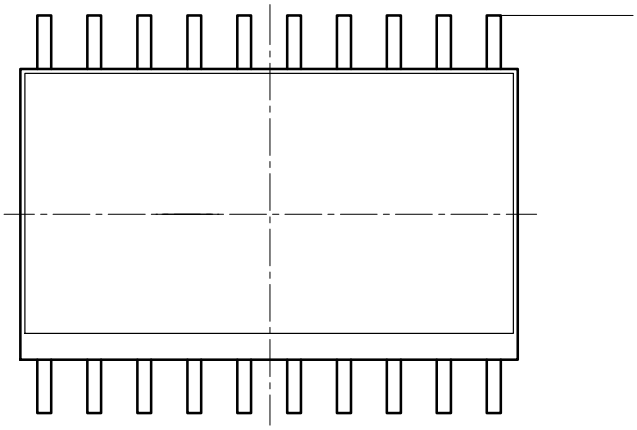
Figure 29 shows a switching sequence of 120° electrical commutation for a three−phase BLDC motor drive system. The waveforms are idealized: they assumed that the generated back EMF waveforms are trapezoidal with flat tops of sufficient width to produce constant torque when the line currents are perfectly rectangular, 120° electrical degrees, with the switching sequence as shown in Figure 29. The operating waveforms of the wye−connection reveal that repeat every 60 electrical degrees, with each 60° segment being “commutated” to another phase, as shown in Figure 29.

330

Figure 29. 120° Commutation Operation Waveforms for 3−Phase BLDC Motor Application

CASE 751BJ
ISSUE O

DATE 19 DEC 2008



onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba “**onsemi**” or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**’s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided “as−is” and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**