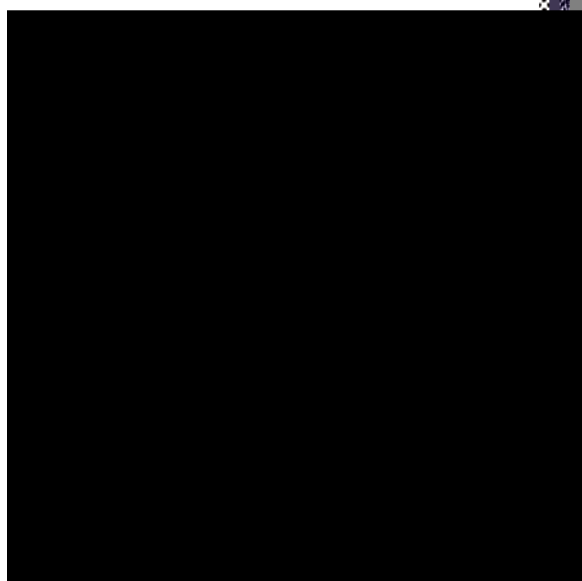




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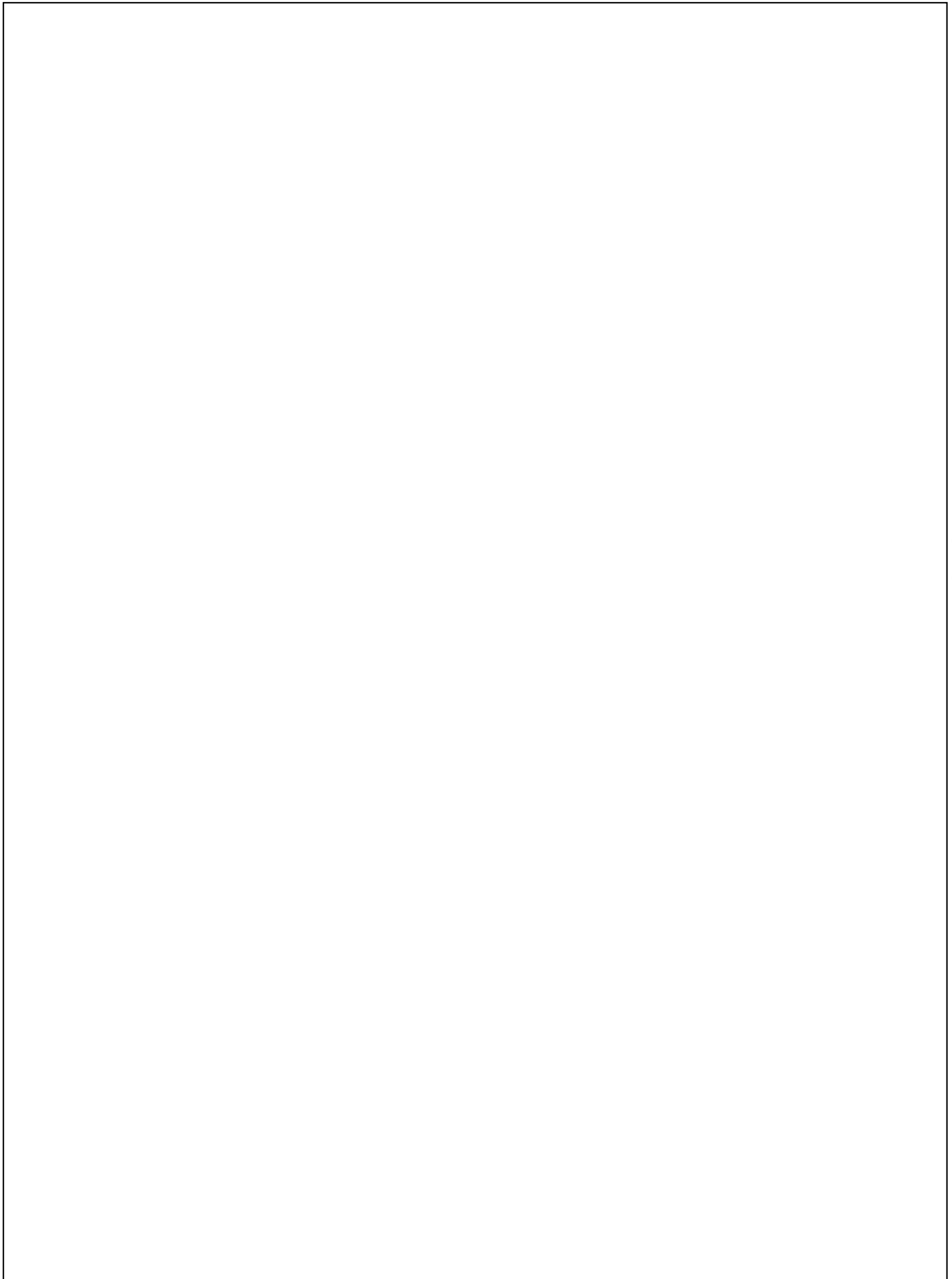
Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the part above the recommended levels is not recommended. In addition, extended exposure to stresses above the recommended conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

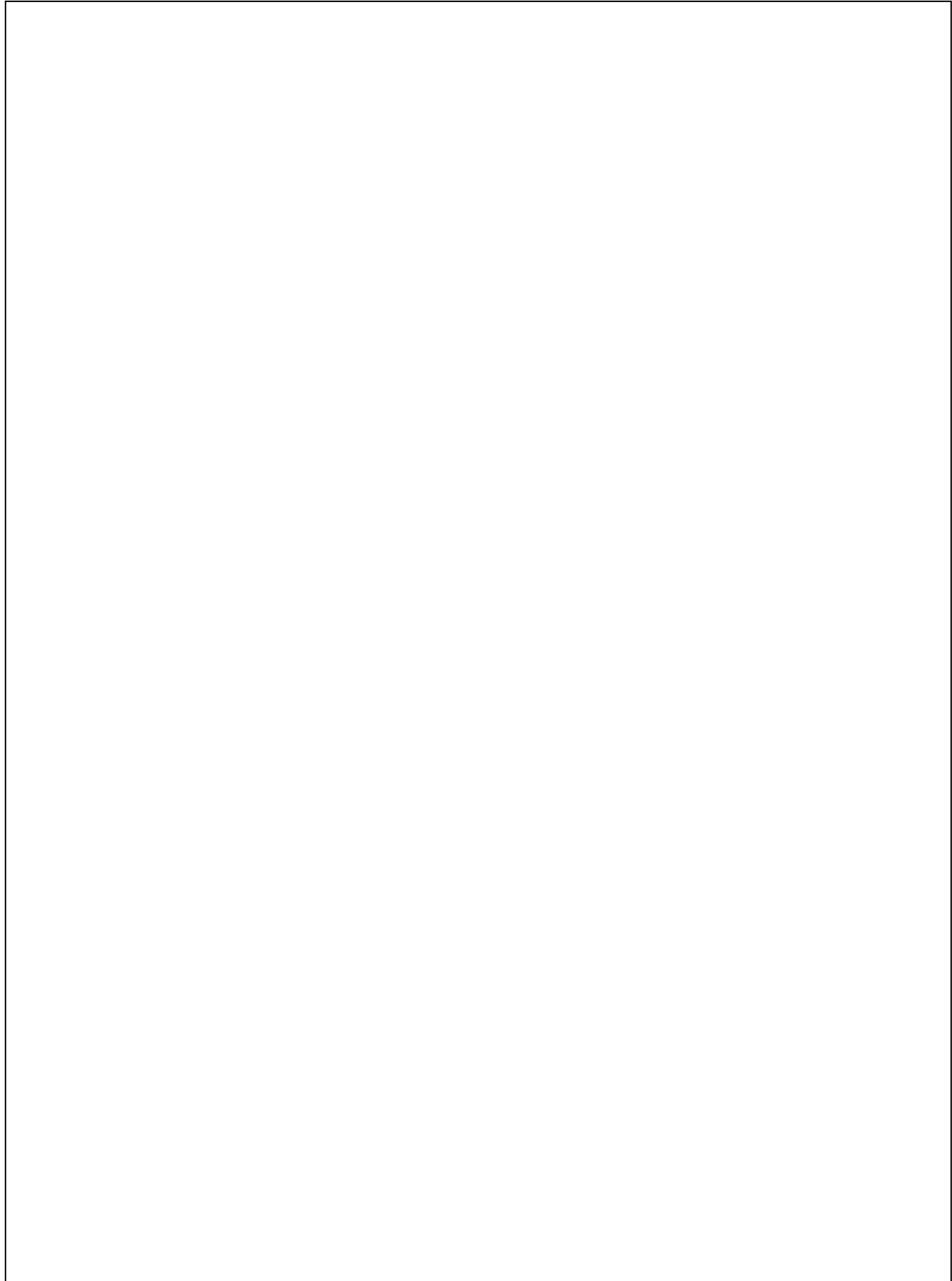
Symbol	Parameter		Max.	Unit
V _{DRV}	DC Link Input Voltage Drain-Source Voltage of each MOSFET		75	V
V _{DD}	DC Supply Voltage for DC-DC Converter		5.5	V
V _{IN,DCDC}	EN, INPUT, FB and COMP to SGND		V _{DD} +0.3	V
V _{IN}	DC Supply Voltage for LDO		75	V
V _{LX}	LX to PGND		36	V
P _D	Power Dissipation ⁽²⁾	1S0P with thermal vias ⁽³⁾	0.98	W
		1S2P with thermal vias ⁽⁴⁾	2.9	
J _A	Thermal Resistance Junction-Air ⁽²⁾	1S0P with thermal vias ⁽³⁾	127	°C/W
		1S2P with thermal vias ⁽⁴⁾	43	
T _A	Operating Ambient Temperature Range		125	°C
T _J	Operating Junction Temperature		150	°C
T _{STG}	Storage Temperature Range		150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	2	KV
		Charged Device Model, JESD22-C101	500	V



Electrical Characteristics

$V_{DD}=3.0\text{ V}$, $V_{IN}=15.0\text{ V}$, $V_{DRV}=60\text{ V}$, $R_T=70\text{ K}$ and $T_A=-40^\circ\text{C}$ to $+125^\circ\text{C}$. Typical values $T_A=25^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Step-Up Switch Section						
$R_{DS(on)}$	N-Channel On Resistance	$V_{DD}=3.3\text{ V}$, $T_A=25^\circ\text{C}$		0.2	0.5	
I_{LK_LX}	LX Leakage Current	$V_{LX}=36\text{ V}$			1.0	μA
Oscillator Section						
f_{OSC}	Operating Frequency	$R_T=58\text{ K}$	40	50	60	KHz
		$R_T=121\text{ K}$	20	25	30	KHz
Logic (EN and INPUT) Section						
V_{INPUT+}	INPUT Logic High Threshold Voltage		1.34			V
V_{INPUT-}	INPUT Logic Low Threshold Voltage				0.5	V
I_{INPUT-}	Input Low Current for INPUT and EN	$V_{EN}=0\text{ V}$			1	μA
I_{INPUT+}	Input High Current for INPUT and EN	$V_{EN}=V_{DD}$	8	12	16	μA
R_{INPUT}	Input Logic Pull-Down Resistance	$V_{EN}=V_{INPUT}=3\text{ V}$		250	375	K
f_{INPUT}	Input Logic Operating Frequency ⁽⁸⁾		20		1000	Hz
Full-Bridge Switch Section						
$R_{DS,ONP}$	Output Upper-Side On Resistance	$T_A=25^\circ\text{C}$		3.0	5.0	
$R_{DS,ONN}$	Output Low-Side On Resistance	$T_A=25^\circ\text{C}$		3.0	5.0	
Output Control Section						
$V_{ADJ,MAX}$	Analog Output Control Maximum Voltage ⁽⁸⁾	$V_{DRV}=100\%$ of Target		1.0		V
$V_{ADJ,MIN}$	Analog Output Control Minimum Voltage ⁽⁸⁾			0.1		V
I_{ADJ+}	Internal Current Source for ADJ Pin	$T_A=25^\circ\text{C}$	9	10	11	μA
Protection (Ready, OVP and TSD)						
V_{READY}	Output Ready Threshold Voltage		0.75	0.80	0.85	V



Typical Performance Characteristics



Figure 12. Maximum On-Time vs. Temperature

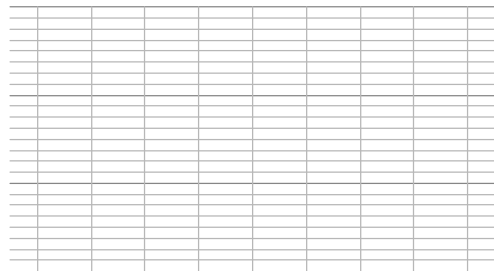


Figure 13. Fist OVP (FB) vs. Temperature

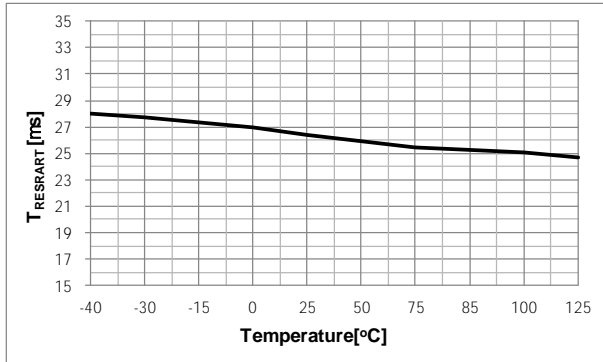


Figure 14. Restart-Time vs. Temperature

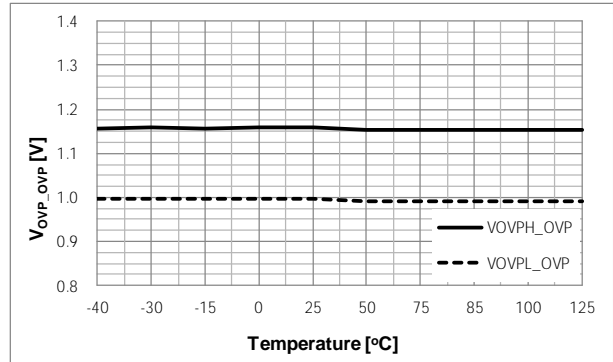


Figure 15.

Typical Performance Characteristics

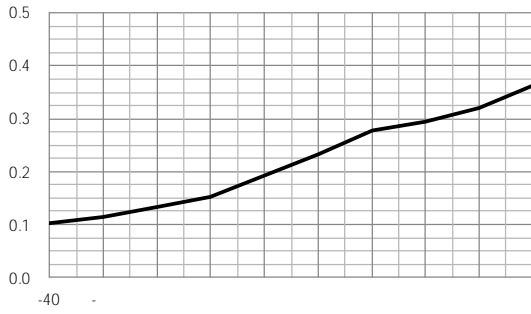


Figure 20. Boost Switch R_{DS(on)} vs. Temperature

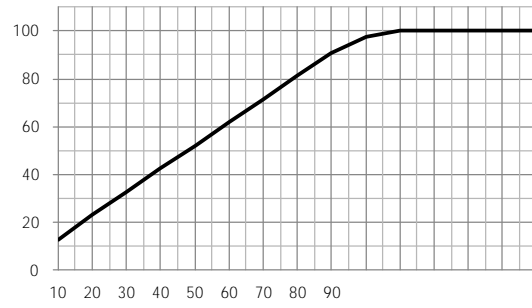


Figure 21. % of Sine Amplitude vs. R_{ADJ}

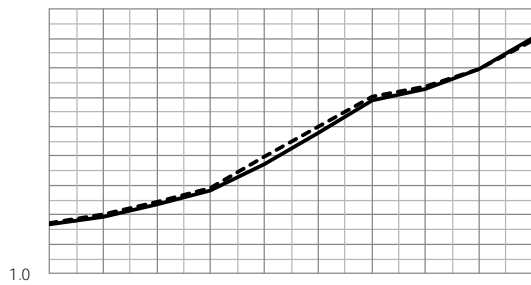


Figure 22. Full-Bridge Switch R_{DS(on)} vs. Temperature

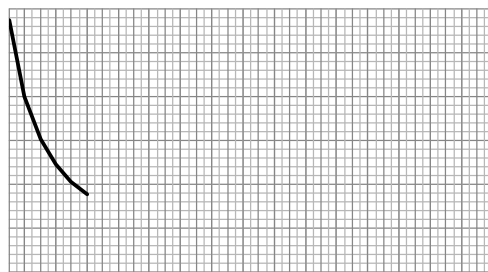


Figure 23. f_{osc} vs. R_T

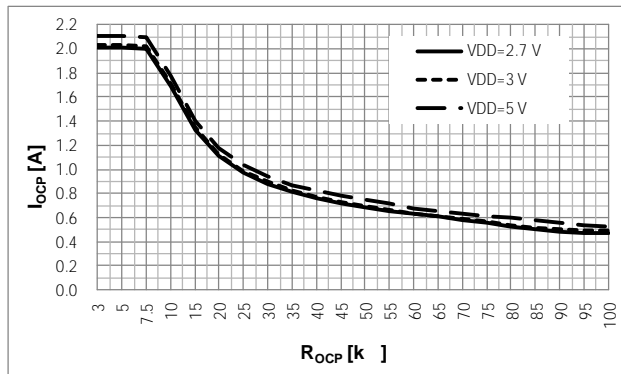
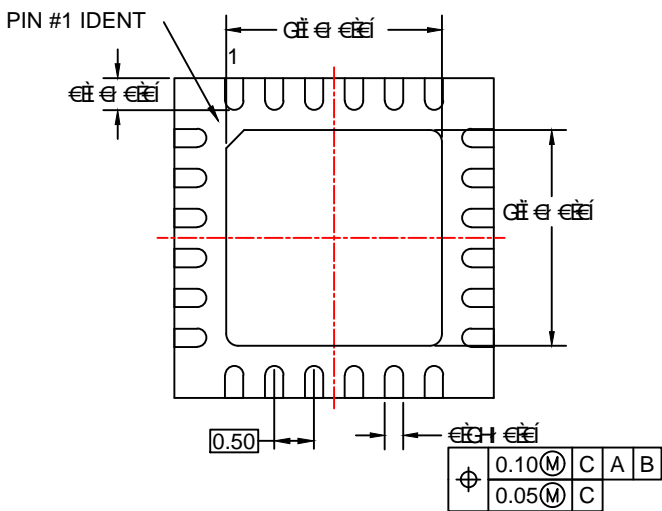
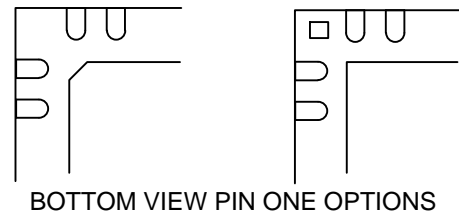
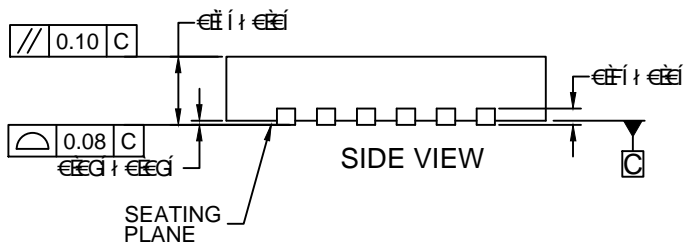
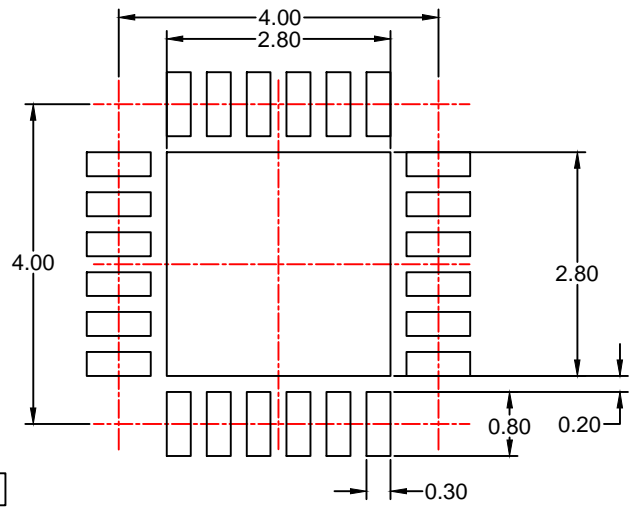
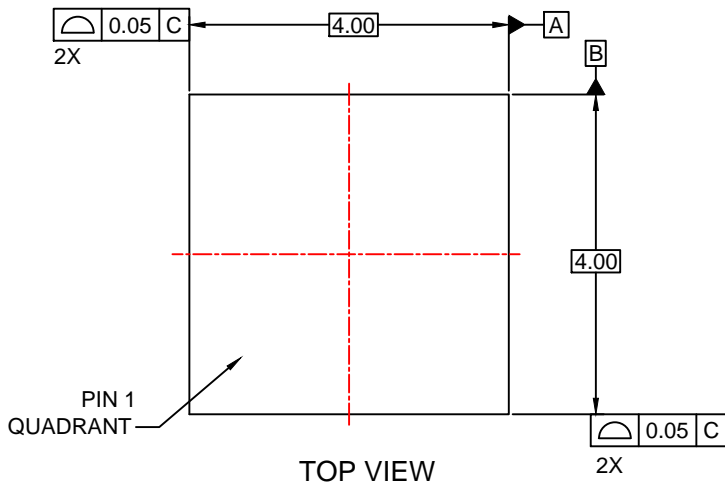


Figure 24. I_{OCP} vs. R_{OCP}



BOTTOM VIEW

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