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FAIRCHILD
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September 8, 2005

FCBS0550

Smart Power Module (SPM)

Features

- UL Certified No.E209204(SPM27-BA package)
- 500V-5A 3-phase MOSFET inverter bridge including control ICs for gate driving and protection
- Divided negative dc-link terminals for inverter current sensing applications
- Single-grounded power supply due to built-in HVIC

Integrated Power Functions

- 500V-5A MOSFET inverter for three-phase DC/AC power conversion (Please refer to Fig. 3)

Integrated Drive, Protection and System Control Functions

- For inverter high-side MOSFETs: Gate drive circuit, High voltage isolated high-speed level shifting
  Control circuit under-voltage (UV) protection
  Note) Available bootstrap circuit example is given in Figs. 10 and 11.
- For inverter low-side MOSFETs: Gate drive circuit, Short circuit protection (SC)
  Control supply circuit under-voltage (UV) protection

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-side Common Bias Voltage for IC and MOSFETs Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-side U Phase
4	$IN_{(VL)}$	Signal Input for Low-side V Phase
5	$IN_{(WL)}$	Signal Input for Low-side W Phase
6	V_{FO}	Fault Output
7	C_{FOD}	Capacitor for Fault Output Duration Time Selection
8	C_{SC}	Capacitor (Low-pass Filter) for Short-Current Detection Input
9	$IN_{(UH)}$	Signal Input for High-side U Phase
10	$V_{CC(UH)}$	High-side Bias Voltage for U Phase IC
11	$V_{B(U)}$	High-side Bias Voltage for U Phase MOSFET Driving
12	$V_{S(U)}$	High-side Bias Voltage Ground for U Phase MOSFET Driving
13	$IN_{(VH)}$	Signal Input for High-side V Phase
14	$V_{CC(VH)}$	High-side Bias Voltage for V Phase IC
15	$V_{B(V)}$	High-side Bias Voltage for V Phase MOSFET Driving
16	V V_2	Phase

Internal Equivalent Circuit and Input/Output Pins

Note:

Absolute Maximum Ratings (T_J = 25°C, Unless Otherwise Specified)

Inverter Part

Symbol	Parameter	Conditions	Rating	Units
V_{PN}	Supply Voltage	Applied between P- N_U, N_V, N_W	400	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P- N_U, N_V, N_W	450	V
V_{DSS}	Drain-Source Voltage		500	V
± I_D	Each MOSFET Drain Current	T_C = 25°C, Peak Sinusoidal Current	5	A
± I_{DP}	Each MOSFET Drain Current (Peak)	T_C = 25°C, Under 1ms Pulse Width	7	A
P_C	Collector Dissipation	T_C = 25°C per One Chip	25	W
T_J	Operating Junction Temperature	(Note 1)	-20 ~ 125	°C

Note:

1. The maximum junction temperature rating of the power chips integrated within the SPM is 150 °C(@$T_C \leq 100$°C). However, to insure safe operation of the SPM, the average junction temperature should be limited to $T_{J(ave)} \leq 125$°C (@$T_C \leq 100$°C)

Control Part

Symbol	Parameter	Conditions	Rating	Units
V_{CC}	Control Supply Voltage	Applied between $V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$, $V_{CC(L)}$ - COM	20	V
V_{BS}	High-side Control Bias Voltage	,=660V88.3(o)0g4.003s25o-22.8421 -29.(3vTcV5004)gs25o-22.8421 -29.(306 TcV)T525o.3uflTcV50		

Total System

Thermal Resistance

Note:

2. For the measurement point of case temperature(T_C), please refer to Figure 2.

Package Marking and Ordering Information

Electrical Characteristics (T_J

Electrical Characteristics (T_J = 25°C, Unless Otherwise Specified)

Control Part

Note:

4. Short-circuit current protection is functioning only at the low-sides.

5. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : $C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}$[F]

Recommended Operating Conditions

Mechanical Characteristics and Ratings

Parameter	Conditions		Limits			Units
			Min.	Typ.	Max.	
Mounting Torque	Mounting Screw: - M3	Recommended 0.62N•m	0.51	0.62	0.72	N•m
Device Flatness		Note Fig. 5	0	-	+120	μm
Weight			-	15.4	-	g

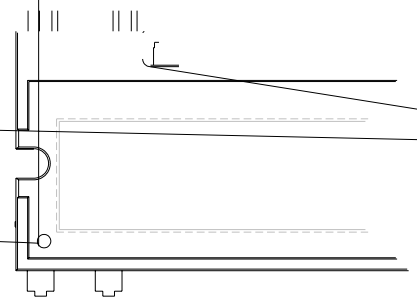


Figure 5. Flatness Measurement Position

Time Charts of SPMs Protective Function

a1 : Control supply voltage rises: After the voltage rises UV_{CCR}, the circuits start to operate when next input is applied.

a2 : Normal operation: MOSFET ON and carrying current.

a3 : Under voltage detection (UV_{CCD}).

a4 : MOSFET OFF in spite of control input condition.

a5 : Fault output operation starts.

a6 : Under voltage reset (UV_{CCR}).

a7 : Normal operation: MOSFET ON and carrying current.

Figure 6. Under-Voltage Protection (Low-side)

b1 : Control supply voltage rises: After the voltage reaches UV_{BSR}, the circuits start to operate when next input is applied.

b2 : Normal operation: MOSFET ON and carrying current.

b3 : Under voltage detection (UV_{BSD}).

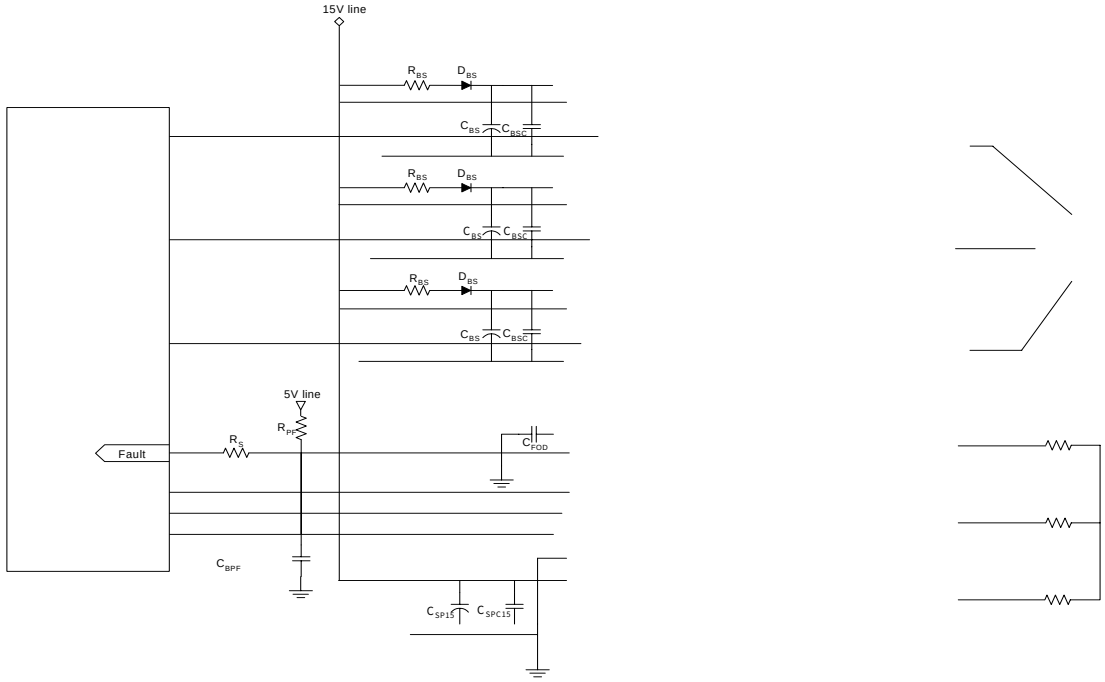
b4 : MOSFET OFF in spite of control input condition, but there is no fault output signal.

b5 : Under voltage reset (UV_{BSR})

b6 : Normal operation: MOSFET ON and carrying current

Figure 7. Under-Voltage Protection (High-side)

Note:



Note:

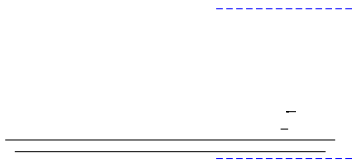
1. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)
2. By virtue of integrating an application specific type HVIC inside the SPM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
3. V_{FO} output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7kΩ resistance. Please refer to Figure 9.
4. C_{SP15} of around 7 times larger than bootstrap capacitor C_{BS} is recommended.
5. V_{FO} output pulse width should be determined by connecting an external capacitor(C_{FOD}) between C_{FOD}(pin7) and COM(pin2). (Example : if C_{FOD} = 33 nF, then t_{FO} = 1.8ms (typ.)) Please refer to the note 5 for calculation method.
6. Input signal is High-Active type. There is a 3.3kΩ resistor inside the IC to pull down each input signal line to GND. When employing RC coupling circuits, set up such RC couple that input signal agree with turn-off/turn-on threshold voltage.
7. To prevent errors of the protection function, the wiring around R_F and C_{SC} should be as short as possible.
8. In the short-circuit protection circuit, please select the R_FC_{SC} time constant in the range 1.5~2 μs.
9. Each capacitor should be mounted as close to the pins of the SPM as possible.
10. To prevent surge destruction, the wiring between the smoothing capacitor and the P&COM pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22μF between the P&COM pins is recommended.
11. Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays.
12. C_{SPC15} should be over 1μF and mounted as close to the pins of the SPM as possible.

Fig. 11. Typical Application Circuit

Detailed Package Outline Drawings

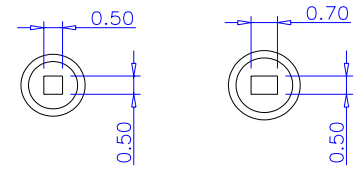
Detailed Package Outline Drawings (Continued)

Detailed Package Outline Drawings (Continued)



LEAD TYPE 1

SCALE 2 : 1



LEAD TYPE 1 LEAD TYPE 2

LEAD SECTION X–X'

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