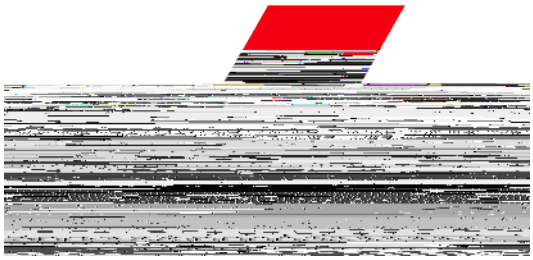

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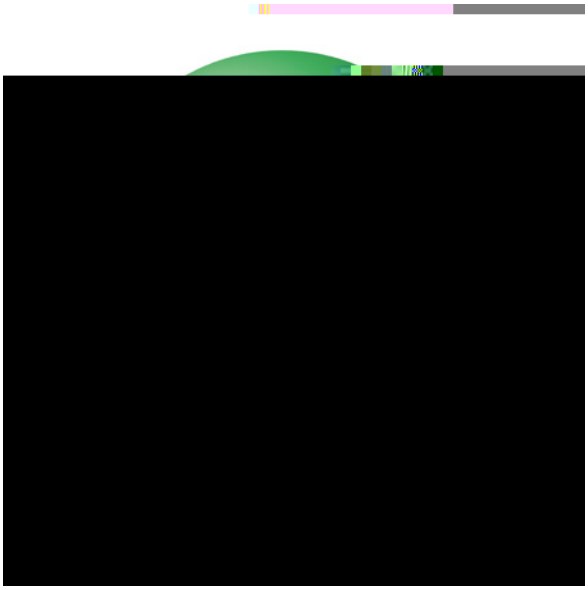

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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

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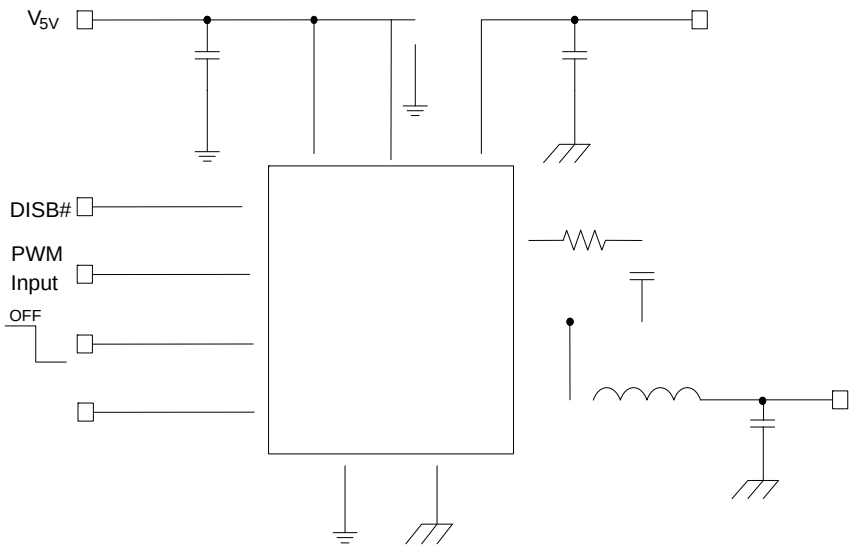
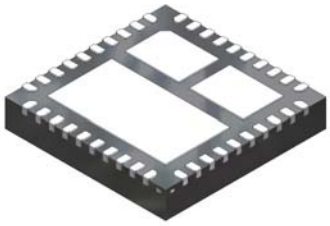
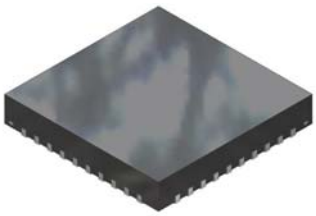
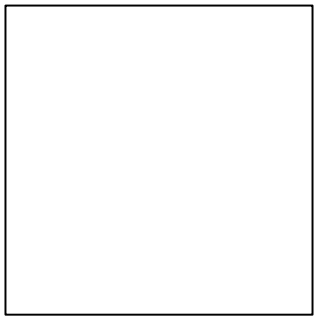
Typical Application Circuit



Pin Configuration







Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended.

Electrical Characteristics

Typical values are V_{IN} = 12 V, V_{CIN} = 5 V, V_{DRV} = 5 V, and $T_A = T_J$ = +25°C unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Thermal Warning Flag						
T_{ACT}	Activation Temperature			150		°C
T_{RST}	Reset Temperature			135		°C
R_{THWN}	Pull-Down Resistance	I_{PLD}=5 mA		30		Ω

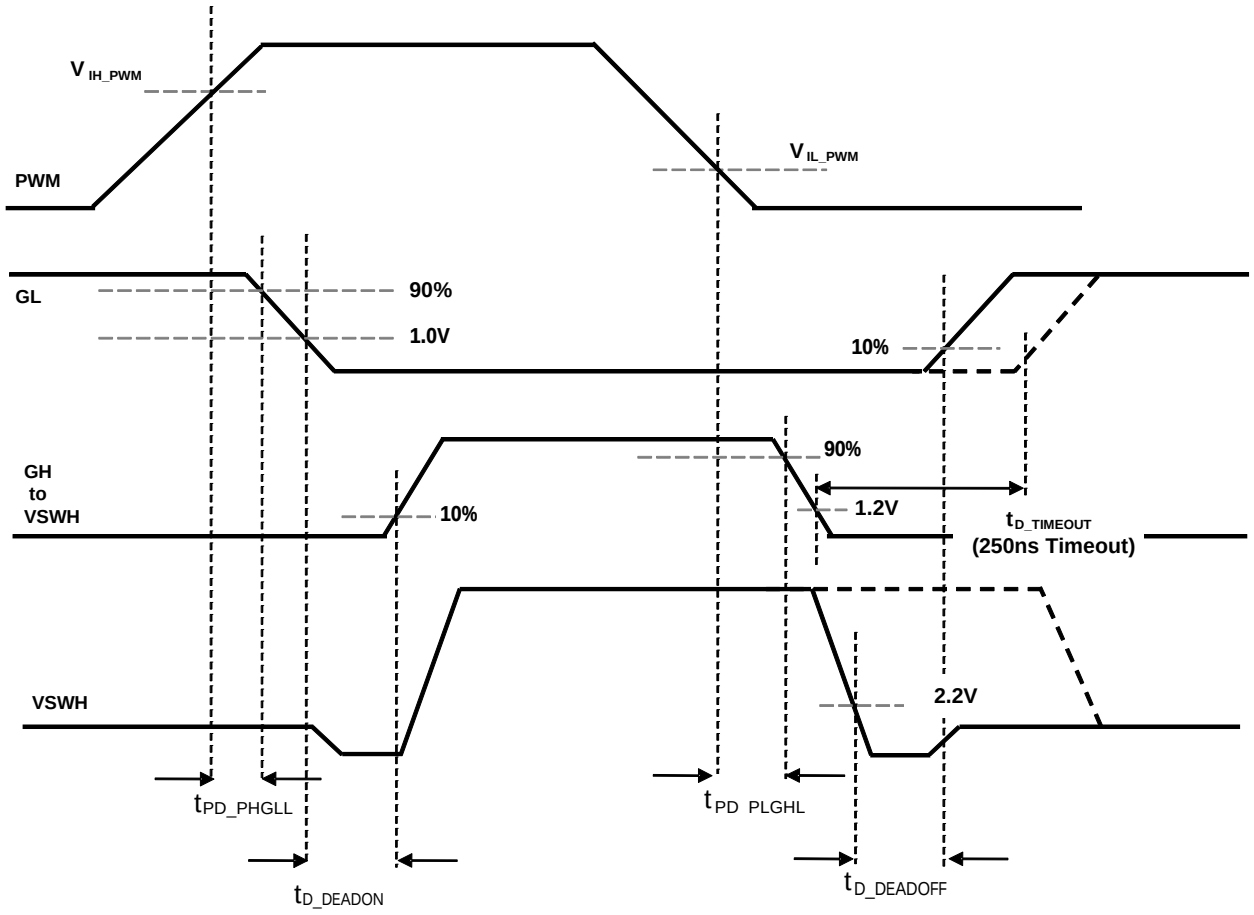


Figure 5. PWM Timing Diagram

Typical Performance Characteristics

Test Conditions: V_{IN}=12 V, V_{OUT}=1 V, V_{CIN}=5 V, V_{DRV}=5 V, L_{OUT}=250 nH, T_A=25°C, and natural convection cooling, unless otherwise specified.

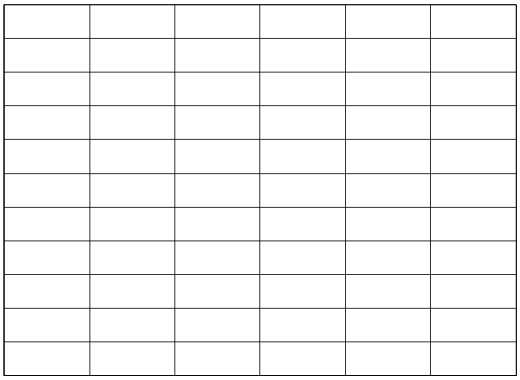


Figure 6. Safe Operating Area

Figure 7. Power Loss vs. Output Current

Figure 8. Power Loss vs. Switching Frequency

Figure 9. Power Loss vs. Input Voltage

Figure 10. Power Loss vs. Driver Supply Voltage

Figure 11. Power Loss vs. Output Voltage

Typical Performance Characteristics

Test Conditions: V_{IN}=12 V, V_{OUT}=1 V, V_{CIN}=5 V, V_{DRV}=5 V, L_{OUT}=250 nH, T_A=25°C, and natural convection cooling, unless otherwise specified.

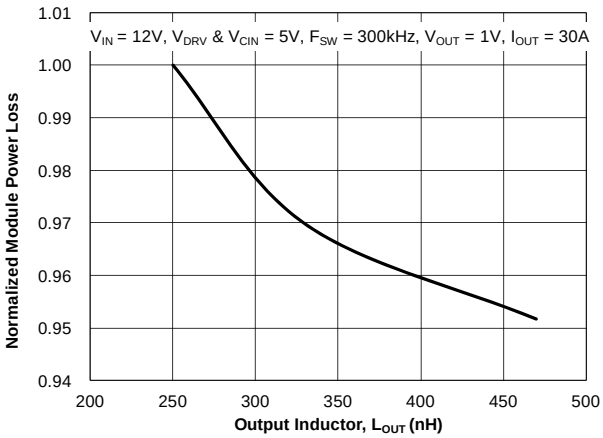


Figure 12. Power Loss vs. Output Inductor

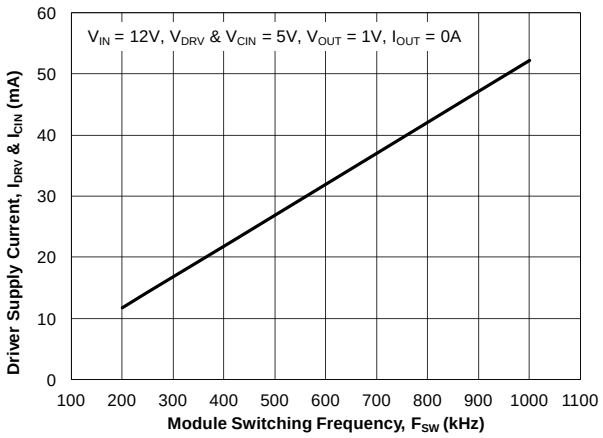


Figure 13. Driver Supply Current vs. Switching Frequency

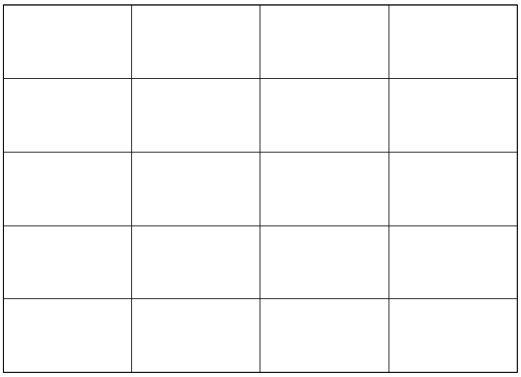


Figure 14. Driver Supply Current vs. Driver Supply Voltage

Figure 15. Driver Supply Current vs. Output Current

Figure 16. UVLO Threshold vs. Temperature

Figure 17. PWM Threshold vs. Driver Supply Voltage

Typical Performance Characteristics

Test Conditions: V_{CIN}=5 V, V_{DRV}=5 V, T_A=25°C, and natural convection cooling, unless otherwise specified.

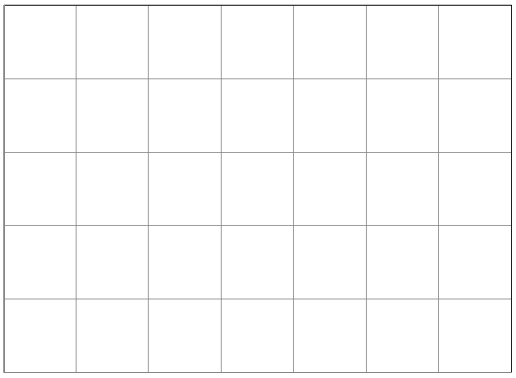


Figure 18. PWM Threshold vs. Temperature

Figure 19. SMOD# Threshold vs. Driver Supply Voltage

Figure 20. SMOD# Threshold vs. Temperature

Figure 21. SMOD# Pull-Up Current vs. Temperature

Figure 22. DISB# Threshold vs. Driver Supply Voltage

Figure 23. DISB# Threshold vs. Temperature

Typical Performance Characteristics

Test Conditions: V_{CIN}=5 V, V_{DRV}=5 V, T_A=25°C, and natural convection cooli

Functional Description

The FDMF6820B is a driver-plus-FET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 1 MHz.

VCIN and Disable (DISB#)

The VCIN pin is monitored by an Under-Voltage Lockout (UVLO) circuit. When V_{CIN} rises above ~3.1 V, the driver is enabled. When V_{CIN} falls below ~2.7 V, the driver is disabled (GH, GL=0). The driver can also be disabled by pulling the DISB# pin LOW (DISB# < V_{IL_DISB}), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH (DISB# > V_{IH_DISB}).

Table 1. UVLO and Disable Logic

UVLO	DISB#	Driver State
0	X	Disabled (GH, GL=0)
1	0	Disabled (GH, GL=0)
1	1	Enabled (*see Table 2*)
1	Open	Disabled (GH, GL=0)

Note:
3. DISB# internal pull-down current source is 10 µA.

Thermal Warning Flag (THWN#)

The FDMF6820B provides a thermal warning flag (THWN#) to warn of over-temperature conditions. The thermal warning flag uses an open-drain output that pulls to CGND when the activation temperature (150°C) is reached. The THWN# output returns to a high-impedance state once the temperature falls to the reset temperature (135°C). For use, the THWN# output requires a pull-up resistor, which can be connected to VCIN. THWN# does NOT disable the DrMOS module.

Figure 26. THWN Operation

Three-State PWM Input

The FDMF6820B incorporates a three-state 3.3 V PWM input gate drive design. The three-state gate drive has both logic HIGH level and LOW level, along with a three-state shutdown window. When the PWM input signal enters and remains within the three-state window for a defined hold-off time ($t_{D\_HOLD-OFF}$), both GL and GH are pulled LOW. This enables the gate drive to shut down both high-side and low-side MOSFETs to support features such as phase shedding, which is common on multi-phase voltage regulators.

Exiting Three-State Condition

When exiting a valid three-state condition, the FDMF6820B follows the PWM input command. If the PWM input goes from three-state to LOW, the low-side MOSFET is turned on. If the PWM input goes from three-state to HIGH, the high-side MOSFET is turned on. This is illustrated in Figure 27. The FDMF6820B design allows for short propagation delays when exiting the three-state window *(see Electrical Characteristics)*.

Low-Side Driver

The low-side driver (GL) is designed to drive a ground-referenced, low-$R_{DS(ON)}$, N-channel MOSFET. The bias for GL is internally connected between the VDRV and CGND pins. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled (DISB#=0 V), GL is held LOW.

High-Side Driver

The high-side driver (GH) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit consisting of the internal Schottky diode and external bootstrap capacitor (C_{BOOT}). During startup, V_{SWH} is held at PGND, allowing C_{BOOT} to charge to V_{DRV} through the

Adaptive Gate Drive Circuit

The driver IC advanced design ensures minimum MOSFET dead-time, while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive adaptively to ensure they do not conduct simultaneously. Figure 27 provides the relevant timing waveforms. To prevent overlap during the LOW-to-HIGH switching transition (Q2 off to Q1 on), the adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes HIGH, Q2 begins to turn off after a propagation delay (t_{PD_PHGLL}). Once the GL pin is discharged below 1.0 V, Q1 begins to turn on after adaptive delay t_{D_DEADON}.

To preclude overlap during the HIGH-to-LOW transition (Q1 off to Q2 on), the adaptive circuitry monitors the voltage at the GH-to-PHASE pin pair. When the PWM signal goes LOW, Q1 begins to turn off after a propagation delay (t_{PD_PLGHL}). Once the voltage across GH-to-PHASE falls below 2.2 V, Q2 begins to turn on after adaptive delay $t_{D\_DEADOFF}$.

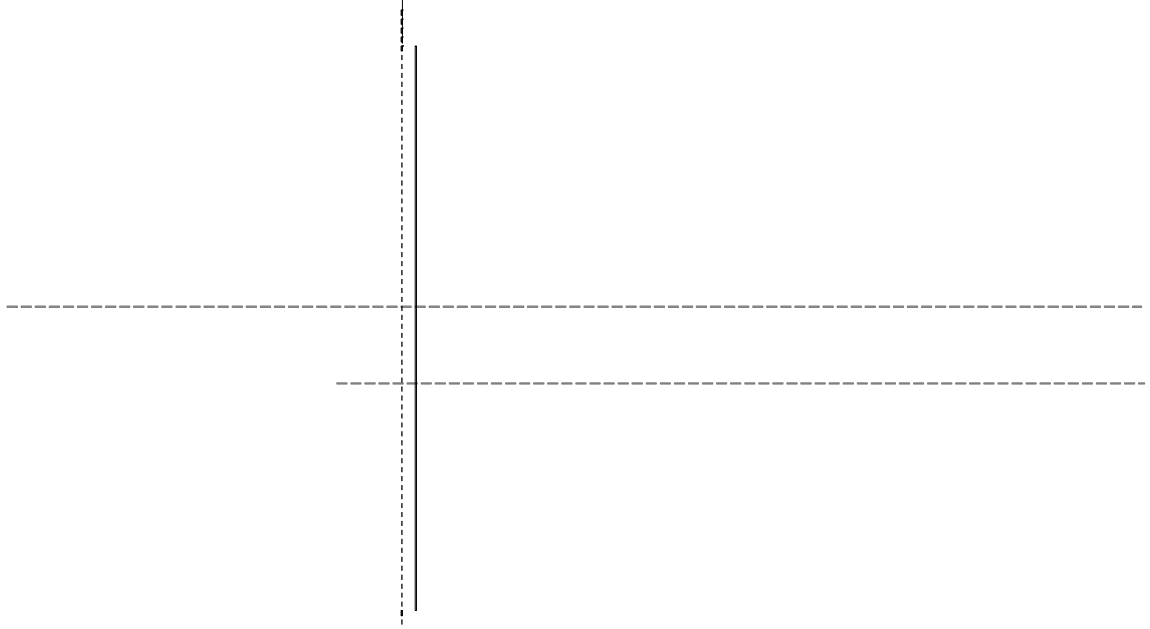


Figure 27. PWM and 3-StateTiming Diagram

Skip Mode (SMOD#)

The Skip Mode function allows for higher converter efficiency when operated in light-load conditions. When SMOD# is pulled LOW, the low-side MOSFET gate signal is disabled (held LOW), preventing discharge of the output capacitors as the filter inductor current attempts reverse current flow – known as “Diode Emulation” Mode.

When the SMOD# pin is pulled HIGH, the synchronous

PCB Layout Guidelines

Figure 31 and Figure 32 provide an example of a proper layout for the FDMF6820B and critical components. All of the high-current paths, such as VIN, VSWH, VOUT, and GND copper, should be short and wide for low inductance and resistance. This aids in achieving a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

Recommendations for PCB Designers

1. Input ceramic bypass capacitors must be placed close to the VIN and PGND pins. This helps reduce the high-current power loop inductance and the input current ripple induced by the power MOSFET switching operation.
2. The V_{SWH} copper trace serves two purposes. In addition to being the high-frequency current path from the DrMOS package to the output inductor, it serves as a heat sink for the low-side MOSFET in the DrMOS package. The trace should be short and wide enough to present a low-impedance path for the high-frequency, high-current flow between the DrMOS and inductor. The short and wide trace minimizes electrical losses as well as the DrMOS temperature rise. Note that the V

Physical Dimensions

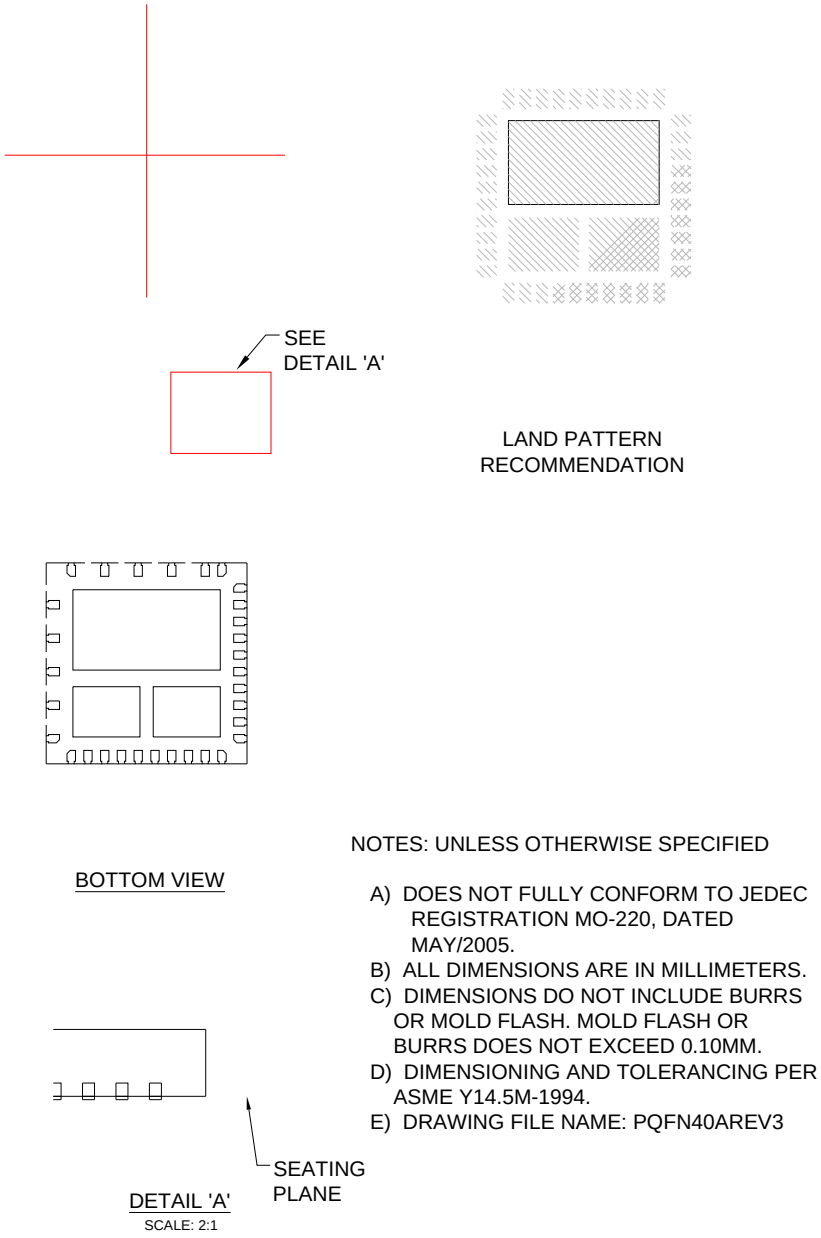


Figure 33. 40-Lead, Clipbond PQFN DrMOS, 6.0x6.0 mm Package

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