



## Benefits

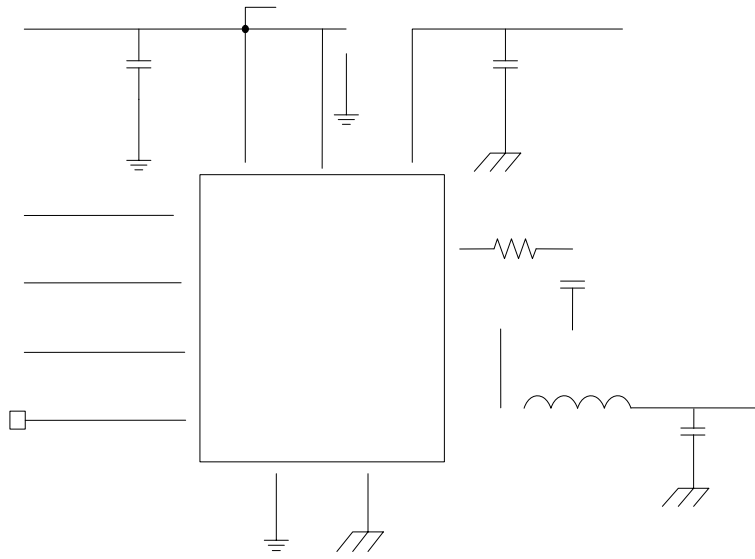
- Ultra-Compact 6x6 mm PQFN, 72% Space-Saving Compared to Conventional Discrete Solutions
- Fully Optimized System Efficiency
- Clean Switching Waveforms with Minimal Ringing
- High-Current Handling

## Features

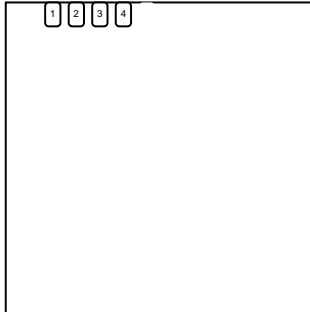
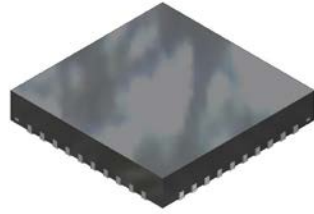
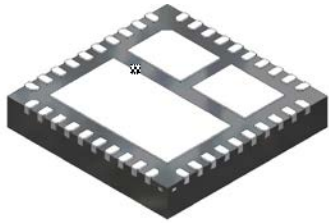
- Over 93% Peak-Efficiency
- High-Current Handling: 50 A
- High-Performance PQFN Copper-Clip Package
- 3-State 3.3 V PWM Input Driver
- Skip-Mode SMOD# (Low-Side Gate Turn Off) Input
- Thermal Warning Flag for Over-Temperature

M--#00P000 (per)7d [(ar)-41.P(ni)29.2(ng)]TJ 0 Tc 0 Tw 3.182 0ind (F)Tj)-0.04 Tc 0.04 Tw 091artion lagW

### Typical Application Circuit



### Pin Configuration







## **Electrical Characteristics**

Typical values are  $V_{IN} = 12\text{ V}$ ,  $V_{CIN} = 5\text{ V}$ ,  $V_{DRV} = 5\text{ V}$ , and  $T_A = T$







## Typical Performance Characteristics

Test Conditions:  $V_{IN}=12\text{ V}$ ,  $V_{OUT}=1\text{ V}$ ,  $V_{CN}=5\text{ V}$ ,  $V_{DRV}=5\text{ V}$ ,  $L_{OUT}=250\text{ nH}$ ,  $T_A=25^\circ\text{C}$ , and natural convection cooling, unless otherwise specified.

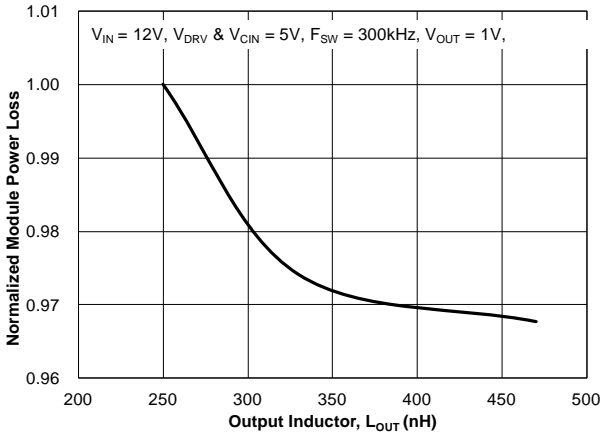


Figure 12. Power Loss vs. Output Inductor

Figure 13. Driver Supply Current vs. Switching Frequency

Figure 14. Driver Supply Current vs. Driver Supply Voltage

Figure 15. Driver Supply Current vs. Output Current

Figure 16. UVLO Threshold vs. Temperature

Figure 17. PWM Threshold vs. Driver Supply Voltage

## Typical Performance Characteristics

Test Conditions:  $V_{CIN}=5\text{ V}$ ,  $V_{DRV}=5\text{ V}$ ,  $T_A=25^\circ\text{C}$ , and natural convection cooling, unless otherwise specified.

Figure 18. PWM Threshold vs. Temperature

Figure 19. SMOD# Threshold vs. Driver Supply Voltage

Figure 20. SMOD# Threshold vs. Temperature

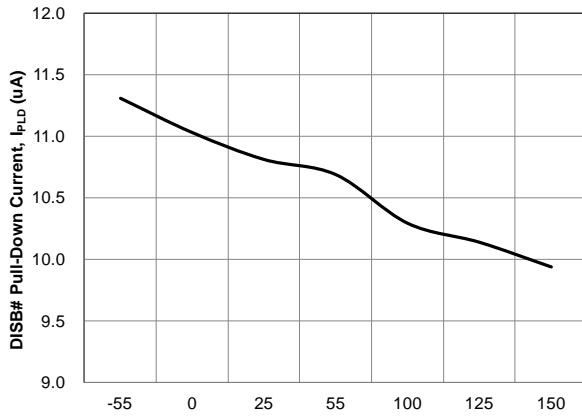
Figure 21. SMOD# Pull-Up Current vs. Temperature

Figure 22. DISB# Threshold vs. Driver Supply Voltage

Figure 23. DISB# Threshold vs. Temperature

## Typical Performance Characteristics

Test Conditions:  $V_{CIN}=5\text{ V}$ ,  $V_{DRV}=5\text{ V}$ ,  $T_A=25^\circ\text{C}$ , and natural convection cooling, unless otherwise specified.



**Figure 24. DISB# Pull-Down Current vs. Temperature**

**Figure 25. Boot Diode Forward Voltage vs. Temperature**







## Application Information

### Supply Capacitor Selection

For the supply inputs ( $V_{\text{CIN}}$ ), a local ceramic bypass capacitor is recommended to reduce noise and to supply the peak current. Use at least a 1  $\mu\text{F}$  X7R or X5R capacitor. Keep this capacitor close to the VCIN pin and connect it to the GND plane with vias.

### Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor ( $C_{\text{BOOT}}$ ), as shown in Figure 30. A bootstrap capacitance of 100 nF X7R or X5R capacitor is usually adequate. A series bootstrap resistor may be needed for specific applications to improve switching noise immunity. The boot







**Physical Dimensions**

SEE  
DETAIL 'A'

LAND PATTERN  
RECOMMENDATION

BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220, DATED MAY/2005.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN40AREV3

DETAIL 'A'  
SCALE: 2:1

SEATING  
PLANE

**Figure 33. 40-Lead, Clipbond PQFN DrMOS, 6.0x6.0 mm Package**

*Package drawings are provided as a service to customers considering ON Semiconductor components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a ON Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of ON Semiconductor's worldwide terms and conditions, specifically the warranty therein, which covers ON Semiconductor products.*

S7CING P PLANE

