Extra-Small, High-Performance, High-Frequency DrMOS Module

FDMF6821B

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PQFN40 6X6, 0.5P
CASE 483AN

MARKING DIAGRAM

$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDMF6821B	= Specific Device Code

See detailed ordering and shipping information on page 2 of

Description

The XS™ DrMOS family is ON Semiconductor's next generation, fully optimized, ultra compact, integrated MOSFET plus driver power stage solution for high current, high frequency, synchronous buck DC DC applications. The FDMF6821B integrates a driver IC, two power MOSFETs, and a bootstrap Schottky diode into a thermally enhanced, ultra compact 6x6 mm package.

With an integrated approach, the complete switching power stage is optimized with regard to driver and MOSFET dynamic performance, system inductance, and power MOSFET $R_{DS(ON)}$. XS DrMOS uses ON Semiconductor's high performance POWERTRENCH® MOSFET technology, which dramatically reduces switch ringing, eliminating the need for snubber circuit in most buck converter applications.

A driver IC with reduced dead times and propagation delays further enhances the performance. A thermal warning function warns of a potential over temperature situation. The FDMF6821B also incorporates a Skip Mode (SMOD#) for improved light load efficiency. The FDMF6821B also provides a 3 state 3.3 V PWM input for compatibility with a wide range of PWM controllers.

Features

- Over 93% Peak Efficiency
- High Current Handling: 55 A
- High Performance PQFN Copper Clip Package
- 3 State 3.3 V PWM Input Driver
- Skip Mode SMOD# (Low Side Gate Turn Off) Input
- Thermal Warning Flag for Over Temperature Condition
- Driver Output Disable Function (DISB# Pin)
- Internal Pull Up and Pull Down for SMOD# and DISB# Inputs, Respectively
- ON Semiconductor PowerTrench Technology MOSFETs for Clean Voltage Waveforms and Reduced Ringing
- ON Semiconductor SyncFET (Integrated Schottky Diode) Technology in Low Side MOSFET
- Integrated Bootstrap Schottky Diode
- Adaptive Gate Drive Timing for Shoot Through Protection
- Under Voltage Lockout (UVLO)
- Optimized for Switching Frequencies up to 1 MHz
- Low Profile SMD Package
- Based on the Intel® 4.0 DrMOS Standard
- This Device is Pb Free, Halogen Free/BFR Free and is RoHS Compliant

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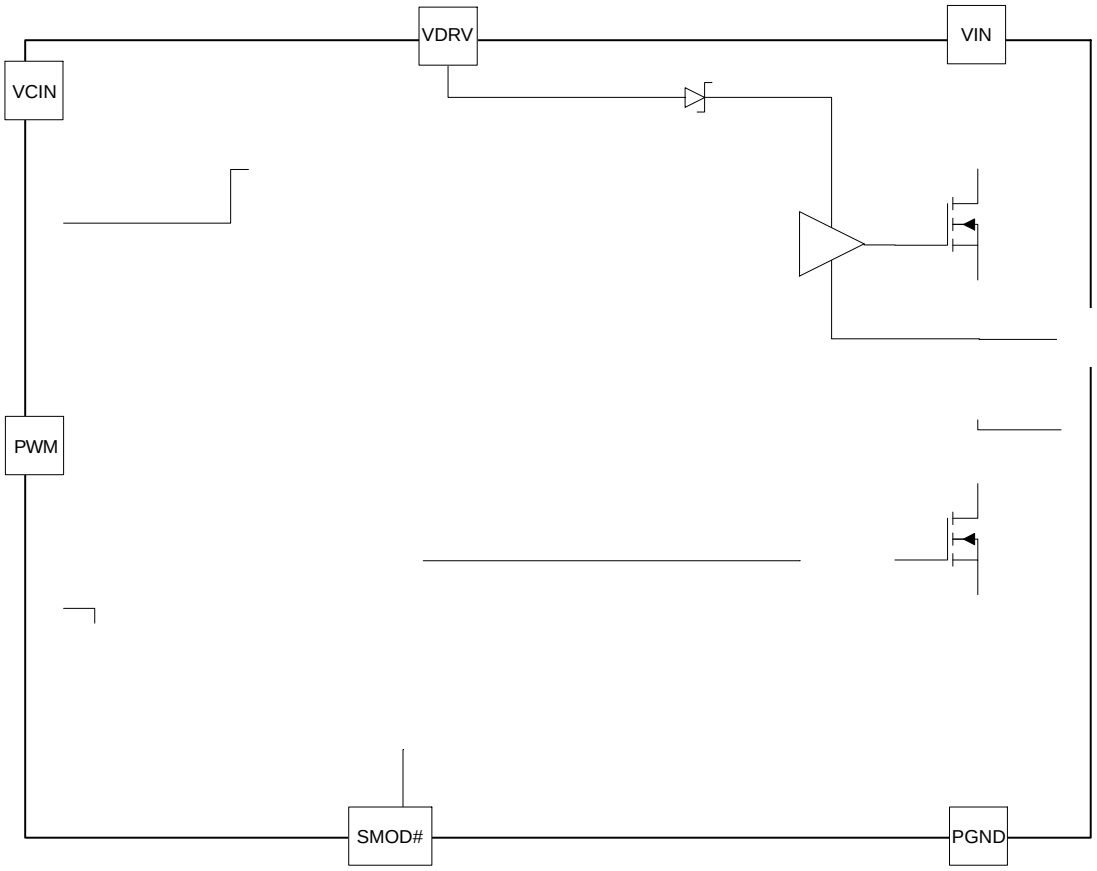

Figure 2. DrMOS Block Diagram

PIN DEFINITIONS

Pin #	Name	Description
1	SMOD#	When SMOD# = HIGH, the low−side driver is the inverse of the PWM input. When SMOD# = LOW, the low−side driver is disabled. This pin has a 10 μA internal pull−up current source. Do not add a noise filter capacitor.
2	VCIN	IC bias supply. Minimum 1 μF ceramic capacitor is recommended from this pin to CGND.
3	VDRV	Power for the gate driver. Minimum 1 μF ceramic capacitor is recommended to be connected as close as possible from this pin to CGND.
4	BOOT	Bootstrap supply input. Provides voltage supply to the high−side MOSFET driver. Connect a bootstrap capacitor from this pin to PHASE.
5, 37, 41	CGND	IC ground. Ground return for driver IC.
6	GH	For manufacturing test only. This pin must float; it must not be connected to any pin.
7	PHASE	Switch node pin for bootstrap capacitor routing. Electrically shorted to VSWH pin.
8	NC	No connect. The pin is not electrically connected internally, but can be connected to VIN for convenience.
9 − 14, 42	VIN	Power input. Output stage supply voltage.
15, 29 − 35, 43	VSWH	Switch node input. Provides return for high−side bootstrapped driver and acts as a sense point for the adaptive shoot−through protection.
16 – 28	PGND	Power ground. Output stage ground. Source pin of the low−side MOSFET.
36	GL	For manufacturing test only. This pin must float; it must not be connected to any pin.
38	THWN#	Thermal warning flag, open collector output. When tela seElrine exceedthe inicap limitthe lotput. s noll.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Unit
V_{CIN}	Supply Voltage	Referenced to CGND	−0.3	6.0	V
V_{DRV}	Drive Voltage	Referenced to CGND	−0.3	6.0	V
$V_{DISB\#}$	Output Disable				

ELECTRICAL CHARACTERISTICS

Typical values are V_{IN} = 12 V, V_{CIN} = 5 V, V_{DRV} = 5 V, and $T_A = T_J$ = +25°C unless otherwise noted.

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Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
THERMAL WARNING FLAG						
T_{ACT}	Activation Temperature			150		°C
T_{RST}	Reset Temperature			135		°C
R_{THWN}	Pull−Down Resistance	I_{PLD} = 5 mA		30		Ω
HIGH−SIDE DRIVER (F_{SW} = 1000 kHz, I_{OUT} = 30 A, T_A = +25°C)						
R_{SOURCE_GH}						

Figure 5. PWM Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: V_{IN} = 12 V, V_{OUT} = 1 V, V_{CIN} = 5 V, V_{DRV} = 5 V, L_{OUT}

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Test Conditions: V_{IN} = 12 V, V_{OUT} = 1 V, V_{CIN}

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The FDMF6821B is a driver plus FET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high side and the low side MOSFETs. Each part is capable of driving speeds up to 1 MHz.

VCIN and Disable (DISB#)

The VCIN pin is monitored by an Under Voltage Lockout (UVLO) circuit. When V_{CIN} rises above ~3.1 V, the driver is enabled. When V_{CIN} falls below ~2.7 V, the driver is disabled (GH, GL = 0). The driver can also be disabled by pulling the DISB# pin LOW (DISB# < V_{IL_DISB}), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH (DISB# > V_{IH_DISB}).

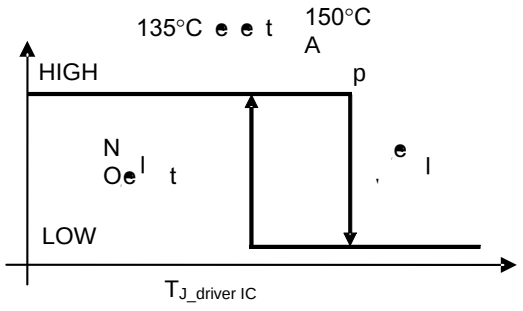
Table 1. UVLO AND DISABLE LOGIC

LO	DI B#	D , I ,
0	X	Disabled (GH, GL = 0)
1	0	Disabled (GH, GL = 0)
1	1	Enabled (see Table 2)
1	Open	Disabled (GH, GL = 0)

3. DISB# internal pull−down current source is 10 μA.

Thermal Warning Flag (THWN#)

The FDMF6821B provides a thermal warning flag (THWN#) to warn of over temperature conditions. The thermal warning flag uses an open drain output that pulls to CGND when the activation temperature (150°C) is reached. The THWN# output returns to a high impedance state once the temperature falls to the reset temperature (135°C). For use, the THWN# output requires a pull up resistor, which can be connected to VCIN. THWN# does NOT disable the DrMOS module.



Adaptive Gate Drive Circuit

The driver IC advanced design ensures minimum MOSFET dead time, while eliminating potential shoot through (cross conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive adaptively to ensure they do not conduct simultaneously. Figure 27 provides the relevant timing waveforms. To prevent overlap during the LOW to HIGH switching transition (Q2 off to Q1 on), the adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes HIGH, Q2 begins to turn off after a propagation delay (t_{PD_PHGLL}). Once the GL pin is discharged below 1.0 V, Q1 begins to turn on after adaptive delay t_{D_DEADON}.

To preclude overlap during the HIGH to LOW transition (Q1 off to Q2 on), the adaptive circuitry monitors the voltage at the GH to PHASE pin pair. When the PWM signal goes ï

APPLICA ION INFORMA ION

Supply Capacitor Selection

For the supply inputs (V_{CIN}), a local ceramic bypass capacitor is recommended to reduce noise and to supply the peak current. Use at least a 1 μF X7R or X5R capacitor. Keep this capacitor close to the VCIN pin and connect it to the

PCB LA O G IDELINE

Figure 31 and Figure 32 provide an example of a proper layout for the FDMF6821B and critical components. All of the high current paths, such as VIN, VSWH, VOUT, and GND copper, should be short and wide for low inductance and resistance. This aids in achieving a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

Recommendations for PCB Designers

1. Input ceramic bypass capacitors must be placed close to the VIN and PGND pins. This helps reduce the high current power loop inductance and the input current ripple induced by the power MOSFET switching operation
2. The V_{SWH} copper trace serves two purposes. In addition to being the high frequency current path from the DrMOS package to the output inductor, it serves as a heat sink for the low side MOSFET in the DrMOS package. The trace should be short and wide enough to present a low impedance path for the high frequency, high current flow between the DrMOS and inductor. The short and wide trace minimizes electrical losses as well as the DrMOS temperature rise. Note that the V_{SWH} node is a high voltage and high frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. Since this copper trace acts as a heat sink for the lower MOSFET, balance using the largest area possible to improve DrMOS cooling while maintaining acceptable noise emission
3. An output inductor should be located close to the FDMF6821B to minimize the power loss due to the V_{SWH} copper trace. Care should also be taken so the inductor dissipation does not heat the DrMOS
4. POWERTRENCH MOSFETs are used in the output stage and are effective at minimizing ringing due to fast switching. In most cases, no VSWH snubber is required. If a snubber is used, it should be placed close to the VSWH and PGND pins. The selected resistor and capacitor need to be the proper size for power dissipation
5. VCIN, VDRV, and BOOT capacitors should be placed as close as possible to the VCIN to CGND, VDRV to CGND, and BOOT to PHASE pin pairs to ensure clean and stable power. Routing width and length should be considered as well
6. Include a trace from the PHASE pin to the VSWH pin to improve noise margin. Keep this trace as short as possible
7. The layout should include the option to insert a small value series boot resistor between the boot capacitor and BOOT pin. The boot loop size, including R_{BOOT}, 024race aln2.3292 Tm.0003 Tc(BOOT)Tj10 0 0 10 158205.2 1028 Tc-0024 Tw(layout for /TT6 2ohc62ohj8l1R

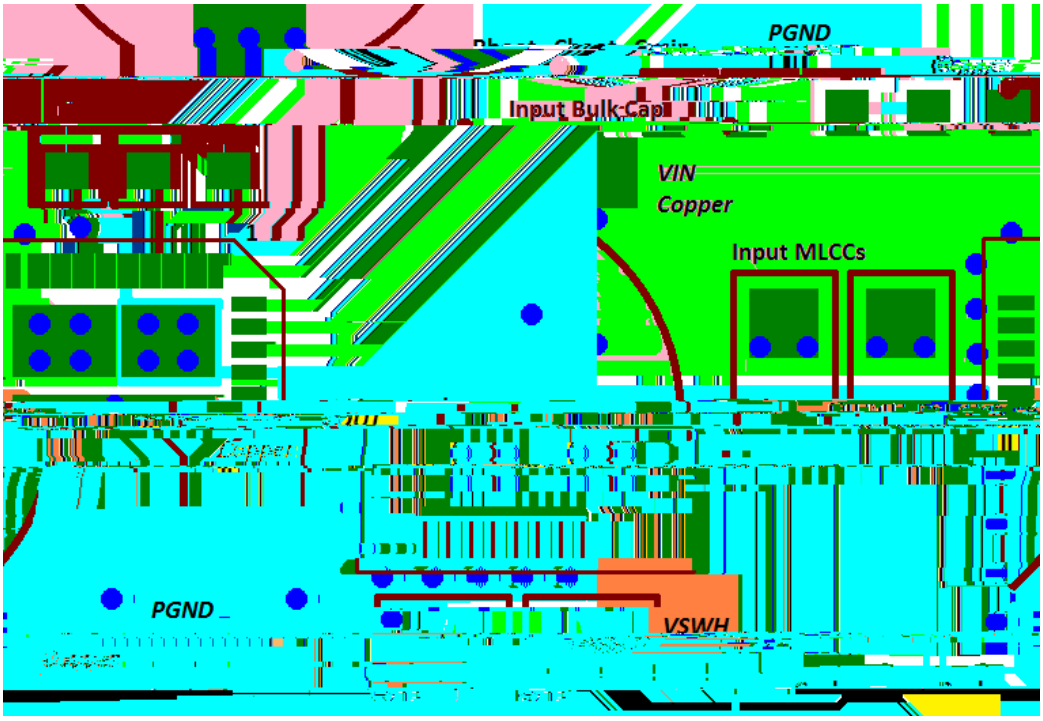


Figure 31. PCB Layout Example (Top View)

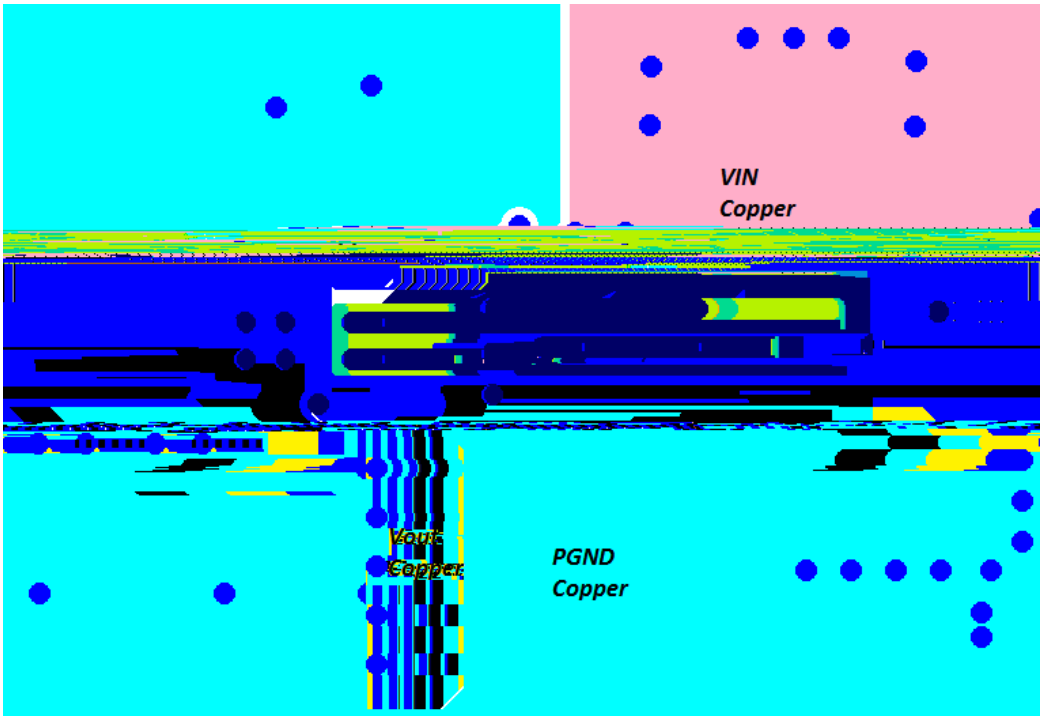


Figure 32. PCB Layout Example (Bottom View)

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