

**Description**  
TM

**FDMF6821C**

# FDMF6821C

## DrMOS Block Diagram

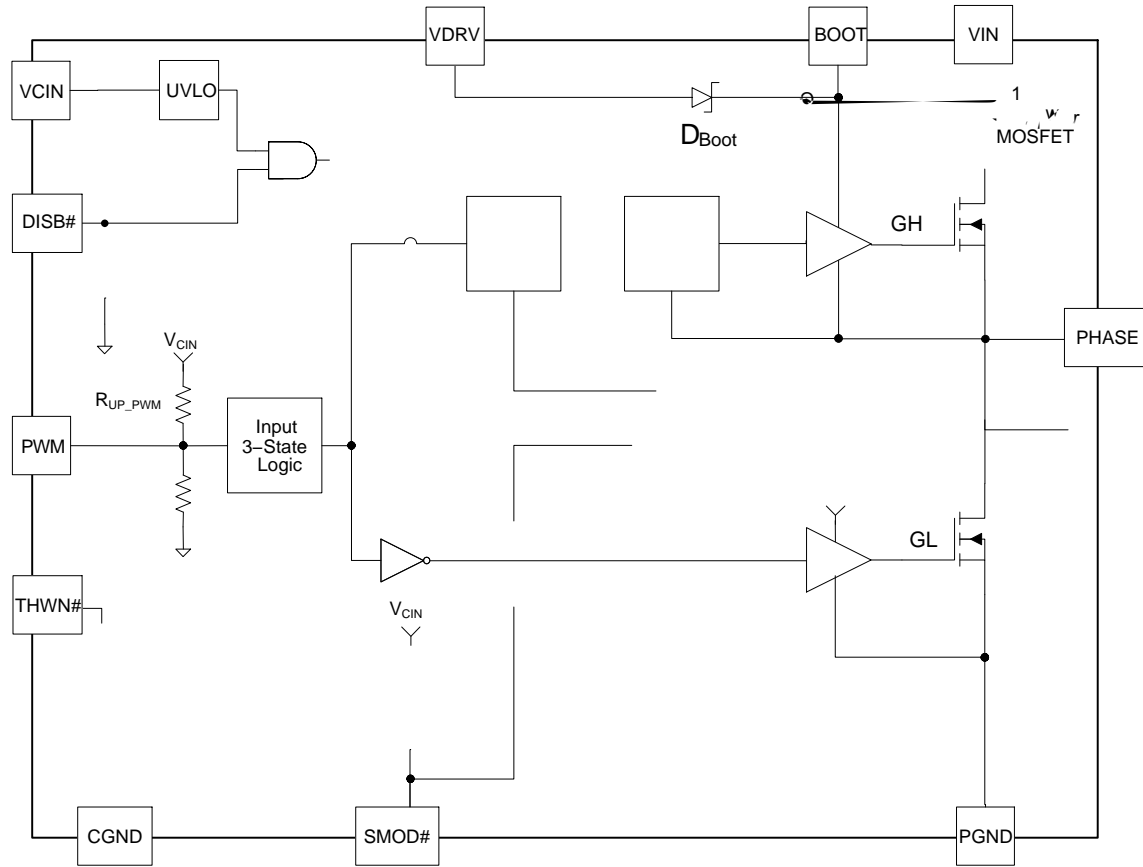


Figure 2. DrMOS Block Diagram

# FDMF6821C

## PIN DEFINITIONS

Pin #	Name	Description
1	SMOD#	When SMOD# = HIGH, the low-side driver is the inverse of the PWM input. When SMOD# = LOW, the low-side driver is disabled. This pin has a 10 $\mu$ A internal pull-up current source. Do not add a noise filter capacitor.
2	VCIN	IC bias supply. Minimum 1 $\mu$ F ceramic capacitor is recommended from this pin to CGND.
3	VDRV	Power for the gate driver. Minimum 1 $\mu$ F ceramic capacitor is recommended to be connected as close as possible from this pin to CGND.
4		

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## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Unit
V <sub>CIN</sub>	Supply Voltage	Referenced to CGND	-0.3	6.0	V
V <sub>DRV</sub>	Drive Voltage	Referenced to CGND	-0.3	6.0	V
V <sub>DISB#</sub>	Output Disable	Referenced to CGND	-0.3	6.0	V
V <sub>PWM</sub>	PWM Signal Input	Referenced to CGND	-0.3	6.0	V
V <sub>SMOD#</sub>	Skip Mode Input	Referenced to CGND	-0.3	6.0	V
V <sub>GL</sub>	Low Gate Manufacturing Test Pin	Referenced to CGND	-0.3	6.0	V
V <sub>THWN#</sub>	Thermal Warning Flag	Referenced to CGND	-0.3	6.0	V
V <sub>IN</sub>	Power Input	V			

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## ELECTRICAL CHARACTERISTICS

Typical values are  $V_{IN} = 12\text{ V}$ ,  $V_{CIN} = 5\text{ V}$ ,  $V_{DRV} = 5\text{ V}$ , and  $T_A = T_J = +25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
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### THERMAL WARNING FLAG

TACT	Activation Temperature			150		°C
TRST	Reset Temperature			135		°C
RTHWN	Pull-Down Resistance	$I_{PLD} = 5\text{ mA}$				

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Figure 5. PWM Timing Diagram



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## TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions:  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 1\text{ V}$ ,  $V_{CIN} = 5\text{ V}$ ,  $V_{DRV} = 5\text{ V}$ ,  $L_{OUT} = 250\text{ nH}$ ,  $T_A = 25^\circ\text{C}$ , and natural convection cooling, unless otherwise specified.

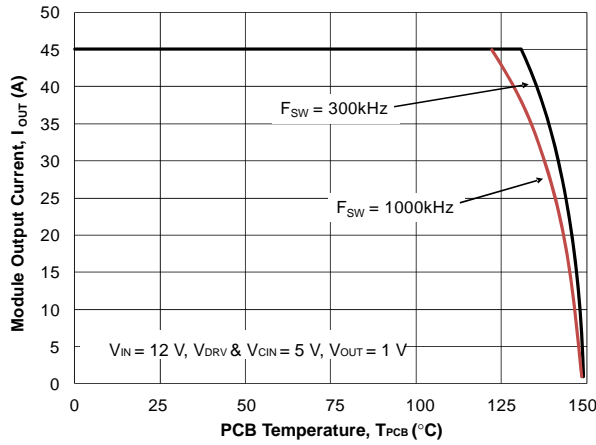


Figure 6. Safe Operating Area

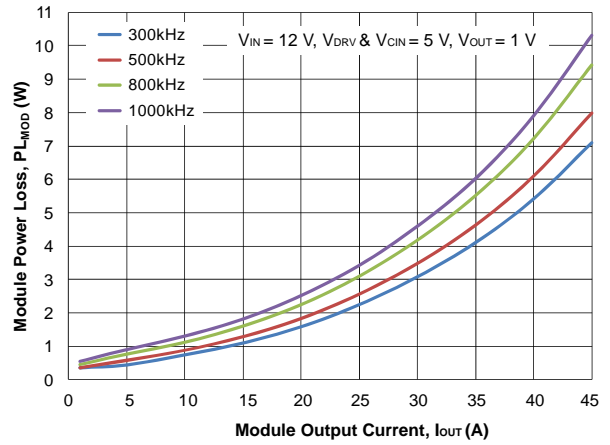


Figure 7. Power Loss vs. Output Current

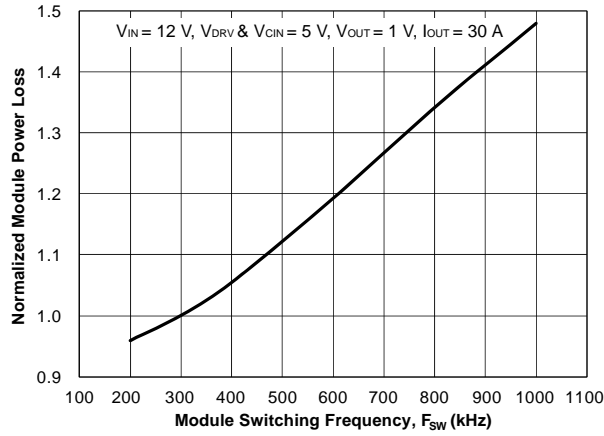


Figure 8. Power Loss vs. Switching Frequency

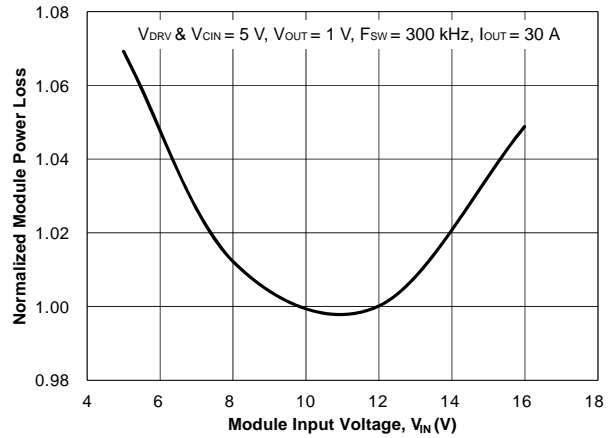


Figure 9. Power Loss vs. Input Voltage

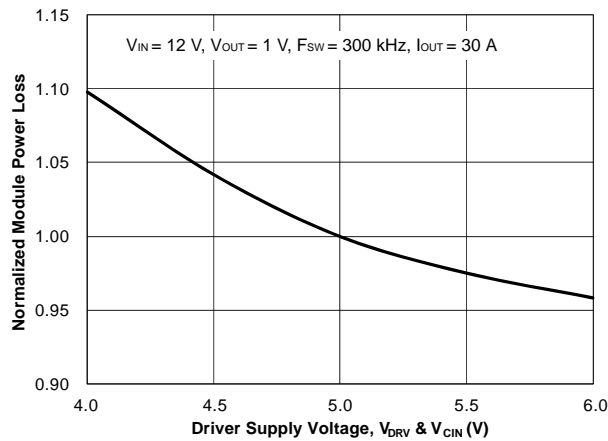


Figure 10. Power Loss vs. Driver Supply Voltage

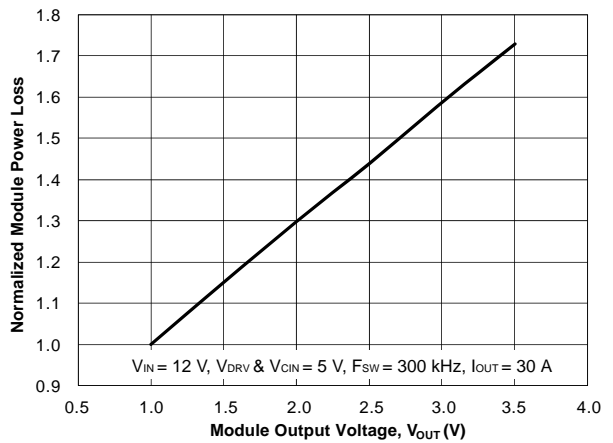


Figure 11. Power Loss vs. Output Voltage



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## TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions:  $V_{CIN} = 5\text{ V}$ ,  $V_{DRV} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , and natural convection cooling, unless otherwise specified.

Figure 18. PWM Threshold vs. Temperature

Figure 19. SMOD# Threshold vs. Driver Supply Voltage



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## FUNCTIONAL DESCRIPTION

### Three-State PWM Input

### VCIN and Disable (DISB#)

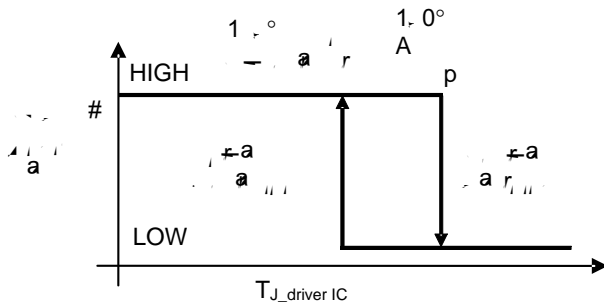
### Exiting Three-

**Table 1. UVLO AND DISABLE LOGIC**

UVLO	DISB#	Driver State
0	X	Disabled (GH, GL = 0)
1	0	Disabled (GH, GL = 0)
1	1	Enabled (see Table 2)
1	Open	Disabled (GH, GL = 0)

3. DISB# internal pull-down current source is 10  $\mu$ A.

### Thermal Warning Flag (THWN#)



**Figure 26. THWN Operation**

Adaptive Gate Drive Circuit



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## APPLICATION INFORMATION

### Supply Capacitor Selection

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## PCB LAYOUT GUIDELINES

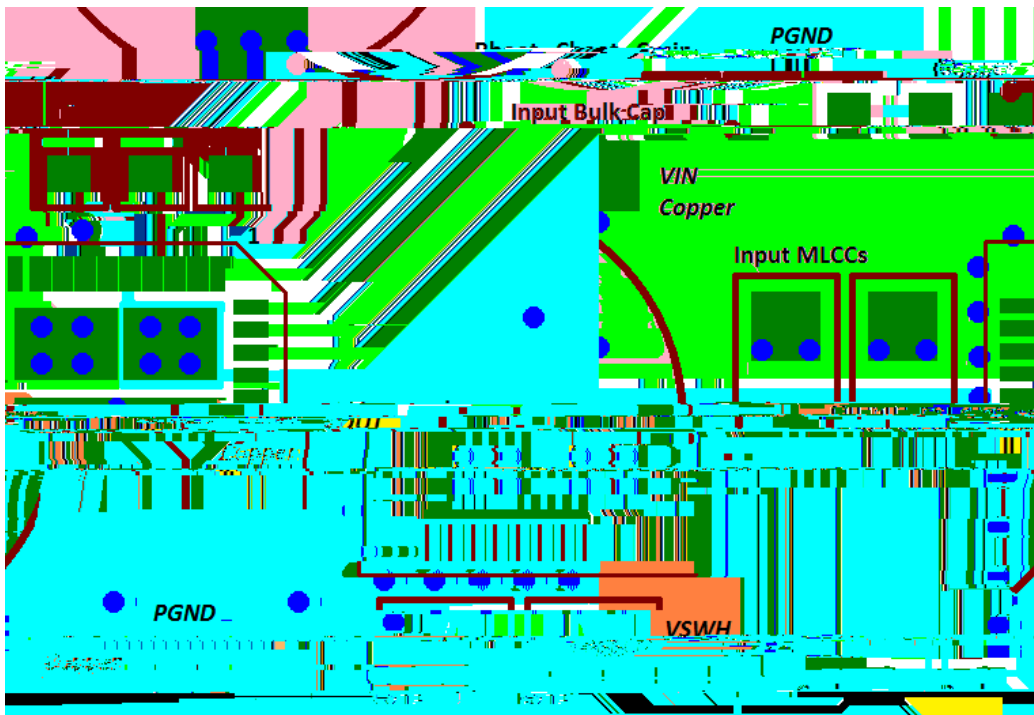


Figure 31. PCB Layout Example (Top View)

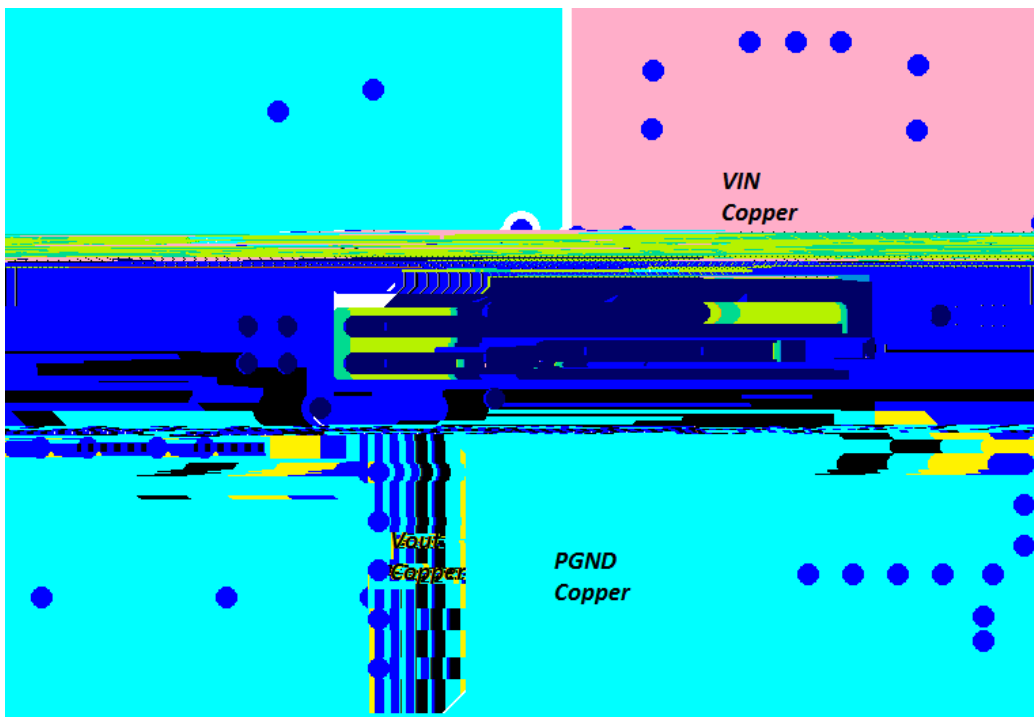
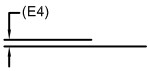
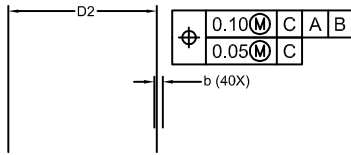
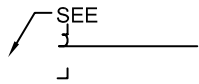


Figure 32. PCB Layout Example (Bottom View)

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