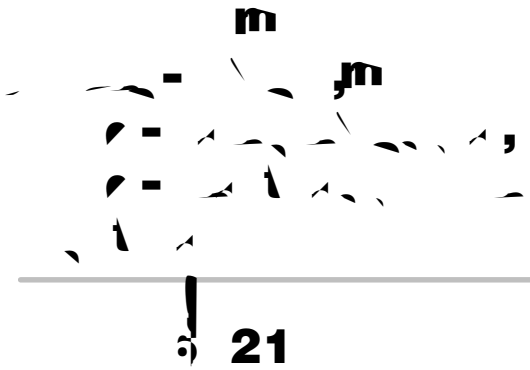

Description

™

FDMF6821C

DrMOS Block Diagram

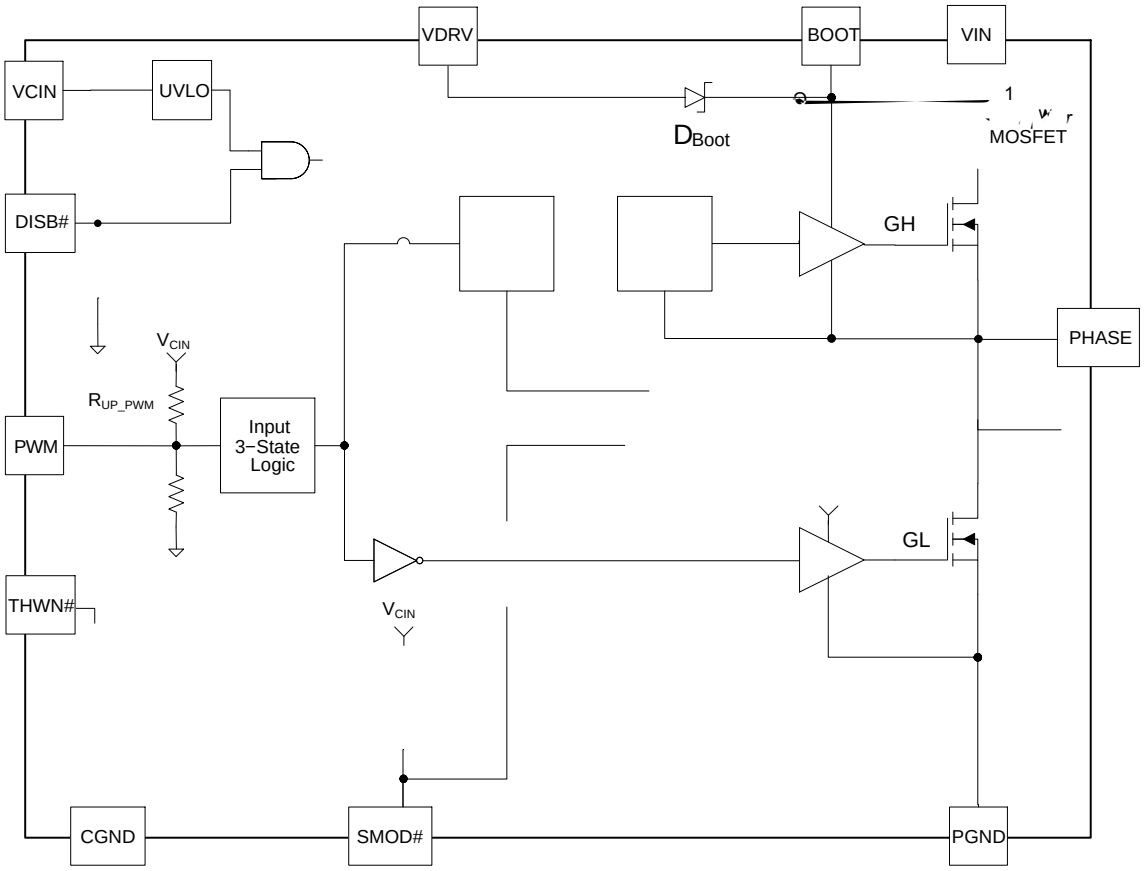

Figure 2. DrMOS Block Diagram

PIN DEFINITIONS

Pin #	Name	Description
1	SMOD#	When SMOD# = HIGH, the low−side driver is the inverse of the PWM input. When SMOD# = LOW, the low−side driver is disabled. This pin has a 10 μA internal pull−up current source. Do not add a noise filter capacitor.
2	VCIN	IC bias supply. Minimum 1 μF ceramic capacitor is recommended from this pin to CGND.
3	VDRV	Power for the gate driver. Minimum 1 μF ceramic capacitor is recommended to be connected as close as possible from this pin to CGND.
4		

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Unit
V_{CIN}	Supply Voltage	Referenced to CGND	−0.3	6.0	V
V_{DRV}	Drive Voltage	Referenced to CGND	−0.3	6.0	V
$V_{DISB\#}$	Output Disable	Referenced to CGND	−0.3	6.0	V
V_{PWM}	PWM Signal Input	Referenced to CGND	−0.3	6.0	V
$V_{SMOD\#}$	Skip Mode Input	Referenced to CGND	−0.3	6.0	V
V_{GL}	Low Gate Manufacturing Test Pin	Referenced to CGND	−0.3	6.0	V
$V_{THWN\#}$	Thermal Warning Flag	Referenced to CGND	−0.3	6.0	V
V_{IN}	Power Input	V			

ELECTRICAL CHARACTERISTICS

Typical values are V_{IN} = 12 V, V_{CIN} = 5 V, V_{DRV} = 5 V, and $T_A = T_J$ = +25°C unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
THERMAL WARNING FLAG						
T_{ACT}	Activation Temperature			150		°C
T_{RST}	Reset Temperature			135		°C
R_{THWN}	Pull−Down Resistance	I_{PLD} = 5 mA				

Figure 5. PWM Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: V_{IN} = 12 V, V_{OUT} = 1 V, V_{CIN} = 5 V, V_{DRV} = 5 V, L_{OUT} = 250 nH, T_A = 25°C, and natural convection cooling, unless otherwise specified.

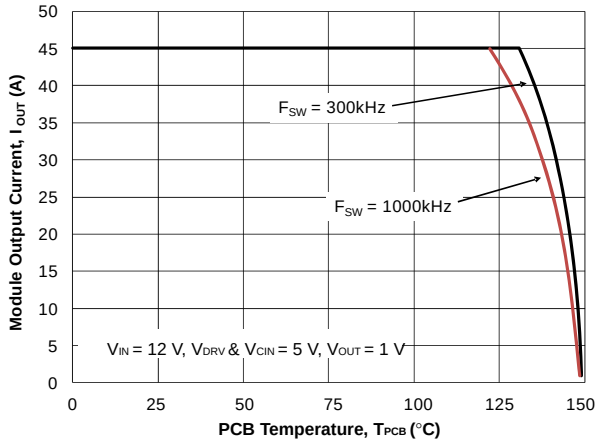

Figure 6. Safe Operating Area

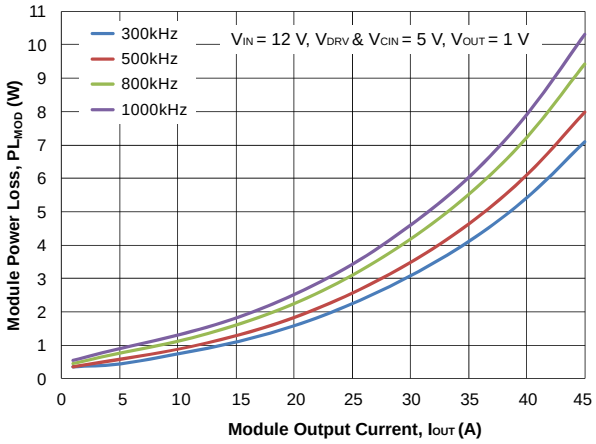

Figure 7. Power Loss vs. Output Current

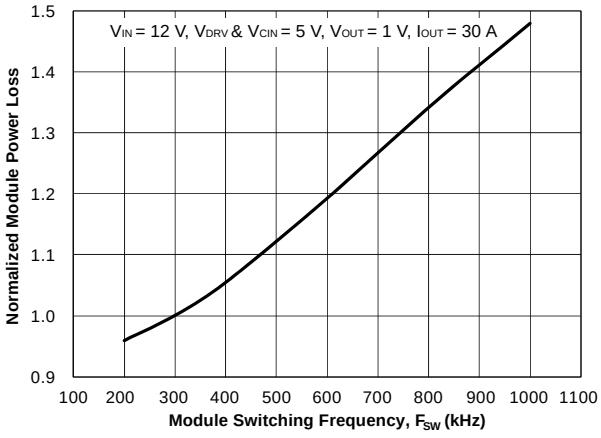

Figure 8. Power Loss vs. Switching Frequency

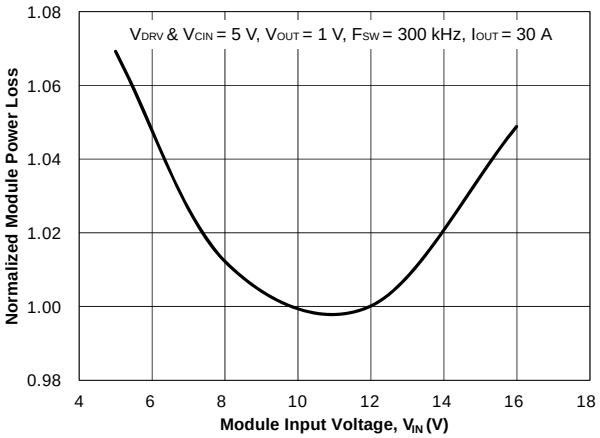

Figure 9. Power Loss vs. Input Voltage

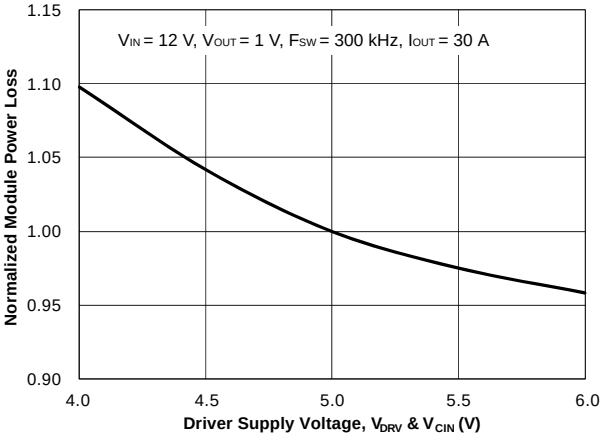

Figure 10. Power Loss vs. Driver Supply Voltage

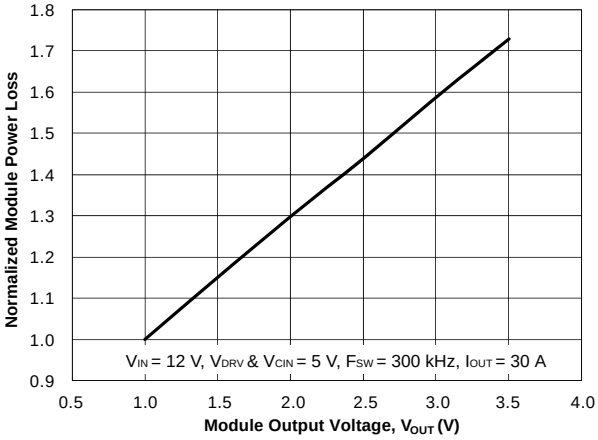

Figure 11. Power Loss vs. Output Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: V_{CIN} = 5 V, V_{DRV} = 5 V, T_A = 25°C, and natural convection cooling, unless otherwise specified.

Figure 18. PWM Threshold vs. Temperature

Figure 19. SMOD# Threshold vs. Driver Supply Voltage

FUNCTIONAL DESCRIPTION

Three−State PWM Input

VCIN and Disable (DISB#)

Exiting Three−

Table 1. UVLO AND DISABLE LOGIC

UVLO	DISB#	Driver State
0	X	Disabled (GH, GL = 0)
1	0	Disabled (GH, GL = 0)
1	1	Enabled (see Table 2)
1	Open	Disabled (GH, GL = 0)

3. DISB# internal pull−down current source is 10 μA.

Thermal Warning Flag (THWN#)

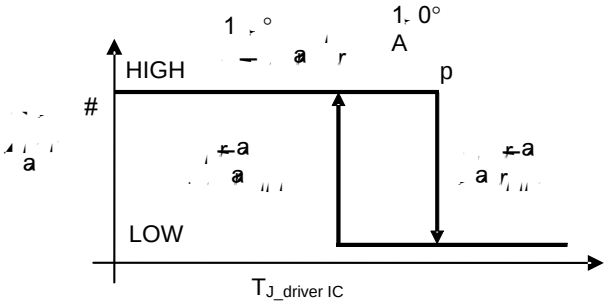

Figure 26. THWN Operation

Adaptive Gate Drive Circuit

APPLICATION INFORMATION

Supply Capacitor Selection

μ

PCB LAYOUT GUIDELINES

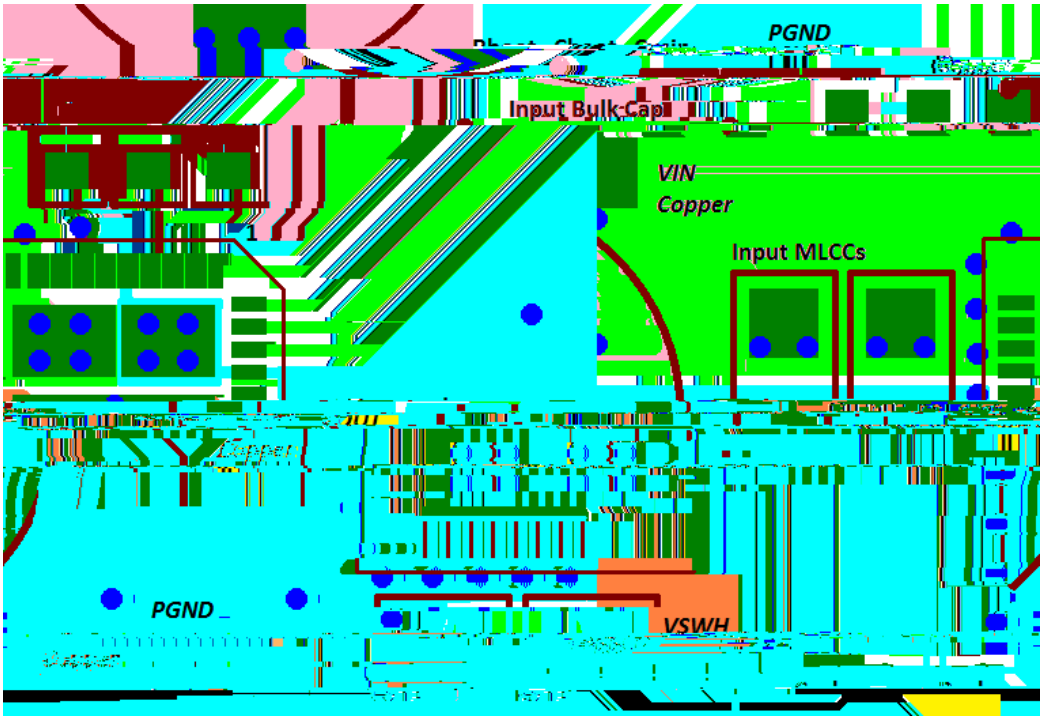

Figure 31. PCB Layout Example (Top View)

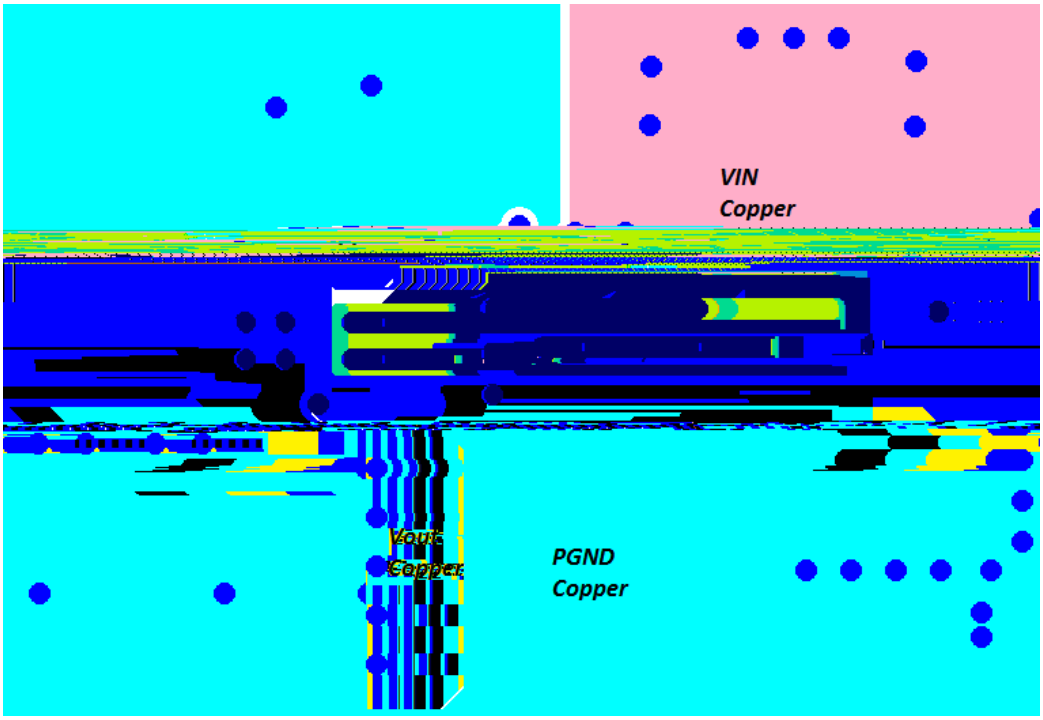

Figure 32. PCB Layout Example (Bottom View)

CASE 483AN
ISSUE A

DATE 08 JUN 2021