

Description

The XS[™] DrMOS family is ON Semiconductor's next–generation, fully optimized, ultra–compact, integrated MOSFET plus driver power stage solution for high–current, high– frequency, synchronous buck DC–DC applications. The FDMF6821C integrates a driver IC, two power MOSFETs, and a bootstrap Schottky diode into a thermally enhanced, ultra

DrMOS Block Diagram

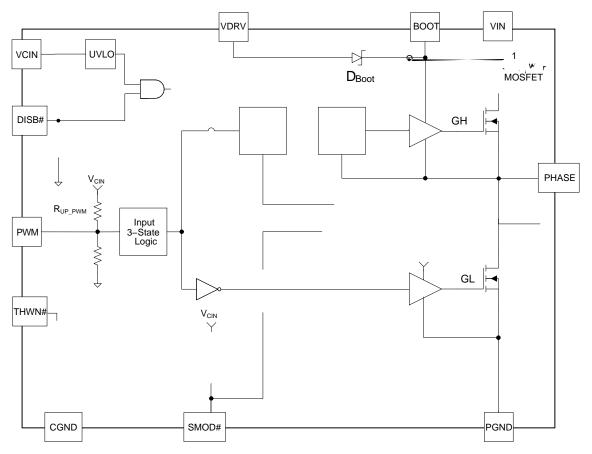


Figure 2. DrMOS Block Diagram

PIN DEFINITIONS

Pin #	Name	Description	
1		When SMOD# = HIGH, the low-side driver is the inverse of the PWM input. When SMOD# = LOW, the low-side driver is disabled. This pin has a 10 μ A internal pull-up current source. Do not add a noise filter capacitor.	
2	VCIN	C bias supply. Minimum 1 μ F ceramic capacitor is recommended from this pin to CGND.	
3		Power for the gate driver. Minimum 1 μ F ceramic capacitor is recommended to be connected as close as possible from this pin to CGND.	
4			

ABSOLUTE MAXIMUM RATINGS

Symbol	Pa	rameter	Min.	Max.	Unit
VCIN	Supply Voltage	Referenced to CGND	-0.3	6.0	V
Vdrv	Drive Voltage	Referenced to CGND	-0.3	6.0	V
VDISB#	Output Disable	Referenced to CGND	-0.3	6.0	V
VPWM	PWM Signal Input	Referenced to CGND	-0.3	6.0	V
Vsmod#	Skip Mode Input	Referenced to CGND	-0.3	6.0	V
Vgl	Low Gate Manufacturing Test Pin	Referenced to CGND	-0.3	6.0	V
Vthwn#	Thermal Warning Flag	Referenced to CGND	-0.3	6.0	V
Vin	Power Input	V	-	-	-

ELECTRICAL CHARACTERISTICS

Typical values are V_{IN} = 12 V, V_{CIN} = 5 V, V_{DRV} = 5 V, and T_A = T_J = +25°C unless otherwise noted.

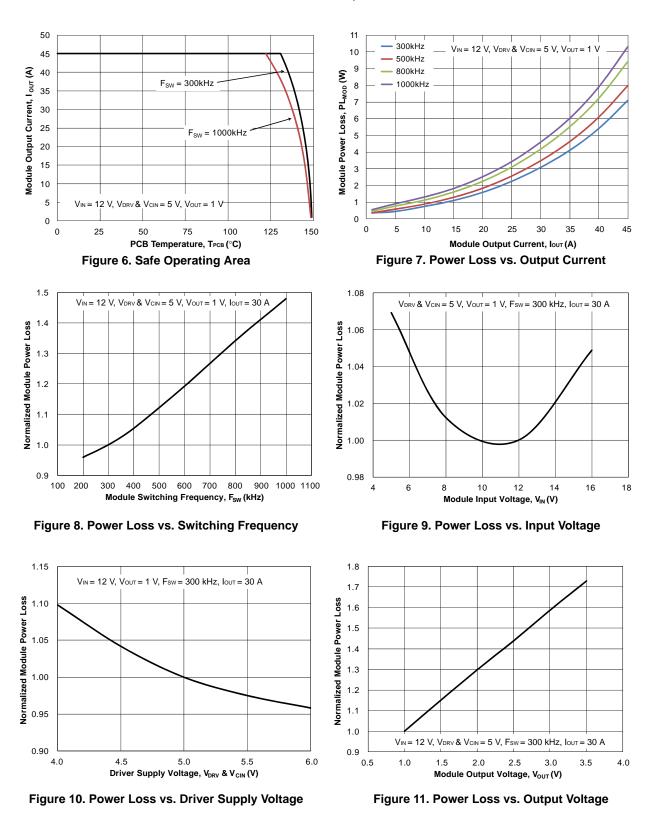
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
THERMAL WARNING FLAG						
Таст	Activation Temperature			150		°C
Trst	Reset Temperature			135		°C
Rthwn	Pull–Down Resistance	I _{PLD} = 5 mA				

Figure 5. PWM Timing Diagram

I

TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: $V_{IN} = 12 \text{ V}$, $V_{OUT} = 1 \text{ V}$, $V_{CIN} = 5 \text{ V}$, $V_{DRV} = 5 \text{ V}$, $L_{OUT} = 250 \text{ nH}$, $T_A = 25^{\circ}\text{C}$, and natural convection cooling, unless otherwise specified.



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TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: $V_{CIN} = 5 V$, $V_{DRV} = 5 V$, $T_A = 25^{\circ}C$, and natural convection cooling, unless otherwise specified.

Figure 18. PWM Threshold vs. Temperature

Figure 19. SMOD# Threshold vs. Driver Supply Voltage

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FUNCTIONAL DESCRIPTION

The FDMF6821C is a driver-plus-FET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 1 MHz.

VCIN and Disable (DISB#)

The VCIN pin is monitored by an Under–Voltage Lockout (UVLO) circuit. When V_{CIN} rises above ~3.1 V, the driver is enabled. When V_{CIN} falls below ~2.7 V, the driver is disabled (GH, GL = 0). The driver can also be disabled by pulling the DISB# pin LOW (DISB# < V_{IL_DISB}), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH (DISB# > V_{IH_DISB}).

Table 1. UVLO AND DISABLE LOGIC

UVLO	DISB#	Driver State
0	Х	Disabled (GH, GL = 0)
1	0	Disabled (GH, $GL = 0$)
1	1	Enabled (see Table 2)
1	Open	Disabled (GH, $GL = 0$)

3. DISB# internal pull-down current source is 10 $\mu\text{A}.$

Thermal Warning Flag (THWN#)

The FDMF6821C provides a thermal warning flag (THWN#) to warn of over-temperature conditions. The thermal warning flag uses an open-drain output that pulls to CGND when the activation temperature (150°C) is reached. The THWN# output returns to a high- impedance state once the temperature falls to the reset temperature (135°C). For use, the THWN# output requires a pull-up resistor, which can be connected to VCIN. THWN# does NOT disable the DrMOS module.

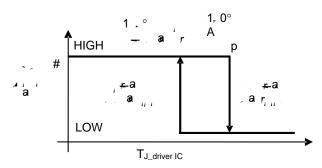


Figure 26. THWN Operation

Three-State PWM Input

The FDMF6821C incorporates a three–state 3.3 V PWM input gate drive design. The three–state gate drive has both logic HIGH level and LOW level, along with a three–state shutdown window. When the PWM input signal enters and remains within the three–state window for a defined hold–off time ($t_{D_HOLD-OFF}$), both GL and GH are pulled LOW. This enables the gate drive to shut down both high–side and Iow–side MOSFETs to support features such as phase shedding, which is common on multi–phase voltage regulators.

Exiting Three-

Adaptive Gate Drive Circuit

APPLICATION INFORMATION

Supply Capacitor Selection

For the supply inputs (V_{CIN}), a local ceramic bypass capacitor is recommended to reduce noise and to supply the peak current. Use at least a 1 μ F X7R or X5R capacitor. Keep this capacitor close to the VCIN pin and connect it to the

PCB LAYOUT GUIDELINES

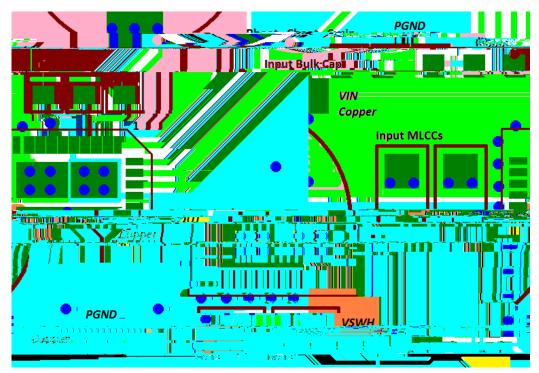


Figure 31. PCB Layout Example (Top View)

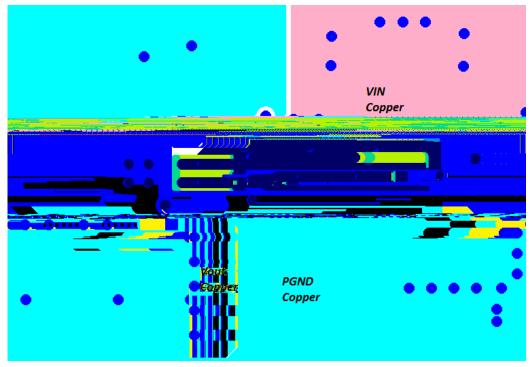


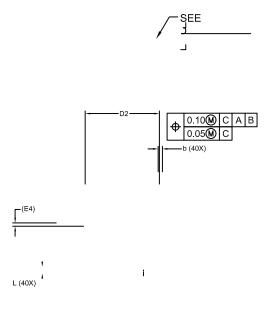
Figure 32. PCB Layout Example (Bottom View)

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