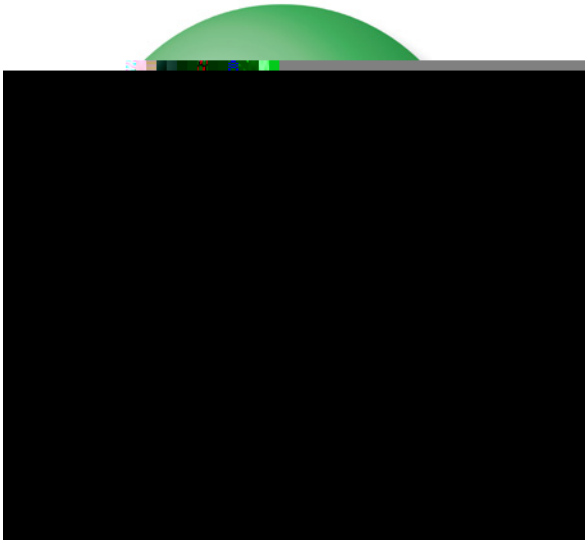
Is Now Part of



To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD
SEMICONDUCTOR®

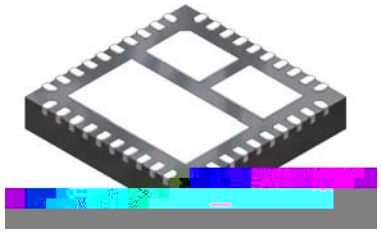
April 2013

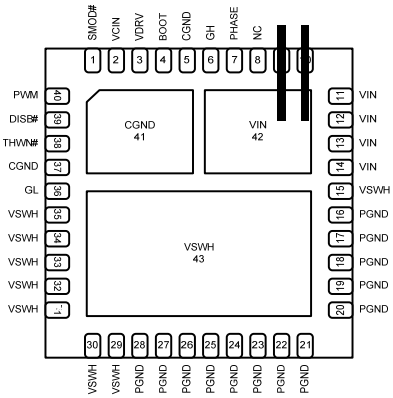
FDMF6823A — Extra-Small, High-Performance, High-Frequency DrMOS Module

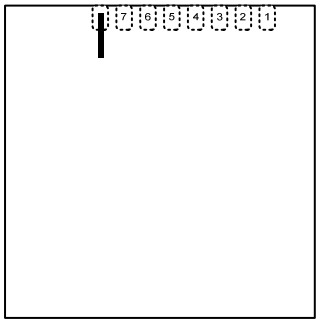
Benefits

- Ultra-Compact 6x6 mm PQFN, 72% Space-Saving Compared to Conventional Discrete Solutions
- Fully Optimized System Efficiency
-

Pin Configuration







Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CIN}	Supply Voltage	Referenced to CGND	-0.3	6.0	V
V_{DRV}	Drive Voltage	Referenced to CGND	-0.3	6.0	V
$V_{DISB\#}$	Output Disable	Referenced to CGND	-0.3	6.0	V
V_{PWM}	PWM Signal Input	Referenced to CGND	-0.3	6.0	V
$V_{SMOD\#}$	Skip Mode Input	Referenced to CGND	-0.3	6.0	V
V_{GL}	Low Gate Manufacturing Test Pin	Referenced to CGND	-0.3	6.0	V
$V_{THWN\#}$	Thermal Warning Flag	Referenced to CGND	-0.3	6.0	V
V_{IN}					

Electrical Characteristics

Typical values are V_{IN} = 12 V, V_{CIN} = 5 V, V_{DRV} = 5 V, and $T_A = T_J$ = +25°C unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Basic Operation						
I_Q	Quiescent Current	$I_Q=I_{VCIN}+I_{VDRV}$, PWM=LOW or HIGH or Float			2	mA
V_{UVLO}	UVLO Threshold	V_{CIN} Rising	2.9	3.1	3.3	V
V_{UVLO_Hys}	UVLO Hysteresis			0.4		V
PWM Input (V_{CIN} = V_{DRV} = 5 V ±10%)						
R_{UP_PWM}	Pull-Up Impedance	V_{PWM}=5 V		10		kΩ
R_{DN_PWM}	Pull-Down Impedance	V_{PWM}=0 V		10		kΩ
V_{IH_PWM}	PWM High Level Voltage		3.04	3.55	4.05	V
V_{TRI_HI}	3-State Upper Threshold		2.95	3.45	3.94	V
V_{TRI_LO}	3-State Lower Threshold		0.98	1.25	1.52	V
V_{IL_PWM}	PWM Low Level Voltage		0.84	1.15	1.42	V
$t_{D\_HOLD-OFF}$	3-State Shut-Off Time			160	200	ns
V_{HiZ_PWM}	3-State Open Voltage		2.20	2.50	2.80	V
$t_{PWM-OFF\_MIN}$	PWM Minimum Off Time		120			ns
PWM Input (V_{CIN} = V_{DRV} = 5 V ±5%)						
R_{UP_PWM}	Pull-Up Impedance	V_{PWM}=5 V		10		kΩ
R_{DN_PWM}	Pull-Down Impedance	V_{PWM}=0 V		10		kΩ
V_{IH_PWM}	PWM High Level Voltage		3.22	3.55	3.87	V
V_{TRI_HI}	3-State Upper Threshold		3.13	3.45	3.77	V
V_{TRI_LO}	3-State Lower Threshold		1.04	1.25	1.46	V
V_{IL_PWM}	PWM Low Level Voltage		0.90	1.15	1.36	V
$t_{D\_HOLD-OFF}$	3-State Shut-Off Time			160	200	ns

D_HOLD-OFF

Electrical Characteristics

Typical values are V_{IN} = 12 V, V_{CIN} = 5 V, V_{DRV} = 5 V, and $T_A = T_J$ = +25°C unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Thermal Warning Flag						
T_{ACT}	Activation Temperature			150		°C
T_{RST}	Reset Temperature			135		°C
R_{THWN}	Pull-Down Resistance	I_{PLD}=5 mA		30		Ω
250 ns Timeout Circuit						
$t_{D\_TIMEOUT}$	Timeout Delay	SW=0 V, Delay Between GH from HIGH to LOW and GL from LOW to HIGH		250		ns
High-Side Driver (f_{SW} = 1000 kHz, I_{OUT} = 30 A, T_A = +25°C)						
R_{SOURCE_GH}	Output Impedance, Sourcing	Source Current=100 mA		1		Ω
R_{SINK_GH}						

Typical Performance Characteristics

Test Conditions: V_{IN}=12 V, V_{OUT}=1 V, V_{CIN}=5 V, V_{DRV}=5 V, L_{OUT}=250 nH, T_A=25°C, and natural convection cooling, unless otherwise specified.

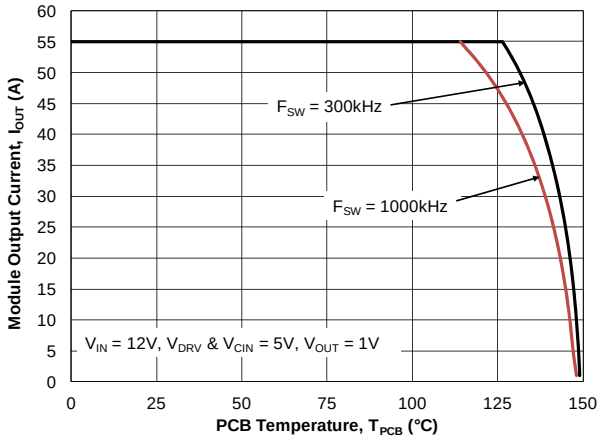


Figure 6. Safe Operating Area

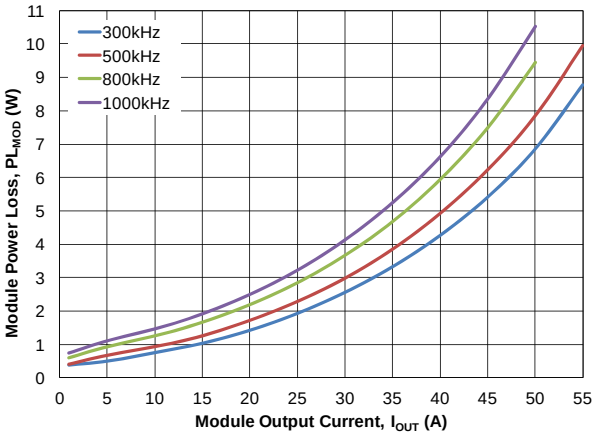


Figure 7. Power Loss vs. Output Current

Figure 8. Power Loss vs. Switching Frequency

Figure 9. Power Loss vs. Input Voltage

Figure 10. Power Loss vs. Driver Supply Voltage

Figure 11. Power Loss vs. Output Voltage

Typical Performance Characteristics

Test Conditions: V_{IN}=12 V, V_{OUT}=1 V, V_{CIN}=5 V, V_{DRV}=5 V, L_{OUT}=250 nH, T_A=25°C, and natural convection cooling, unless otherwise specified.

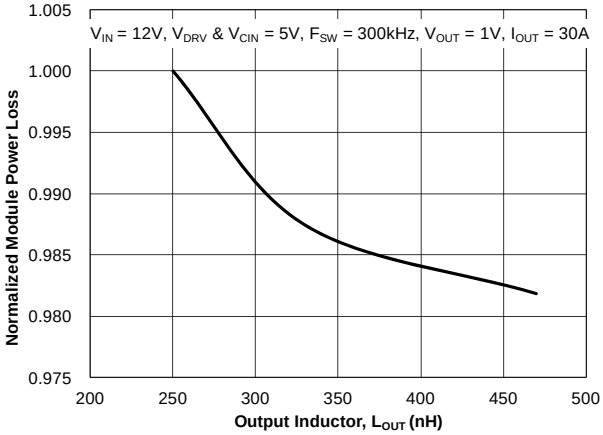


Figure 12. Power Loss vs. Output Inductor

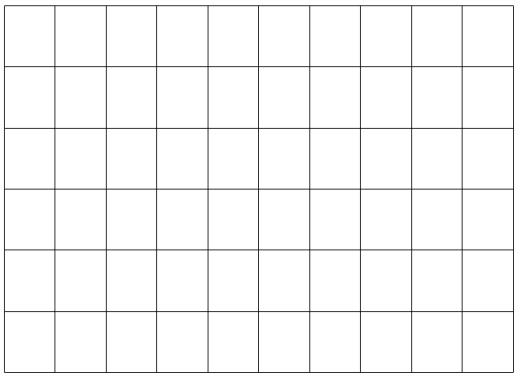


Figure 13. Driver Supply Current vs. Switching Frequency

Figure 14. Driver Supply Current vs. Driver Supply Voltage

Figure 15. Driver Supply Current vs. Output Current

Figure 16. UVLO Threshold vs. Temperature

Figure 17. PWM Threshold vs. Driver Supply Voltage

Typical Performance Characteristics

Test Conditions: V_{CIN}=5 V, V_{DRV}=5 V, T_A=25°C, and natural convection cooling, unless otherwise specified.

Figure 18. PWM Threshold vs. Temperature

Figure 19. SMOD# Threshold vs. Driver Supply Voltage

Figure 20. SMOD# Threshold vs. Temperature

Figure 21. SMOD# Pull-Up Current vs. Temperature

Figure 22. DISB# Threshold vs. Driver Supply Voltage

Figure 23. DISB# Threshold vs. Temperature

Typical Performance Characteristics

Test Conditions: V_{CIN}=5 V, V_{DRV}=5 V, T

Functional Description

The FDMF6823A is a driver-plus-FET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 1 MHz.

VCIN and Disable (DISB#)

The VCIN pin is monitored by an Under-Voltage Lockout (UVLO) circuit. When V_{CIN} rises above ~3.1 V, the driver is enabled. When V_{CIN} falls below ~2.7 V, the driver is disabled (GH, GL=0). The driver can also be disabled by pulling the DISB# pin LOW (DISB# < V_{IL_DISB}), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH (DISB# > V_{IH_DISB}).

Table 1. UVLO and Disable Logic

UVLO	DISB#	Driver State
0	X	Disabled (GH, GL=0)

Adaptive Gate Drive Circuit

The driver IC advanced design ensures minimum MOSFET dead-time, while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive adaptively to ensure they do not conduct simultaneously. Figure 27 provides the relevant timing waveforms. To prevent overlap during the LOW-to-HIGH switching transition (Q2 off to Q1 on), the adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes HIGH, Q2 begins to turn off after a propagation delay (t_{PD_PHGLL}

Application Information

Supply Capacitor Selection

For the supply inputs (V_{CIN}), a local ceramic bypass capacitor is recommended to reduce noise and to supply the peak current. Use at least a 1 µF X7R or X5R capacitor. Keep this capacitor close to the VCIN pin and connect it to the GND plane with vias.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}), as shown in Figure 30. A bootstrap capacitance of 100 nF X7R or X5R capacitor is usually adequate. A series bootstrap resistor may be needed for specific applications to improve switching noise immunity. The boot resistor may be required when operating above 15 V_{IN} and is effective at controlling the high-side MOSFET turn-on slew rate and V_{SHW} overshoot. R_{BOOT} values from 0.5 to 3.0 Ω are typically effective in reducing VSWH overshoot.

VCIN Filter

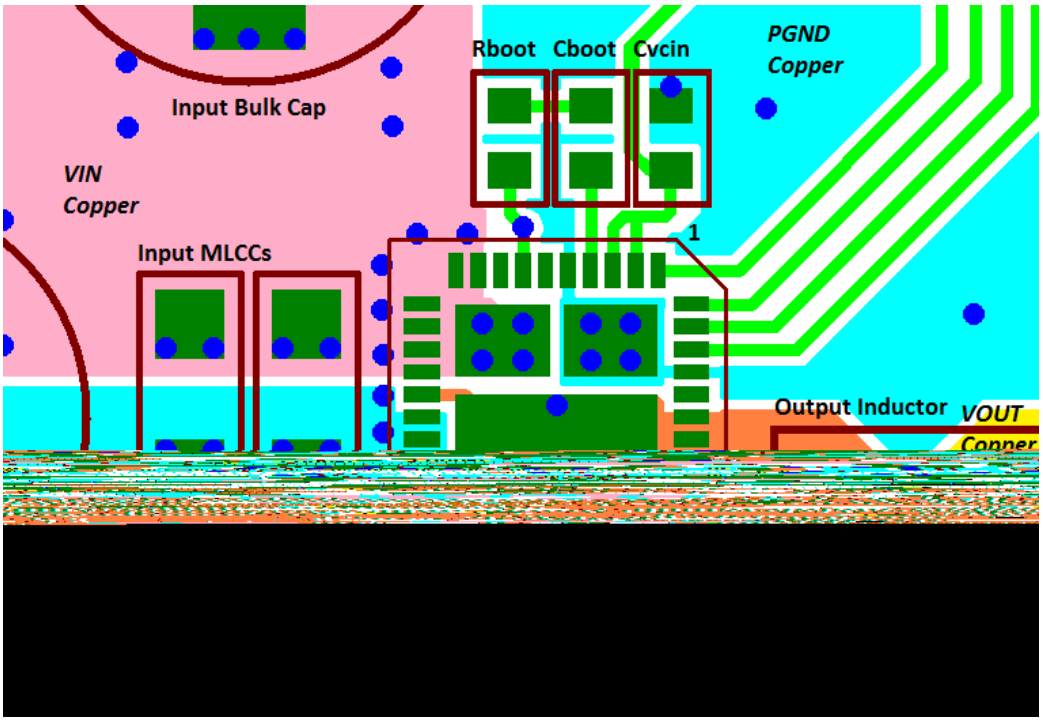


Figure 31. PCB Layout Example (Top View)

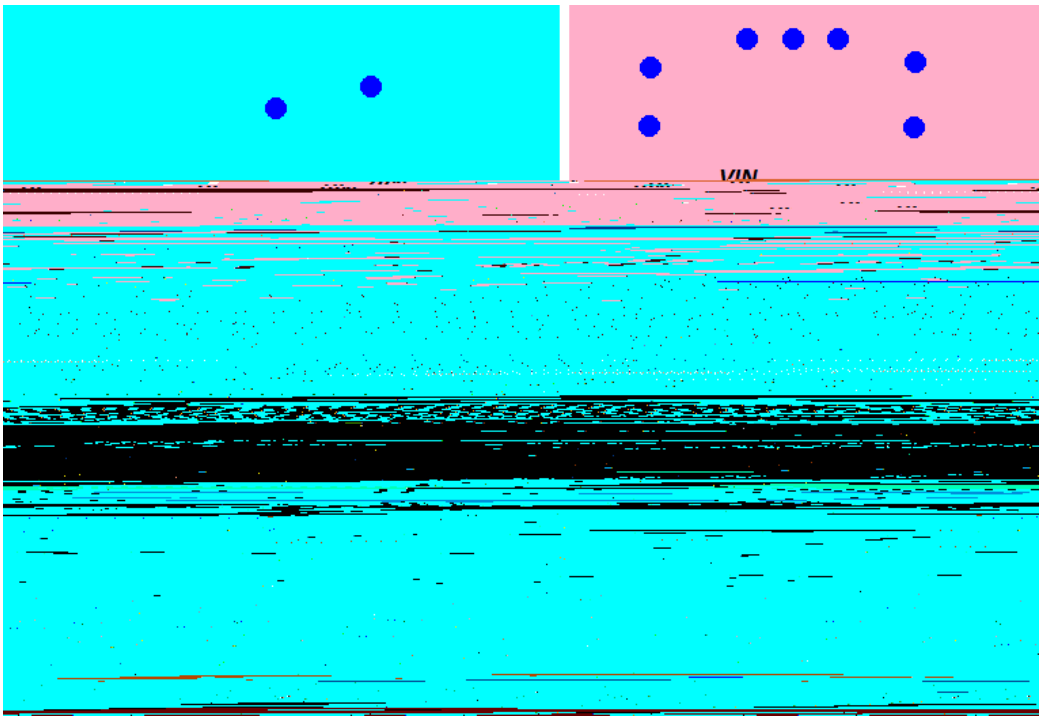
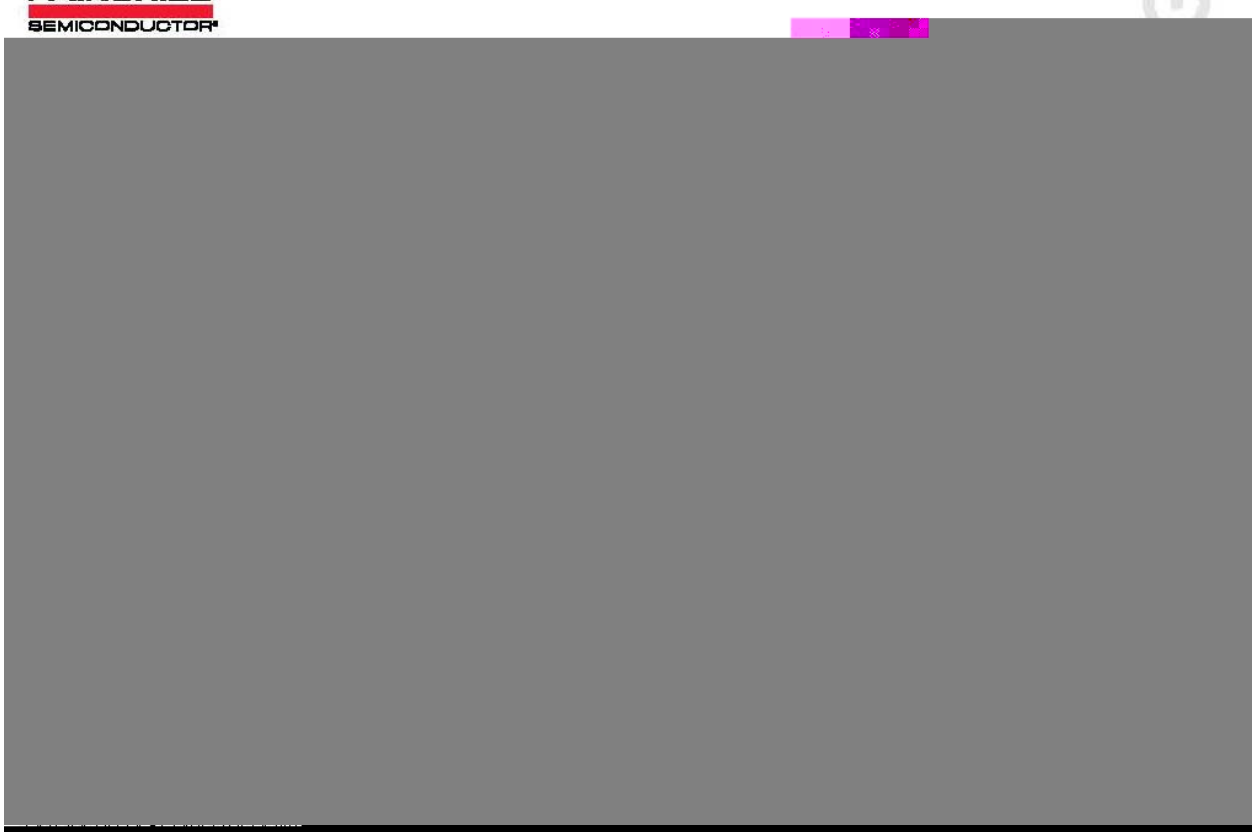


Figure 32. PCB Layout Example (Bottom View)



PUBLICATION ORDERING INFORMATION