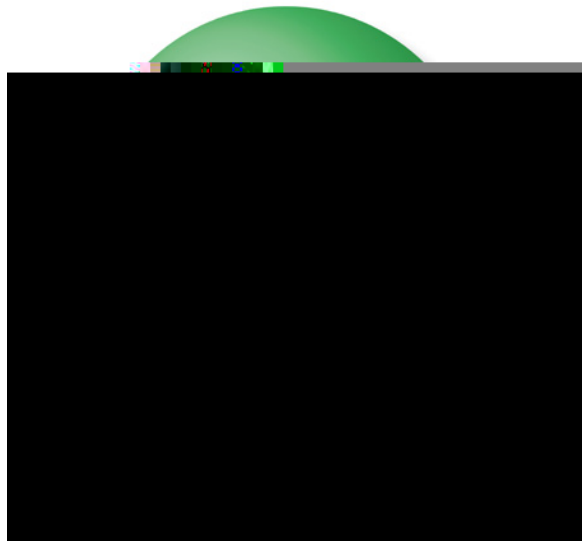




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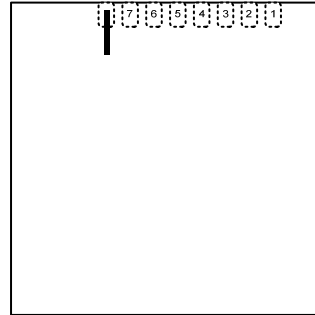
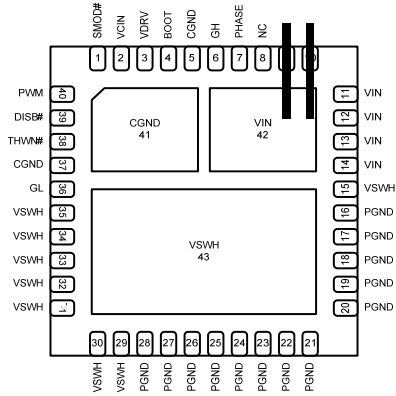
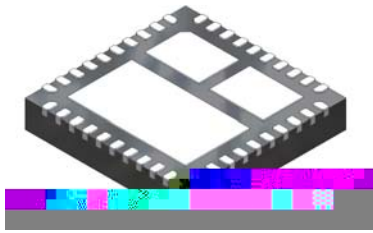
## **FDMF6823A — Extra-Small, High-Performance, High-Frequency DrMOS Module**

### **Benefits**

- Ultra-Compact 6x6 mm PQFN, 72% Space-Saving Compared to Conventional Discrete Solutions
- Fully Optimized System Efficiency
-



## Pin Configuration



## Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
$V_{CIN}$	Supply Voltage	Referenced to CGND	-0.3	6.0	V
$V_{DRV}$	Drive Voltage	Referenced to CGND	-0.3	6.0	V
$V_{DISB\#}$	Output Disable	Referenced to CGND	-0.3	6.0	V
$V_{PWM}$	PWM Signal Input	Referenced to CGND	-0.3	6.0	V
$V_{SMOD\#}$	Skip Mode Input	Referenced to CGND	-0.3	6.0	V
$V_{GL}$	Low Gate Manufacturing Test Pin	Referenced to CGND	-0.3	6.0	V
$V_{THWN\#}$	Thermal Warning Flag	Referenced to CGND	-0.3	6.0	V

$V_{IN}$

### Electrical Characteristics

Typical values are  $V_{IN} = 12\text{ V}$ ,  $V_{CIN} = 5\text{ V}$ ,  $V_{DRV} = 5\text{ V}$ , and  $T_A = T_J = +25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Basic Operation</b>						
$I_Q$	Quiescent Current	$I_Q = I_{VCIN} + I_{VDRV}$ , PWM=LOW or HIGH or Float			2	mA
$V_{UVLO}$	UVLO Threshold	$V_{CIN}$ Rising	2.9	3.1	3.3	V
$V_{UVLO\_Hys}$	UVLO Hysteresis			0.4		V
<b>PWM Input (<math>V_{CIN} = V_{DRV} = 5\text{ V} \pm 10\%</math>)</b>						
$R_{UP\_PWM}$	Pull-Up Impedance	$V_{PWM} = 5\text{ V}$		10		k
$R_{DN\_PWM}$	Pull-Down Impedance	$V_{PWM} = 0\text{ V}$		10		k
$V_{IH\_PWM}$	PWM High Level Voltage		3.04	3.55	4.05	V
$V_{TRI\_HI}$	3-State Upper Threshold		2.95	3.45	3.94	V
$V_{TRI\_LO}$	3-State Lower Threshold		0.98	1.25	1.52	V
$V_{IL\_PWM}$	PWM Low Level Voltage		0.84	1.15	1.42	V
$t_{D\_HOLD-OFF}$	3-State Shut-Off Time			160	200	ns
$V_{HIz\_PWM}$	3-State Open Voltage		2.20	2.50	2.80	V
$t_{PWM-OFF\_MIN}$	PWM Minimum Off Time		120			ns
<b>PWM Input (<math>V_{CIN} = V_{DRV} = 5\text{ V} \pm 5\%</math>)</b>						
$R_{UP\_PWM}$	Pull-Up Impedance	$V_{PWM} = 5\text{ V}$		10		k
$R_{DN\_PWM}$	Pull-Down Impedance	$V_{PWM} = 0\text{ V}$		10		k
$V_{IH\_PWM}$	PWM High Level Voltage		3.22	3.55	3.87	V
$V_{TRI\_HI}$	3-State Upper Threshold		3.13	3.45	3.77	V
$V_{TRI\_LO}$	3-State Lower Threshold		1.04	1.25	1.46	V
$V_{IL\_PWM}$	PWM Low Level Voltage		0.90	1.15	1.36	V
$t_{D\_HOLD-OFF}$	3-State Shut-Off Time			160	200	ns

### Electrical Characteristics

Typical values are  $V_{IN} = 12\text{ V}$ ,  $V_{CIN} = 5\text{ V}$ ,  $V_{DRV} = 5\text{ V}$ , and  $T_A = T_J = +25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Thermal Warning Flag</b>						
$T_{ACT}$	Activation Temperature			150		$^\circ\text{C}$
$T_{RST}$	Reset Temperature			135		$^\circ\text{C}$
$R_{THWN}$	Pull-Down Resistance	$I_{PLD}=5\text{ mA}$		30		
<b>250 ns Timeout Circuit</b>						
$t_{D\_TIMEOUT}$	Timeout Delay	SW=0 V, Delay Between GH from HIGH to LOW and GL from LOW to HIGH		250		ns
<b>High-Side Driver (<math>f_{sw} = 1000\text{ kHz}</math>, <math>I_{OUT} = 30\text{ A}</math>, <math>T_A = +25^\circ\text{C}</math>)</b>						
$R_{SOURCE\_GH}$ $R_{SINK\_GH}$	Output Impedance, Sourcing	Source Current=100 mA		1		





## Typical Performance Characteristics

Test Conditions:  $V_{IN}=12\text{ V}$ ,  $V_{OUT}=1\text{ V}$ ,  $V_{CIN}=5\text{ V}$ ,  $V_{DRV}=5\text{ V}$ ,  $L_{OUT}=250\text{ nH}$ ,  $T_A=25^\circ\text{C}$ , and natural convection cooling, unless otherwise specified.

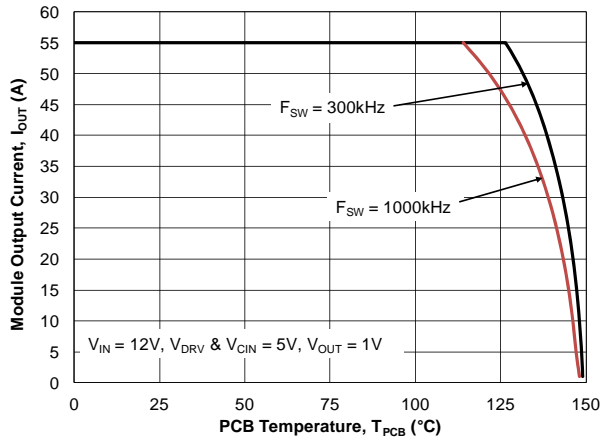


Figure 6. Safe Operating Area

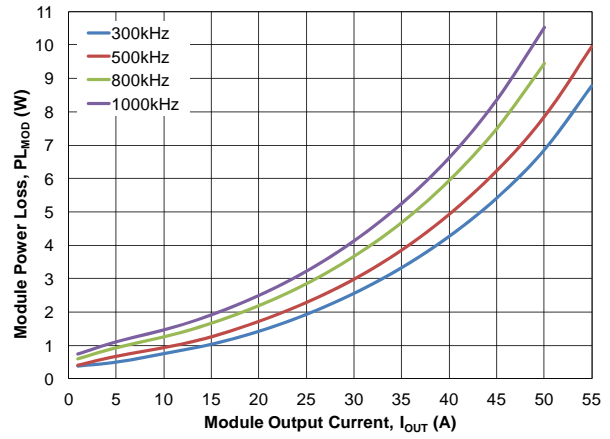


Figure 7. Power Loss vs. Output Current

Figure 8. Power Loss vs. Switching Frequency

Figure 9. Power Loss vs. Input Voltage

Figure 10. Power Loss vs. Driver Supply Voltage

Figure 11. Power Loss vs. Output Voltage

## Typical Performance Characteristics

Test Conditions:  $V_{IN}=12\text{ V}$ ,  $V_{OUT}=1\text{ V}$ ,  $V_{CIN}=5\text{ V}$ ,  $V_{DRV}=5\text{ V}$ ,  $L_{OUT}=250\text{ nH}$ ,  $T_A=25^\circ\text{C}$ , and natural convection cooling, unless otherwise specified.

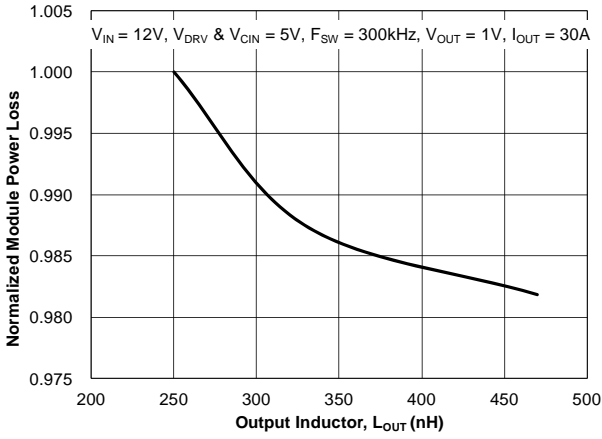


Figure 12. Power Loss vs. Output Inductor

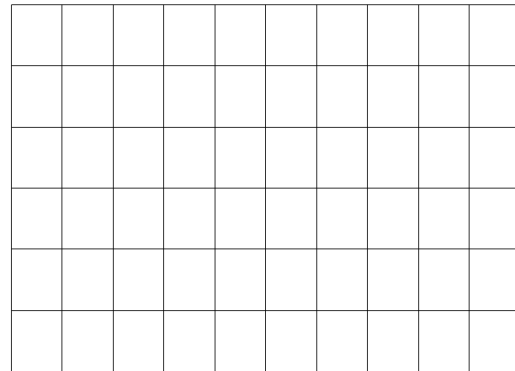


Figure 13. Driver Supply Current vs. Switching Frequency

Figure 14. Driver Supply Current vs. Driver Supply Voltage

Figure 15. Driver Supply Current vs. Output Current

Figure 16. UVLO Threshold vs. Temperature

Figure 17. PWM Threshold vs. Driver Supply Voltage

## Typical Performance Characteristics

Test Conditions:  $V_{CIN}=5\text{ V}$ ,  $V_{DRV}=5\text{ V}$ ,  $T_A=25^\circ\text{C}$ , and natural convection cooling, unless otherwise specified.

Figure 18. PWM Threshold vs. Temperature

Figure 19. SMOD# Threshold vs. Driver Supply Voltage

Figure 20. SMOD# Threshold vs. Temperature

Figure 21. SMOD# Pull-Up Current vs. Temperature

Figure 22. DISB# Threshold vs. Driver Supply Voltage

Figure 23. DISB# Threshold vs. Temperature

## Typical Performance Characteristics

Test Conditions:  $V_{CIN}=5\text{ V}$ ,  $V_{DRV}=5\text{ V}$ , T

## Functional Description

The FDMF6823A is a driver-plus-FET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 1 MHz.

### VCIN and Disable (DISB#)

The VCIN pin is monitored by an Under-Voltage Lockout (UVLO) circuit. When  $V_{CIN}$  rises above  $\sim 3.1$  V, the driver is enabled. When  $V_{CIN}$  falls below  $\sim 2.7$  V, the driver is disabled (GH, GL=0). The driver can also be disabled by pulling the DISB# pin LOW ( $DISB\# < V_{IL\_DISB}$ ), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH ( $DISB\# > V_{IH\_DISB}$ ).

**Table 1. UVLO and Disable Logic**

UVLO	DISB#	Driver State
0	X	Disabled (GH, GL=0)

### Adaptive Gate Drive Circuit

The driver IC advanced design ensures minimum MOSFET dead-time, while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive adaptively to ensure they do not conduct simultaneously. Figure 27 provides the relevant timing waveforms. To prevent overlap during the LOW-to-HIGH switching transition (Q2 off to Q1 on), the adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes

HIGH, Q2 begins to turn off after a propagation delay ( $t_{PD\_PHGLL}$ )



## Application Information

### Supply Capacitor Selection

For the supply inputs ( $V_{CIN}$ ), a local ceramic bypass capacitor is recommended to reduce noise and to supply the peak current. Use at least a 1  $\mu$ F X7R or X5R capacitor. Keep this capacitor close to the VCIN pin and connect it to the GND plane with vias.

### Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor ( $C_{BOOT}$ ), as shown in Figure 30. A bootstrap capacitance of 100 nF X7R or X5R capacitor is usually adequate. A series bootstrap resistor may be needed for specific applications to improve switching noise immunity. The boot resistor may be required when operating above 15  $V_{IN}$  and is effective at controlling the high-side MOSFET turn-on slew rate and  $V_{SHW}$  overshoot.  $R_{BOOT}$  values from 0.5 to 3.0  $\Omega$  are typically effective in reducing  $V_{SWH}$  overshoot.

### VCIN Filter





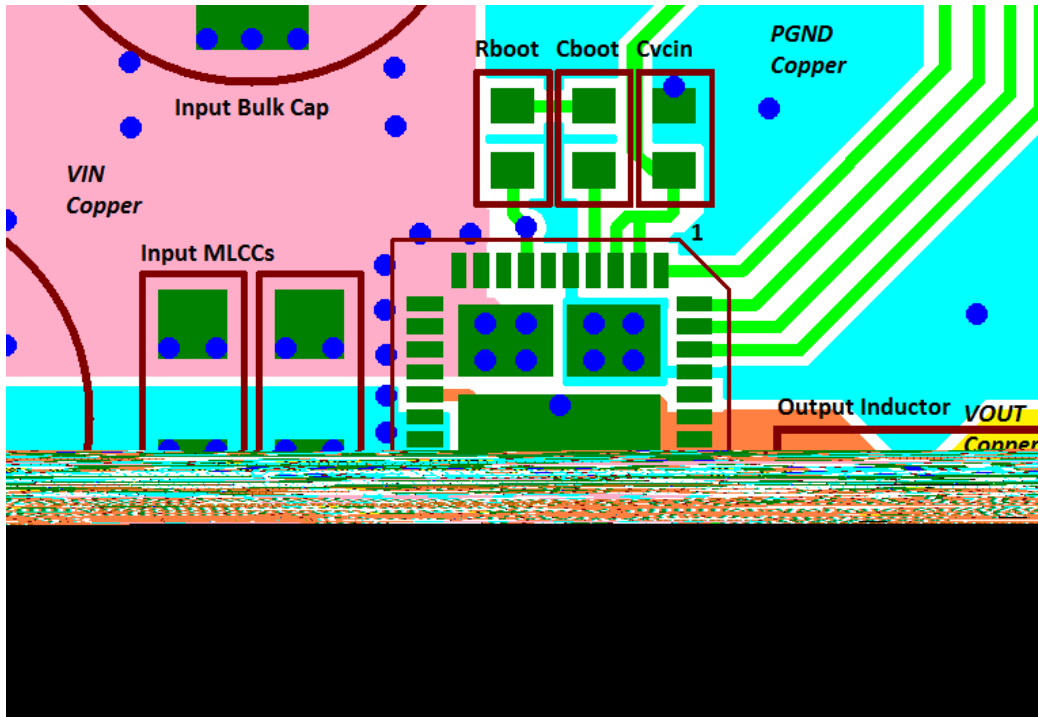


Figure 31. PCB Layout Example (Top View)

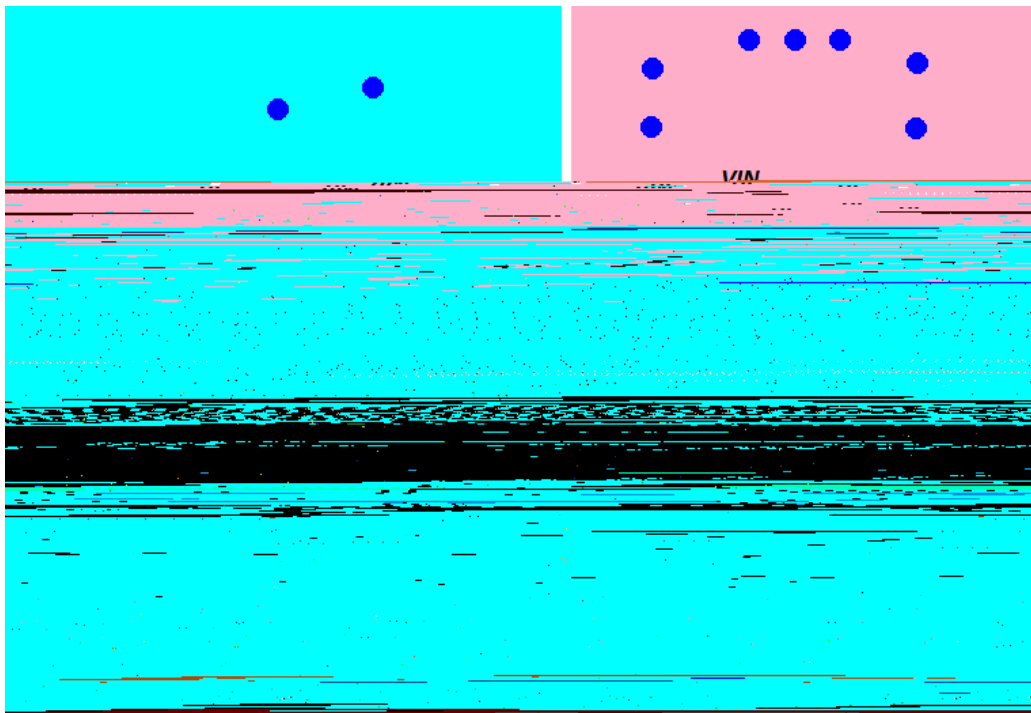
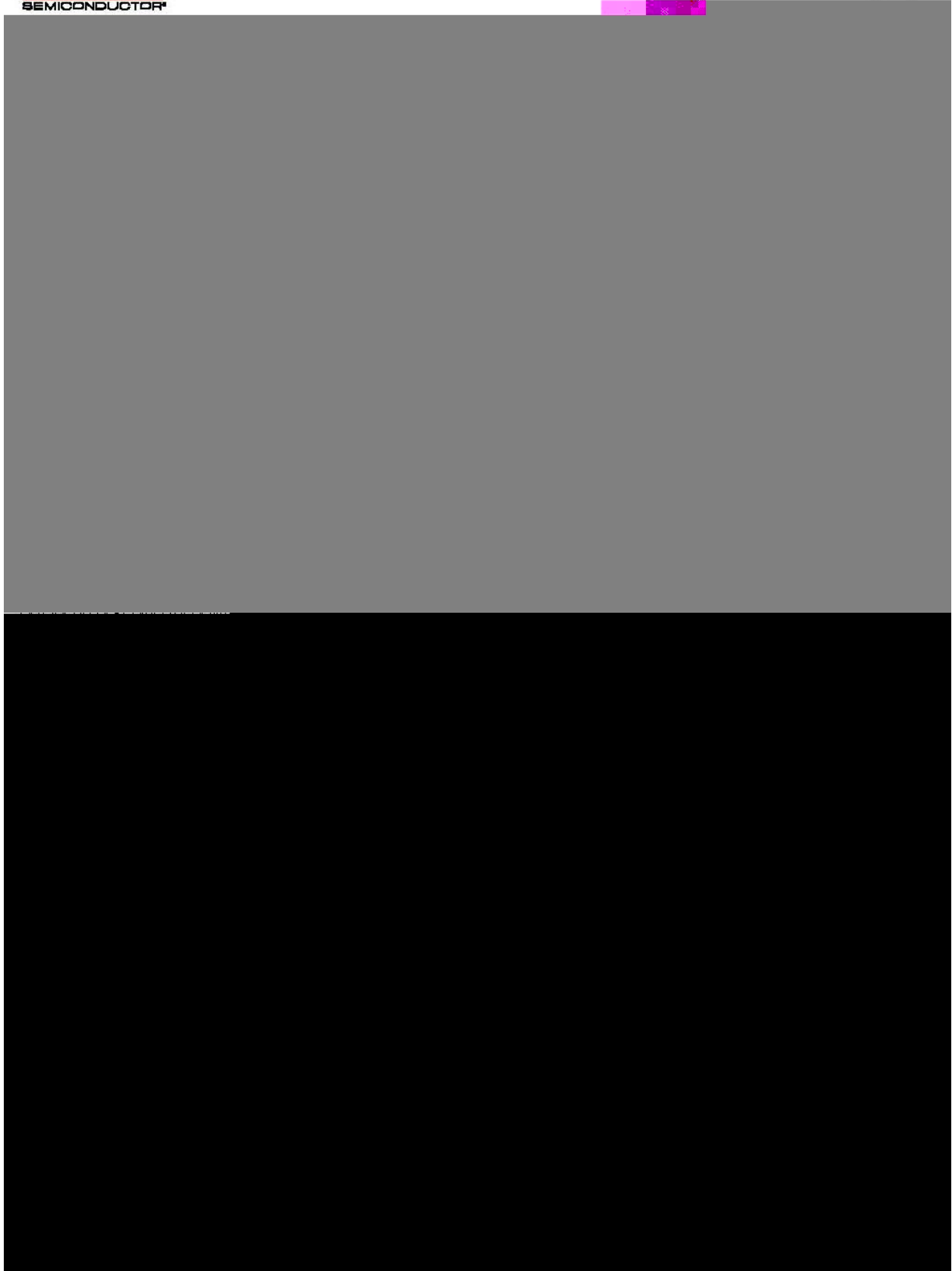


Figure 32. PCB Layout Example (Bottom View)





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