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FIN1022 2 X 2 LVDS High Speed Crosspoint Switch

FIN1022 2 X 2 LVDS High Speed Crosspoint Switch

General Description

This non-blocking 2x2 crosspoint switch has a fully differential input to output data path for low noise generation and low pulse width distortion. The device can be used as a

1 data pattern at 800 Mbps

- Rail-to-rail common mode range is 0.5V to 3.25V
- \blacksquare Worst case power dissipation is less than 126 mW
- Open-circuit fail safe protection
- Fast switch time of 1.1 ns typical
- 35 ps typical pin channel to channel skew
- 3.3V power supply operation
- Non-blocking switch
- LVDS receiver inputs accept LVPECL signals directly
- 7.5 kV HBM ESD protection
- 16-lead SOIC package and TSSOP package
- Inter-operates with TIA/EIA 644-1995 specification
- See the Fairchild Interface Solutions web page for cross reference information: www.fairchildsemi.com/products/interface/lvds.html

Ordering Code:

| Order Number | Package Number | Package Description | | | | |
|--|----------------|--|--|--|--|--|
| FIN1022M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow | | | | |
| FIN1022MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide | | | | |
| Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code | | | | | | |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code

Logic Symbol



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FIN1022

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

| Symbol | Paramotor | Test Conditions | Min | Тур | Max | Unite |
|-------------------|---|---------------------------------------|-----|----------|-------|-------|
| | Falanetei | | | (Note 4) | Units | |
| t _{PLHD} | Differential Output Propagation Delay | 0.7 | | 1.6 | | |
| | LOW-to-HIGH | $R_L = 75 \ \Omega, \ C_L = 5 \ pF$, | 1.0 | 1.2 | 1.3 | nS |
| t _{PHLD} | Differential Output Propagation Delay | $V_{CC} = 3.3V$, $T_A = 25^{\circ}C$ | 0.7 | | 1.6 | ns |
| | HIGH-to-LOW | See Figure 4 and Figure 5 | 1.0 | 1.2 | 1.3 | |
| t _{TLHD} | Differential Output Rise Time (20% to 80%) | 290 | | 580 | ps | |
| t _{THLD} | Differential Output Fall Time (80% to 20%) | | | | 580 | ps |
| t _{PLH} | Selection Propagation Delay | 0.6 | | 1.5 | | |
| | LOW-to-HIGH (SEL _n to OUT _n) | $R_L = 75 \ \Omega, \ C_L = 5 \ pF$, | 0.9 | 1.1 | 1.2 | ns |
| t _{PHL} | Selection Propagation Delay | $V_{CC} = 3.3V$, $T_A = 25^{\circ}C$ | 0.6 | | 1.5 | |
| | HIGH-to-LOW (SEL _n to OUT _n) | See Figure 6 and Figure 7 | 0.9 | 1.1 | 1.2 | ns |
| t _{ZHD} | | | | | | |

Note 4: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

Note 5: Part-to-part skew is the maximum delay time difference on like edges (LOW-to-HIGH or HIGH-to-LOW) for the same V_{CC} and temperature conditions.

Required Specifications

- 1. When the true and complement LVDS outputs (having a 75 Ω connected between outputs) are connected to 3.75 k Ω resistors and the common point of those 3.75 k Ω resistors are connected to a voltage source that sweeps from 0 to 2.4V, the DC V_{OD} and Δ V_{OD} are still maintained (see Figure 1).
- 2. When the true and complement LVDS outputs (having a 5 pF capacitor attached between outputs) are connected with 37.5 Ω resistors each to common point, then the common point does not vary by more than 150 mV under all process, temperature and voltage conditions when the outputs switch either from LOW-to-HIGH or from HIGH-to-LOW (see Figure 2).

FIN1022



Required Specifications (Continued)



FIGURE 3. LVDS Driver DC Test Circuit



Note A: All input pulses have frequency = 50 MHz, t_R or t_F = 500 ps Note B: C_L includes all probe and jig capacitances

FIGURE 4. LVDS Input to LVDS Driver Propagation Delay and Transition Time Circuit



FIGURE 5. LVDS Input to LVDS Output AC Waveforms



FIGURE 6. LVTTL Input to LVDS Driver Propagation Delay and Transition Time Test Circuit



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