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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

August 2001
Revised December 2001

FIN1032

3FIN1032 Fl12a3 Tw chLN100031 T(Hi)8rrogy. The receiver translates LVDS ferential input threshold of 100mV, to LVTTL signal leve th Greater than 40

- 3.3V power supply operation
- 0.4ns maximum differential pulse skew
- 2.5ns maximum propagation delay
- Low power dissipation
- Power OFF protection

Ordering Code:

- 16-Lead SOIC and TSSOP packages save space

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +4.6 V
DC Input Voltage (V_{IN})	−0.5V to +4.6 V
DC Input Voltage (V_{OUT})	−0.5V to 6 V
DC Output Current (I_O)	16 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
ESD (Human Body Model)	≥ 10,000 V
ESD (Machine Model)	≥ 500 V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0 V to 3.6 V
Magnitude of Differential Voltage ($\|V_{ID}\|$)	100 mV to V_{CC}
Common-Mode Input Voltage (V_{IC})	0.05 V to 2.35V
Input Voltage (V_{IN})	0 to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
V_{TH}	Differential Input Threshold HIGH	See Figure 1 and Table 1			100	mV
V_{TL}	Differential Input Threshold LOW	See Figure 1 and Table 1	−100			mV
I_{IN}	Input Current	V_{IN} = 0V or V_{CC}			±20	µA
$I_{I(OFF)}$	Power-OFF Input Current	V_{CC} = 0V, V_{IN} = 0V or 3.6V			±20	µA
V_{IH}	Input High Voltage (EN or $\overline{EN}$)		2.0		V_{CC}	V
V_{IL}	Input Low Voltage (EN or $\overline{EN}$)		GND		0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = −100 µA	V_{CC} −0.2			V
		I_{OH} = −8 mA	2.4			
V_{OL}	Output LOW Voltage	I_{OH} = 100 µA			0.2	V
		I_{OL} = 8 mA			0.5	
V_{IK}	Input Clamp Voltage	I_{IK} = −18 mA	−1.5			V
I_{OZ}	Disabled Output Leakage Current	EN = 0.8 and $\overline{EN}$ = 2V, V_{OUT} = 3.6V or 0V			±20	µA
I_{OS}	Output Short Circuit Test	Receiver Enabled, V_{OUT} = 0V (one output shorted at a time)	−15		−100	mA
I_{CCZ}	Disabled Power Supply Current	Receiver Disabled			5	mA
I_{CC}	Power Supply Current	Receiver Enabled, (R_{IN+} = 1V and R_{IN-} = 1.4V) or (R_{IN+} = 1.4V and R_{IN-} = 1V)			15	mA
$I_{PU/PD}$	Output Power Up/Power Down	V_{CC} = 0V to 1.5V			±20	µA

Note 2: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

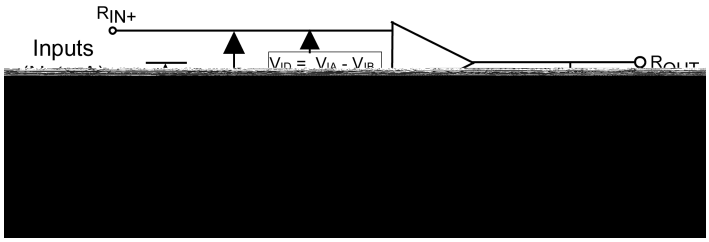
Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
t_{PLH}	Propagation Delay LOW-to-HIGH	$\|V_{ID}\|$ = 400 mV, C_L = 10 pF, R_L = 1kΩ See Figure 1 and Figure 2	1.0		2.5	ns
t_{PHL}	Propagation Delay HIGH-to-LOW		1.0		2.5	ns
t_{TLH}	Output Rise Time (20% to 80%)			0.7	1.2	ns
t_{THL}	Output Fall Time (80% to 20%)			0.7	1.2	ns
$t_{SK(P)}$	Pulse Skew $\|t_{PLH} - t_{PHL}\|$				0.4	ns
$t_{SK(LH)}$ $t_{SK(HL)}$	Channel-to-Channel Skew (Note 4)				0.3	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 5)				1.0	ns
f_{MAX}	Maximum Operating Frequency (Note 6)	R_L = 1kΩ, C_L = 10 pF, see Figure 1 and Figure 2	200	325		MHz
t_{ZH}	LVTTL Output Enable Time from Z to HIGH	R_L = 1kΩ, C_L = 10 pF, See Figure 3 and Figure 4			5.0	ns
t_{ZL}	LVTTL Output Enable Time from Z to LOW				5.0	ns
t_{HZ}	LVTTL Output Disable Time from HIGH to Z				5.0	ns
t_{LZ}	LVTTL Output Disable Time from LOW to Z				5.0	ns

Note 3: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

Note 4: $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

Note 5: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

Note 6: f_{MAX} Criteria: Input t_R = t_F < 1 ns, V_{ID} = 300 mV, (1.05V to 1.35V pp), 50% duty cycle; Output duty cycle 40% to 60%, V_{OL} < 0.5V, V_{OH} > 2.4V. All channels switching in phase.



Note A: All input pulses have frequency = 10MHz, t_R or t_F = 1ns

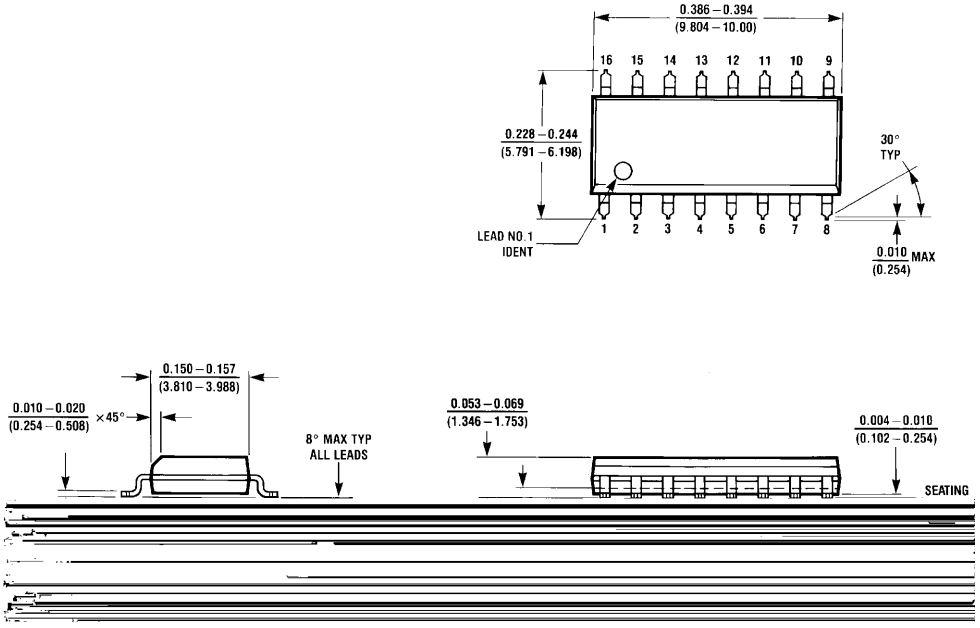
Note B: C_L includes all probe and jig capacitances

FIGURE 1. Differential Receiver Voltage Definitions and Propagation Delay and Transition Time Test Circuit

TABLE 1. Receiver Minimum and Maximum Input Threshold Test Voltages

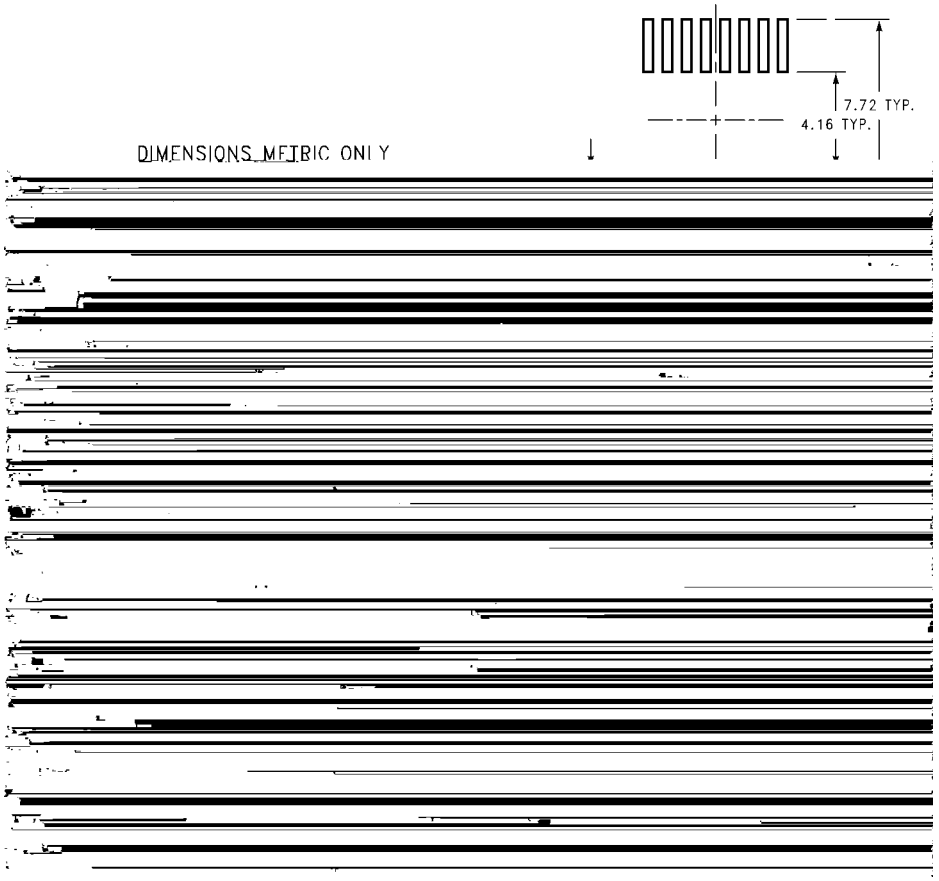
Applied Voltages (V)		Resulting Differential Input Voltage (mA)	Resulting Common Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	−100	1.2
2.4	2.3	100	2.35
2.3	2.4	−100	2.35
0.1	0	100	0.05
0	0.1	−100	0.05
1.5	0.9	600	1.2
0.9	1.5	−600	1.2
2.4	1.8	600	2.1
1.8	2.4	−600	2.1
0.6	0	600	0.3
0	0.6	−600	0.3

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

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