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# FIN1048

## 3.3V LVDS 4-Bit Flow-Through High Speed Differential Receiver

### General Description

This quad receiver is designed for high speed interconnect utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100mV, to LVTTTL signal levels. LVDS provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FIN1048 can be paired with its companion driver, the FIN1047, or any other LVDS driver.

### Features

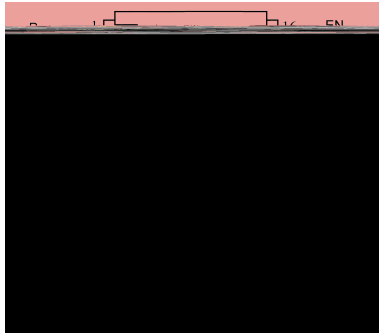
- Greater than 400Mbps data rate
- Flow-through pinout si/5 Meets or exceeds the TIA/EIA-644 LVDS standard
- Pin compatible with equivalent RS-422 and LVPECL devices
- 16-Lead SOIC and TSSOP packages save space

### Ordering Code:

Order Number	Package Number	Package Description
FIN1048M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FIN1048MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



### Pin Descriptions

Pin Name	Description
ROUT1, ROUT2, ROUT3, ROUT4	LVTTTL Data Outputs
RIN1+, RIN2+, RIN3+, RIN4+	Non-Inverting LVDS Inputs
RIN1-, RIN2-, RIN3-, RIN4-	Inverting LVDS Inputs
EN	Driver Enable Pin
$\overline{\text{EN}}$	Inverting Driver Enable Pin
V <sub>CC</sub>	Power Supply
GND	Ground

### Function Table

Inputs				Outputs
EN	$\overline{\text{EN}}$	R <sub>IN+</sub>	R <sub>OUT-</sub>	R <sub>OUT</sub>
H	L or Open	H	L	H
H	L or Open	L	H	L
H	L or Open	Fail Safe Condition		H
X	H	X	X	Z
L or Open	X	X	X	Z

H = HIGH Logic Level    L = LOW Logic Level    X = Don't Care  
Z = High Impedance    Fail Safe = Open, Shorted, Terminated

FIN1048 3.3V LVDS 4-Bit Flow-Through High Speed Differential Receiver

**Absolute Maximum Ratings**(Note 1)

**Recommended Operating Conditions**

**Note 1:** The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild

## AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

**Note 3:** All typical values are at  $T_A = 25^\circ\text{C}$  and with  $V_{CC} = 3.3\text{V}$ .

**Note 4:**  $t_{SK(LH)}$ ,  $t_{SK(HL)}$  is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same d



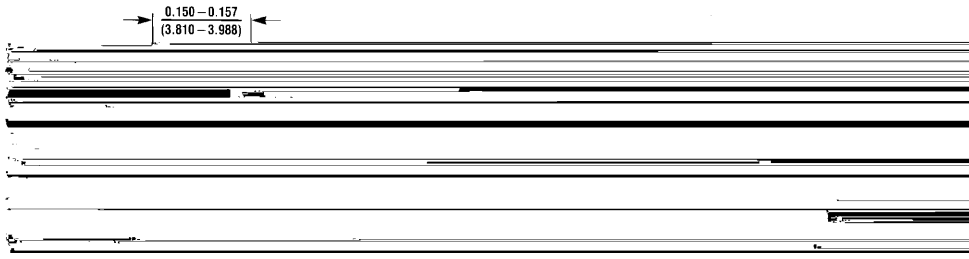
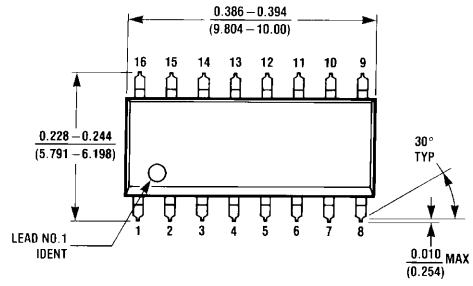
FIGURE 2. LVDS Input to LVTTTL Output AC Waveforms

Test Circuit for LVTTTL Outputs

Voltage Waveforms Enable and Disable Times

FIGURE 3. LVTTTL Outputs Test Circuit and AC Waveforms

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16

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