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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

September 2001
Revised August 2003

FIN1048
3.3V LVDS 4-Bit Flow-Through High Speed Differential Receiver

General Description

This quad receiver is designed for high speed interconnect utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100mV, to LVTTL signal levels. LVDS provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FIN1048 can be paired with its companion driver, the FIN1047, or any other LVDS driver.

Features

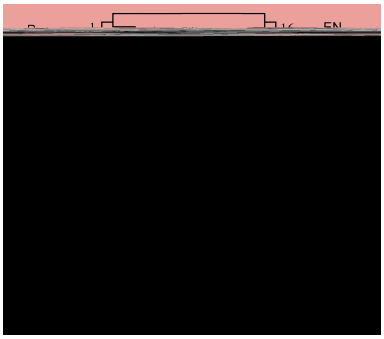
- Greater than 400Mbs data rate
- Flow-through pinout si/5 Meets or exceeds the TIA/EIA-644 LVDS standard
- Pin compatible with equivalent RS-422 and LVPECL devices
- 16-Lead SOIC and TSSOP packages save space

Ordering Code:

Order Number	Package Number	Package Description
FIN1048M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FIN1048MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Name	Description
R_{OUT1}, R_{OUT2}, R_{OUT3}, R_{OUT4}	LVTTL Data Outputs
R_{IN1+}, R_{IN2+}, R_{IN3+}, R_{IN4+}	Non-Inverting LVDS Inputs
R_{IN1-}, R_{IN2-}, R_{IN3-}, R_{IN4-}	Inverting LVDS Inputs
EN	Driver Enable Pin
$\overline{EN}$	Inverting Driver Enable Pin
V_{CC}	Power Supply
GND	Ground

Function Table

Inputs				Outputs
EN	$\overline{EN}$	R_{IN+}	R_{OUT-}	R_{OUT}
H	L or Open	H	L	H
H	L or Open	L	H	L
H	L or Open	Fail Safe Condition		H
X	H	X	X	Z
L or Open	X	X	X	Z

H = HIGH Logic Level L = LOW Logic Level X = Don't Care
Z = High Impedance Fail Safe = Open, Shorted, Terminated

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

Note 1: The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Note 3: All typical values are at $T_A = 25°C$ and with $V_{CC} = 3.3V$.

Note 4: $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same d

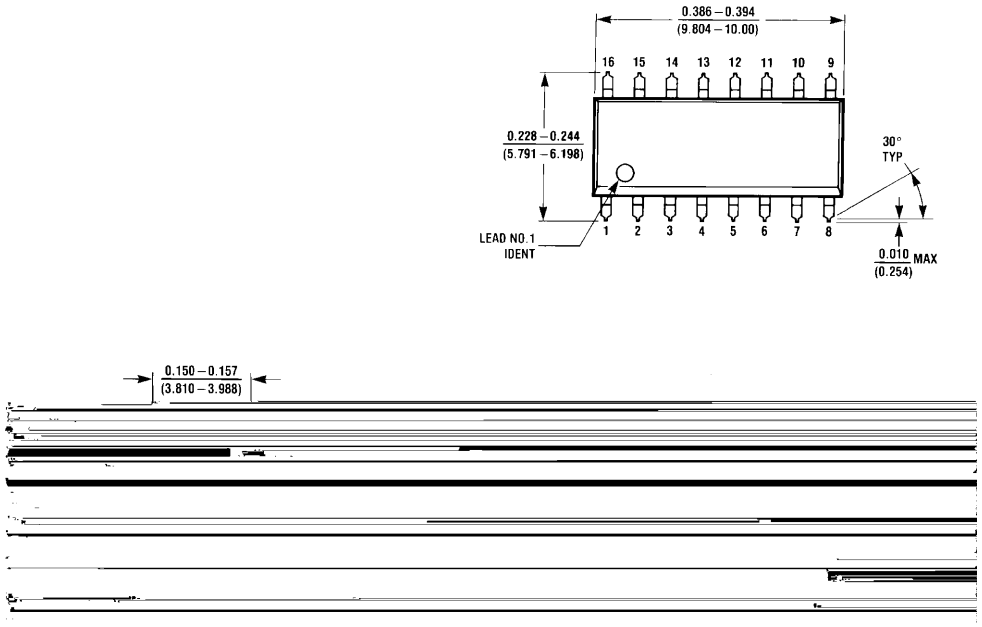
FIGURE 2. LVDS Input to LVTTL Output AC Waveforms

Test Circuit for LVTTL Outputs

Voltage Waveforms Enable and Disable Times

FIGURE 3. LVTTL Outputs Test Circuit and AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16