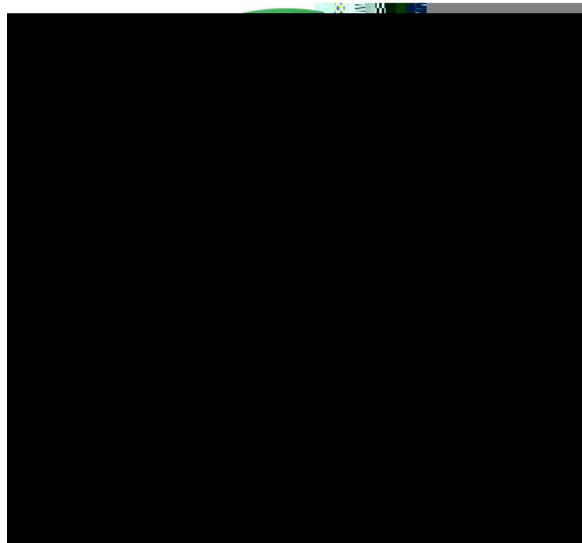




Is Now Part of



To learn more about ON Semiconductor, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (\_), the underscore (\_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (\_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at [www.onsemi.com](http://www.onsemi.com). Please email any questions regarding the system integration to [Fairchild\\_questions@onsemi.com](mailto:Fairchild_questions@onsemi.com).

---

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC. ON Semiconductor makes no warranty, representation or guarantee regarding the

arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be verified by independent technical experts. ON Semiconductor does not



# **FIN3385 / FIN3386**

## **Low-Voltage, 28-Bit, Flat-Panel Display Link Serializer / Deserializer**

### **Features**

- Operation -40°C to +85°C
- Low Power Consumption
- 20MHz to 85MHz Shift Clock Support
- ±1V Common-Mode Range around 1.2V
- Narrow Bus Reduces Cable Size and Cost

**FIN3385 / FIN3386 — Low-Voltage, 28-Bit Flat Panel Display Link Serializer / Deserializer**



## Transmitter Pin Configuration

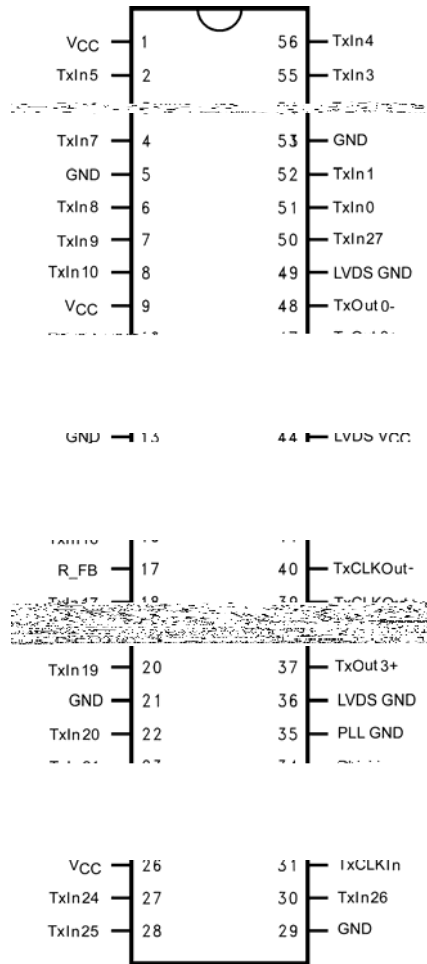


Figure 3. FIN3385 (28:4 Transmitter) Pin Assignments

### Pin Definitions

Pin Names	I/O Types	Number of Pins	Description of Signals
TxIn	I	28/21	LVTTTL Level Input
TxCLKIn	I	1	LVTTTL Level Clock Input, the rising edge is for data strobe
TxOut+	O	4/3	Positive LVDS Differential Data Output
TxOut-	O	4/3	Negative LVDS Differential Data Output
TxCLKOut+	O	1	Positive LVDS Differential Clock Output
TxCLKOut-	O	1	Negative LVDS Differential Clock Output
R_FB	I	1	Rising Edge Data Strobe: Assert HIGH ( $V_{CC}$ ) Falling Edge Data Strobe: Assert LOW (Ground)
/PwrDn	I	1	LVTTTL Level Power-Down Input Assertion (LOW) puts the outputs in High-Impedance state
PLL $V_{CC}$	I	1	Power Supply Pin for PLL
PLL GND	I	2	Ground Pins for PLL
LVDS $V_{CC}$	I	1	Power Supply Pin for LVDS Output
LVDS GND	I	3	Ground Pins for LVDS Output
$V_{CC}$	I	3	Power Supply Pins for LVTTTL Input
GND	I	5	Ground Pin for LVTTTL Input

## Receiver Pin Configuration

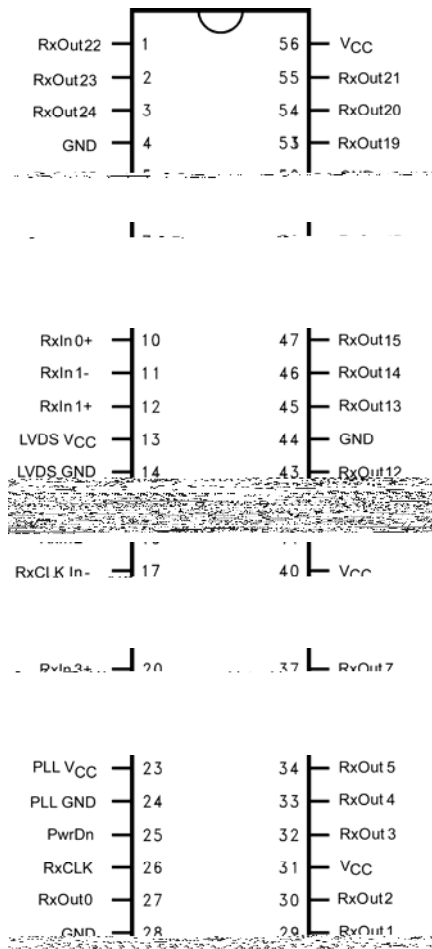


Figure 4. FIN3386 (28:4 Receiver) Pin Assignments

### Pin Definitions

Pin Names	I/O Types	Number of Pins	Description of Signals
RxIn	I	4/3	Negative LVDS Differential Data Output
RxIn+	I	4/3	Positive LVDS Differential Data Output
RxCLKIn-	I	1	Negative LVDS Differential Data Input
RxCLKIn+	I	1	Positive LVDS Differential Clock Input
RxOut	O	28/21	LVTTTL Level Data Output, goes HIGH for /PwrDn LOW
RxCLKOut-	O	1	LVTTTL Clock Output
/PwrDn	I	1	LVTTTL Level Input. Refer to Table 2
PLL V <sub>CC</sub>	I	1	Power Supply Pin for PLL
PLL GND	I	2	Ground Pins for PLL
LVDS V <sub>CC</sub>			

## Truth Tables

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Power Supply Voltage	-0.3	+4.6	V
$V_{ID\_TTL}$	TTL/CMOS Input/Output Voltage	-0.5	+4.6	V
$V_{IO\_LVDS}$	LVDS Input/Output Voltage	-0.3	+4.6	V
$I_{OSD}$	LVDS Output Short-Circuit Current	Continuous		
$T_{STG}$	Storage Temperature Range	-65	+150	°C
$T_J$	Maximum Junction Temperature		+150	°C
$T_L$	Lead Temperature, Soldering, 4 Seconds		+260	°C
ESD	Human Body Model, JESD22-A114 (1.5k $\Omega$ , 100pF)	I/O to GND	>10.0	kV
		All Pins	>6.5	
	Machine Model, JESD22-A115 (0 $\Omega$ , 200pF)		>400	V

**Note:**

- Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$				

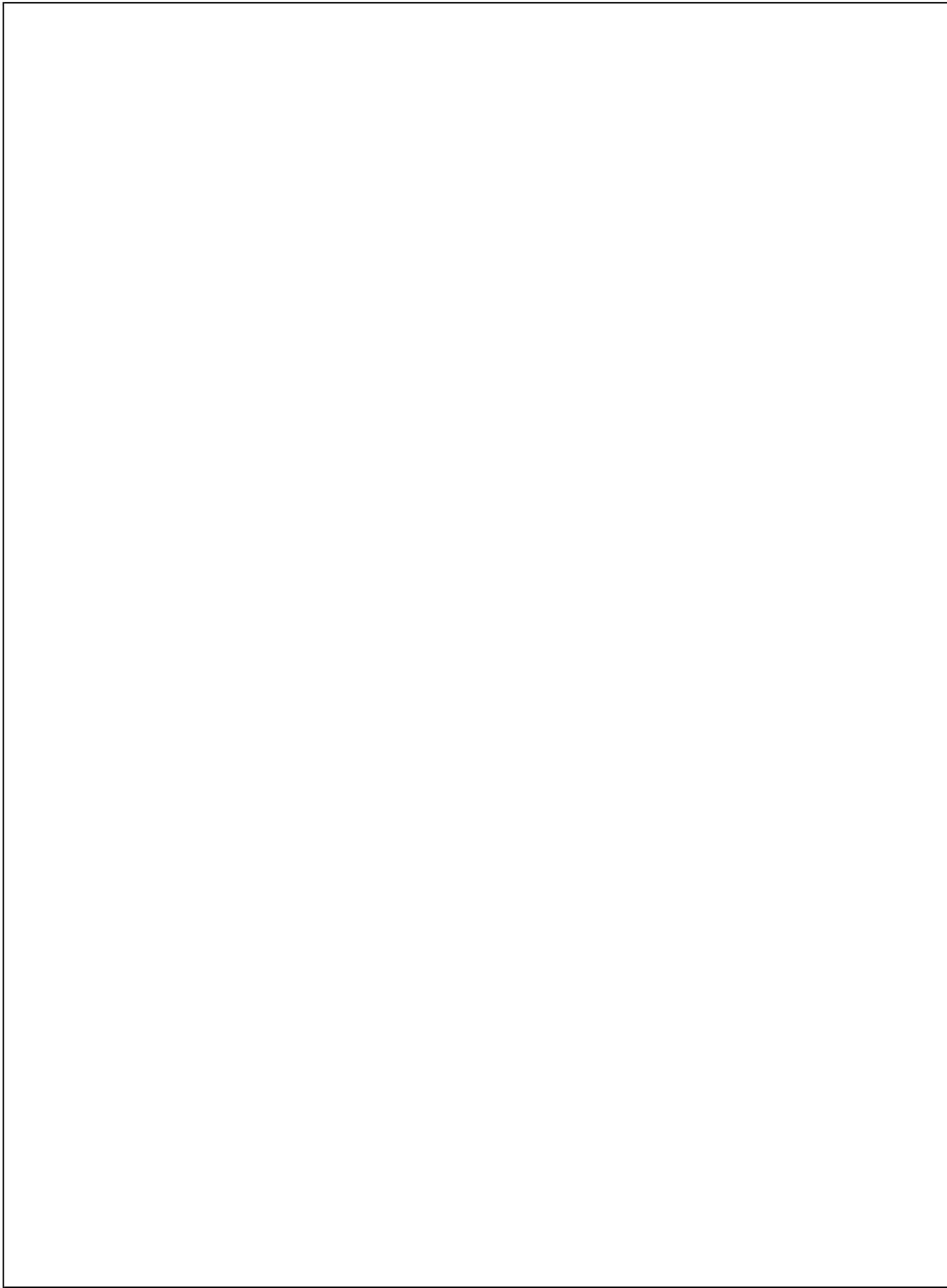
## Transmitter DC Electrical Characteristics



### Transmitter AC Electrical Characteristics

Typical values are at  $T_A=25^{\circ}\text{C}$  and with  $V_{CC}=3.3\text{V}$ ; minimum and maximum are at over supply voltages and operating temperatures ranges, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{TCP}$	Transmit Clock Period	Figure 9	11.76	T	50.00	ns
$t_{TCH}$	Transmit Clock (TxCLKIn) HIGH Time		0.35	0.50	0.65	T
$t_{TCL}$	Transmit Clock LOW Time		0.35	0.50	0.65	T
$t_{CLKT}$	TxCLKIn Transition Time (Rising and Falling)	(10% to 90%) Figure 10	1.0		6.0	ns
$t_{JIT}$	TxCLKIn Cycle-to-Cycle Jitter				3.0	
$t_{XIT}$	TxIn Transition Time		1.5		6.0	ns





### Receiver AC Characteristics

Typical values are at  $T_A=25^{\circ}\text{C}$  and with  $V_{CC}=3.3\text{V}$ ; minimum and maximum are at over supply voltages and operating temperatures ranges, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
--------	-----------	-----------	------	------	------	------

## Receiver AC Characteristics

Typical values are at  $T_A=25^\circ\text{C}$  and with  $V_{CC}=3.3\text{V}$ ; minimum and maximum are at over supply voltages and operating temperatures ranges, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{RSP0}$	Receiver Input Strobe Position of Bit 0	Figure 21, $f=66\text{MHz}$	0.7	1.1	1.4	ns
$t_{RSP1}$	Receiver Input Strobe Position of Bit 1		2.9	3.3	3.6	
$t_{RSP2}$	Receiver Input Strobe Position of Bit 2		5.1	5.5	5.8	
$t_{RSP3}$	Receiver Input Strobe Position of Bit 3		7.3	7.7	8.0	
$t_{RSP4}$	Receiver Input Strobe Position of Bit 4		9.5	9.9	10.2	
$t_{RSP5}$	Receiver Input Strobe Position of Bit 5		11.7	12.1	12.4	
$t_{RSP6}$	Receiver Input Strobe Position of Bit 6		13.9	14.3	14.6	
$t_{RSKM}$	RxIn Skew Margin <sup>(19)</sup>	$f=40\text{MHz}$ , Figure 21	490			ps

## Test Circuits

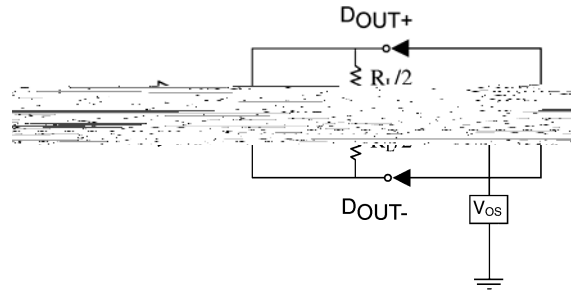
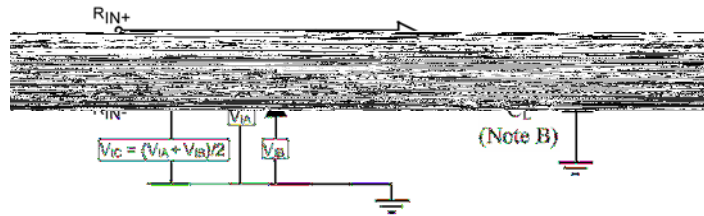


Figure 5. Differential LVDS Output DC Test Circuit



### Notes:

- A: For all input pulses,  $t_r$  or  $t_f \leq 1\text{ns}$ .
- B:  $C_L$  includes all probe and jig capacitance.

Figure 6. Differential Receiver Voltage Definitions, Propagation Delay, and Transition Time Test Circuit

Table 4. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)
$V_{IA}$	$V_{IB}$	$V_{ID}$	$V_{ICM}$
1.25	1.15	100	1.20
1.15	1.25	-100	1.20
2.40	2.30	100	2.35
2.30	2.40	-100	2.35
0.10	0	100	0.05
0	0.10	-100	0.05
1.50	0.90	600	1.20
0.90	1.50	-600	1.20
2.40	1.80	600	2.10
1.80	2.40	-600	2.10
0.60	0	600	0.30
0	0.60	-600	0.30

## AC Loadings and Waveforms

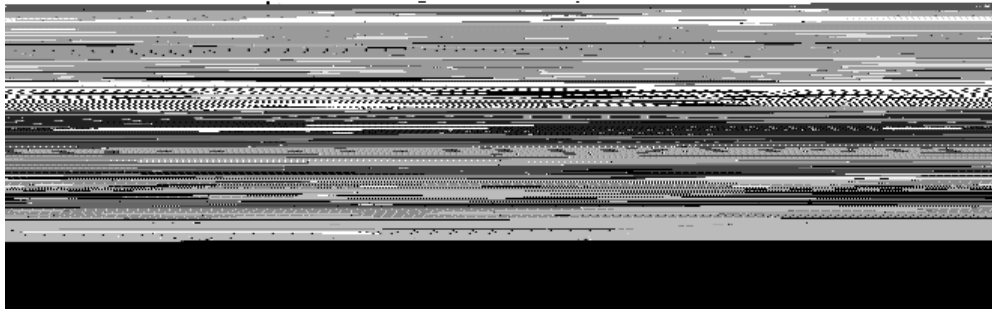


Figure 7. Worst-Case Test Pattern

**Note:**

20. The worst-case test pattern produces a maximum toggling of digital circuits, LVDS I/O, and LVTTTL/CMOS I/O. Depending on the valid strobe edge of the transmitter, the TxCLKIn can be rising or falling edge data strobe.

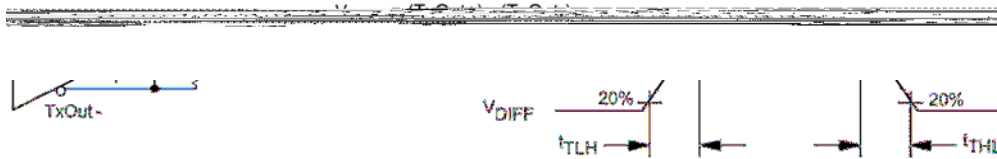


Figure 8. Transmitter LVDS Output Load and Transition Times

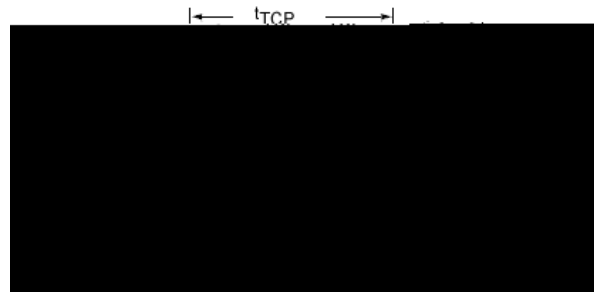


Figure 9. Transmitter Setup/Hold and HIGH/LOW Times (Rising-Edge Strobe)

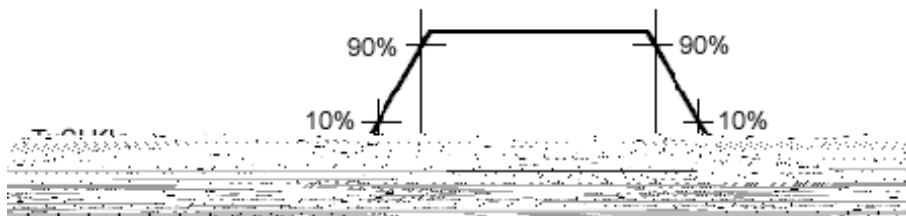


Figure 10. Transmitter Input Clock Transition Time

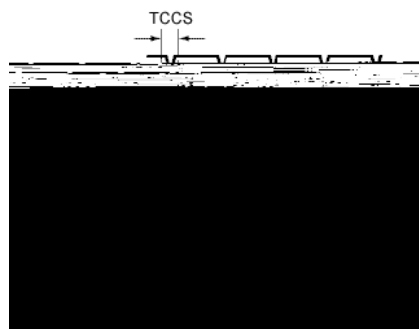


Figure 11. Transmitter Outputs Channel-to-Channel Skew

AC Loadings and Waveforms (Continued)

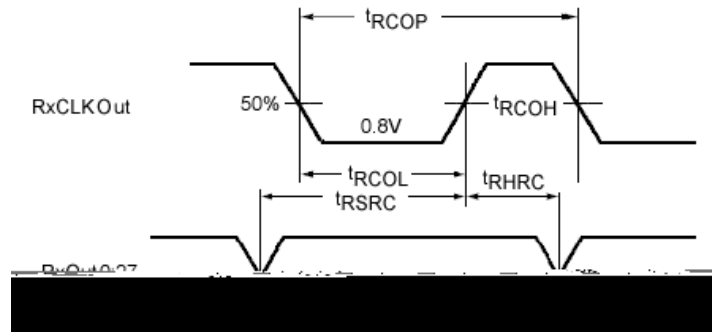


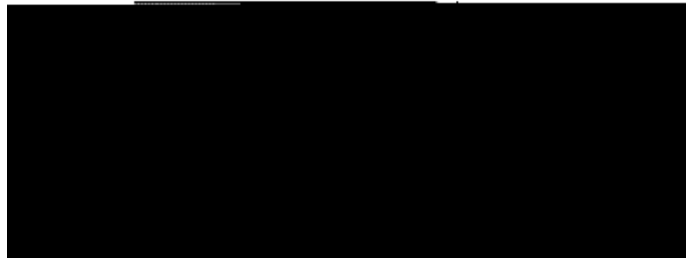
Figure 12. Receiver Setup/Hold and HIGH/LOW Times

**Note:**

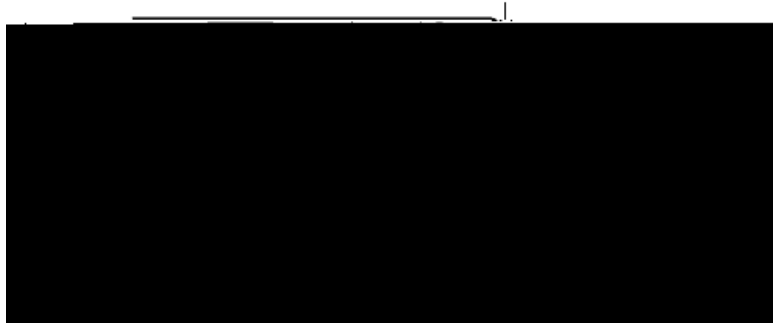
21. For the receiver with falling-edge strobe, the definition of setup/hold time is slightly different from the one with



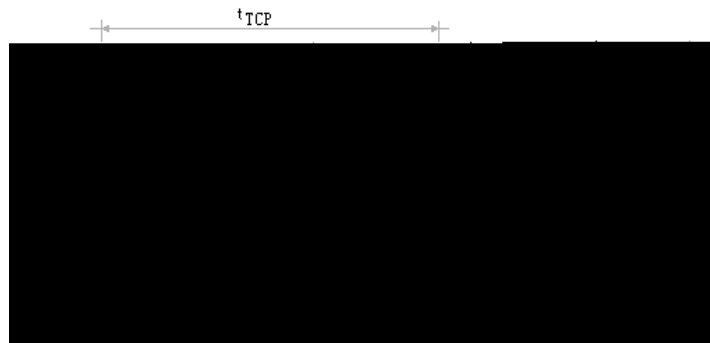
**AC Loadings and Waveforms (Continued)**



**Figure 16. Transmitter Power-Down Delay**



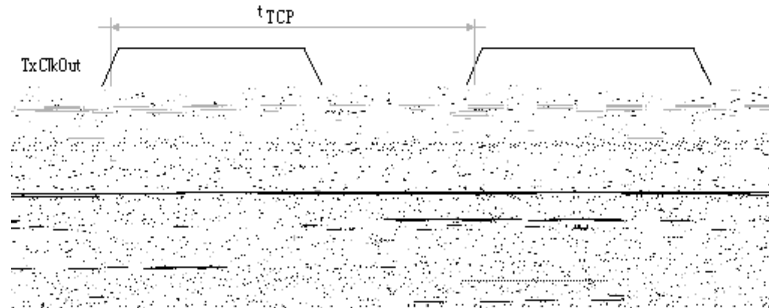
**Figure 17. Receiver Power-Down Delay**



**Figure 18. 28 Parallel LVTTTL Inputs Mapped to Four Serial LVDS Outputs**

**Note:**

22. The information in this diagram shows the difference between clock out and the first data bit. A 2-bit cycle delay is guaranteed when the MSB is output from the transmitter.



**Figure 19. 21 Parallel LVTTTL Inputs Mapped to Three Serial Outputs**

**Note:**

23. This output data pulse position works for both transmitters with 21 TTL inputs, except the LVDS output bit mapping difference. Two-bit cycle delay is guaranteed with the MSB is output from transmitter.

## AC Loadings and Waveforms (Continued)

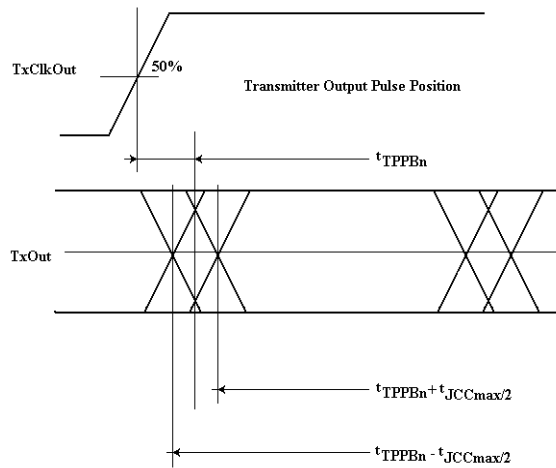


Figure 20. Transmitter Output Pulse Bit Position

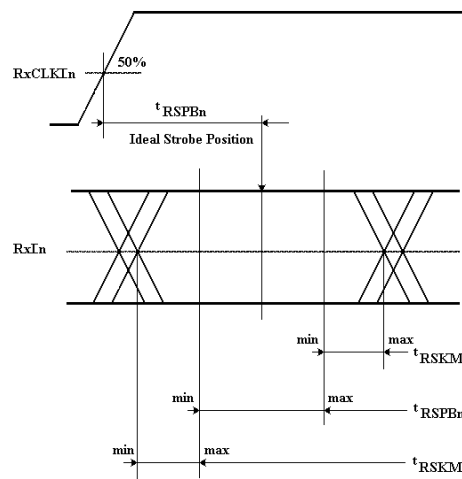


Figure 21. Receiver Input Bit Position



Figure 22. Receiver LVDS Input Skew Margin

**Note:**

24.  $t_{RSKM}$  is the budget for the cable skew and source clock skew plus Inter-Symbol Interference (ISI). The minimum and maximum pulse position values are based on the bit position of each of the seven bits within the LVDS data stream across PVT (Process, Voltage Supply, and Temperature).



AC Loadings and Waveforms (Continued)

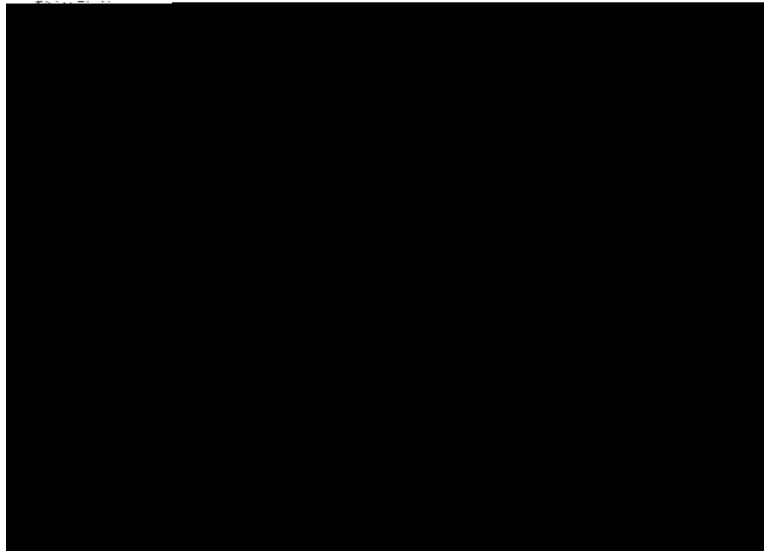


Figure 25. “16-Grayscale” Test Pattern

Note:

- 29. The 16-grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.

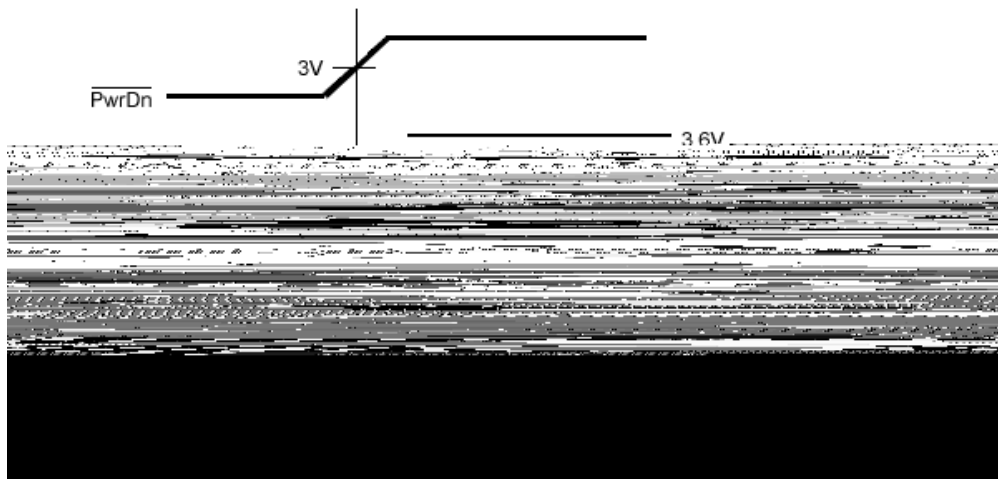
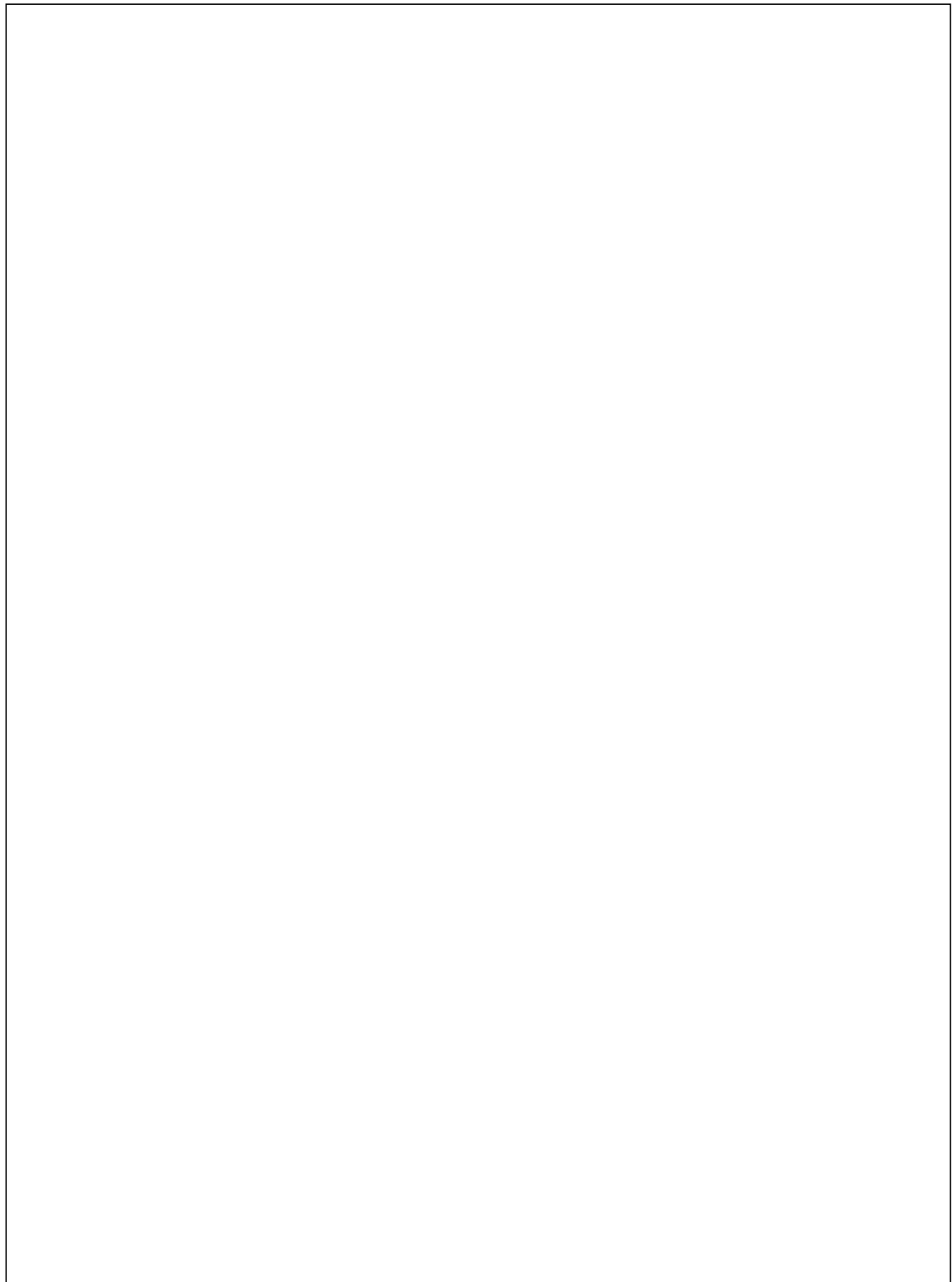



Figure 26. Transmitter Phase-Lock-Loop Time





ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent\\_Marking.pdf](http://www.onsemi.com/site/pdf/Patent_Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303 675 2175 or 800 344 3860 Toll Free USA/Canada  
**Fax:** 303 675 2176 or 800 344 3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800 282 9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81 3 5817 1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative