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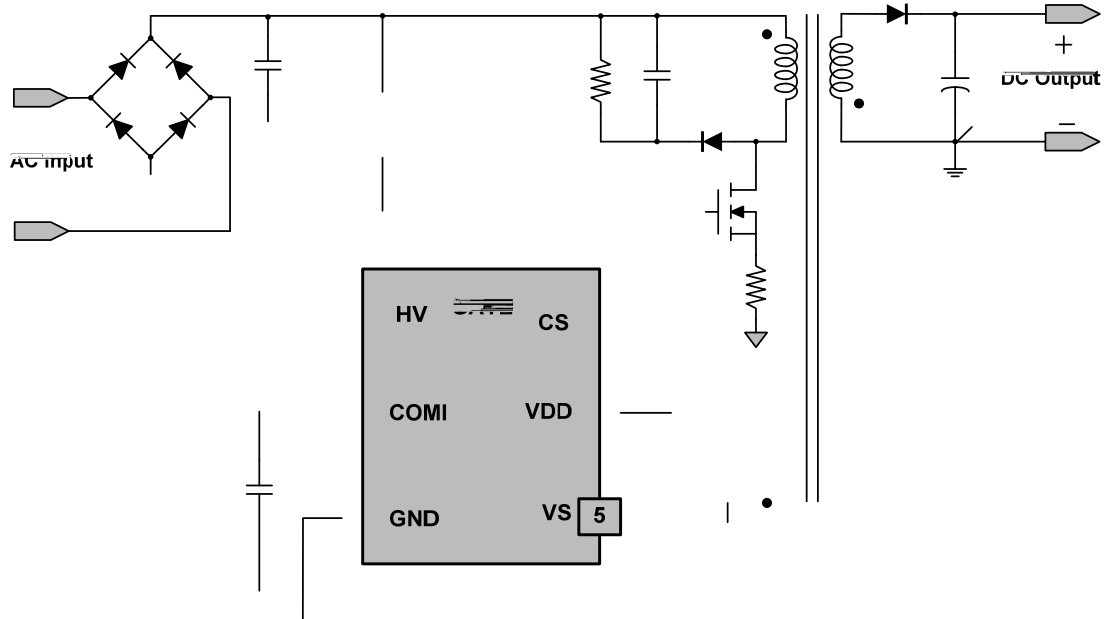
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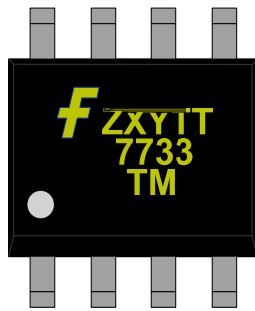
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Application Diagram



Marking Information



F: Fairchild Logo
Z: Plant Code
X: 1-Digit Year Code
Y: 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (M=SOP)
M: Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

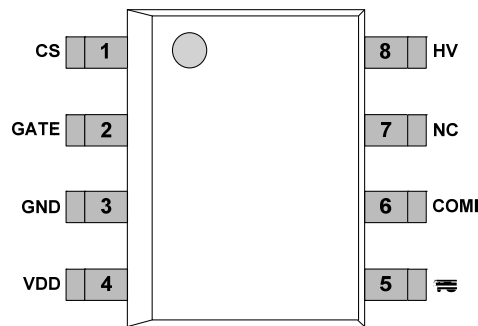


Figure 4. Pin Configuration (Top View)

Pin Descriptions

Pin #	Name	Description
1	CS	Current Sense. This pin connects a current-sense resistor to detect the MOSFET current for constant output current regulation.
2	GATE	PWM Signal Output. This pin uses the internal totem-pole output driver to drive the power MOSFET.
3	GND	Ground
4	VDD	Power Supply. IC operating current and MOSFET driving current are supplied using this pin.
5	VS	Voltage Sense. This pin detects the output voltage and discharge time information for CC regulation. This pin is connected to the auxiliary winding of the transformer via a resistor divider.
6	COMI	Constant Current Loop Compensation. This pin is connected to a capacitor between COMI and GND for compensating the current loop gain.
7	NC	No Connect
8	HV	High Voltage. This pin is connected to the rectified input voltage via a resistor.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
HV	HV Pin Voltage		700	V
V _{VDD}	DC Supply Voltage ^(1,2)		30	V
V _{VS}	VS Pin Input Voltage	-0.3	6.0	V
V _{CS}	CS Pin Input Voltage	-0.3	6.0	V
V _{COMI}	COMI Pin Input Voltage	-0.3	6.0	V
V _{GATE}	GATE Pin Input Voltage	-0.3	30.0	V
P _D T	Power Dissipation (T _A 50°C)		633	mW

Electrical Characteristics

$V_{DD}=15\text{ V}$, $T_J=-40$ to $+125^\circ\text{C}$, unless otherwise specified. Currents are defined as positive into the device and negative out of device.

Electrical Characteristics (Continued)

$V_{DD}=15\text{ V}$, $T_J=-40$ to $+125^\circ\text{C}$, unless otherwise specified. Currents are defined as positive into the device and negative out of device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VOLTAGE-SENSE SECTION						
$V_{VS-MAX-CC}$	V_S for Maximum Frequency in CC	$f=f_{MAX-CC}-2\text{ kHz}$	2.25	2.35	2.45	V
$V_{VS-MIN-CC}$	V_S for Minimum Frequency in CC	$f=f_{MIN-CC}+2\text{ kHz}$	0.55	0.85	1.15	V
$t_{DIS-BNK}$	t_{DIS} Blanking Time of V_S ⁽⁵⁾		0.85	1.15	1.45	μs
I_{VS-BNK}	V_S Current for VS Blanking		-75	-90	-105	μA
V_{VS-OVP}	V_S Level for Output Over-Voltage Protection		2.95	3.00	3.15	V
$V_{VS-LOW-CL-EN}$	V_S Threshold Voltage to Enable Low Current Limit ⁽⁵⁾		0.25	0.30	0.35	V
$V_{VS-HIGH-CL-DIS}$	V_S Threshold Voltage to Disable Low Current Limit ⁽⁵⁾		0.54	0.60	0.66	V
$V_{VS-SLP-TH}$	V_S Threshold Voltage for Output Short-LED Protection		0.25	0.30	0.35	V
$t_{SLP-BNK}$	V_S Detection Disable Time after Startup ⁽⁵⁾	$T_A=25^\circ\text{C}$		15		ms
CURRENT-SENSE SECTION						
V_{RV}	Reference Voltage	$T_A=25^\circ\text{C}$	1.485	1.500	1.515	V
t_{LEB}	Leading-Edge Blanking Time ⁽⁵⁾			300		ns
t_{MIN}	Minimum On Time in CC ⁽⁵⁾	$V_{COMI}=0\text{ V}$		500		ns
t_{PD}	Propagation Delay to GATE Output		50	100	150	ns
$V_{CS-HIGH-CL}$	High Current Limit Threshold		0.9	1.0	1.1	V

V

Typical Performance Characteristics

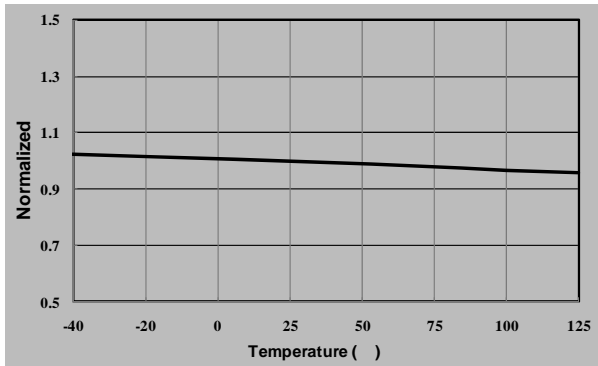


Figure 5. V_{DD-ON} vs. Temperature

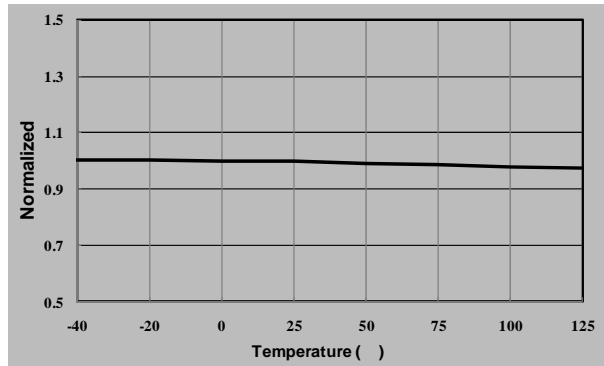


Figure 6. V_{DD-OFF} vs. Temperature

Typical Performance Characteristics (Continued)

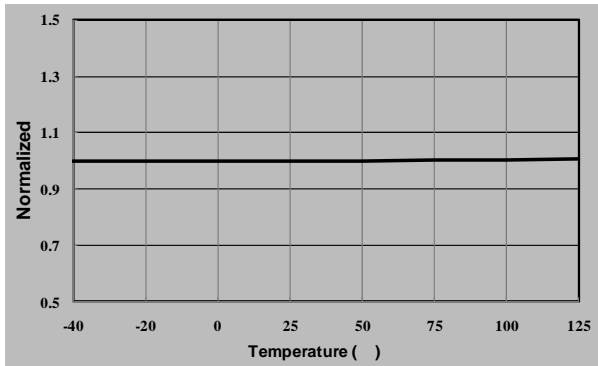


Figure 11. V_{VR} vs. Temperature

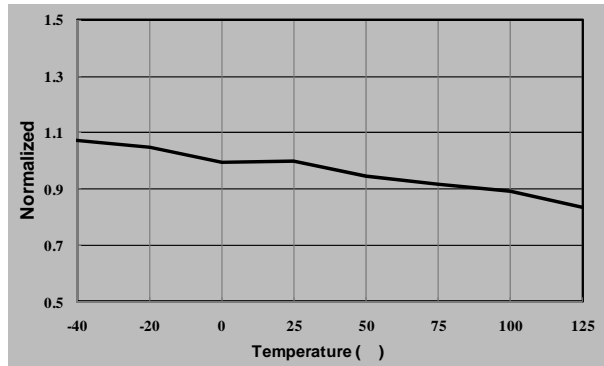


Figure 12. G_m vs. Temperature

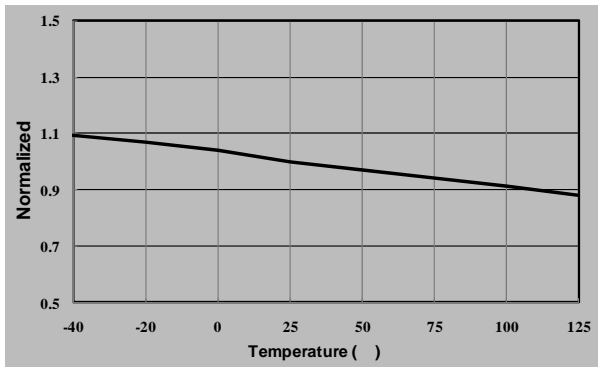


Figure 13. $I_{COMI-SOURCE}$ vs. Temperature

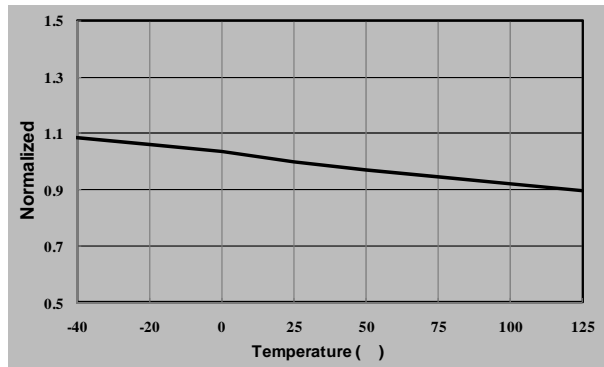


Figure 14. $I_{COMI-SINK}$ vs. Temperature

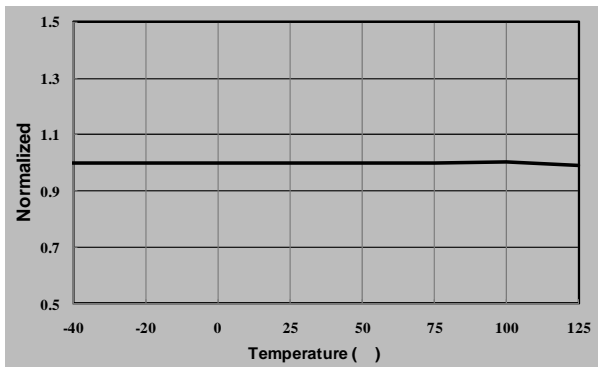


Figure 15. V_{VS-OVP} vs. Temperature

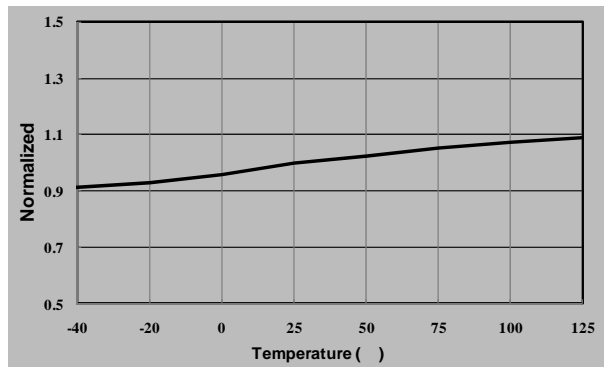


Figure 16. V_{CS-OCF} vs. Temperature

Functional Description

FL7733 is AC-DC PWM controller for LED lighting applications. TRUECURRENT[®] techniques regulate accurate constant LED current; independent of input voltage, output voltage, and magnetizing inductance variations. The DCM control in the oscillator reduces conduction loss and maintains DCM operation over a wide range of output voltage, which implements high power factor correction in a single-stage flyback or buck-boost topology. A variety of protections, such as LED short / open protection, sensing resistor short / open protection, over-current protection, over-temperature protection, and cycle-by-cycle current limitation stabilize system operation and protect external components.

Startup

At startup, an internal high-voltage JFET supplies startup current and V_{DD} capacitor charging current, as shown in Figure 17. When V_{DD} reaches 16 V, switching begins and the internal high-voltage JFET continues to supply V_{DD} operating current for an initial 250 ms to maintain V_{DD} voltage higher than V_{DD-OFF} . As the output voltage increases, the auxiliary winding becomes the dominant V_{DD} supply current source.

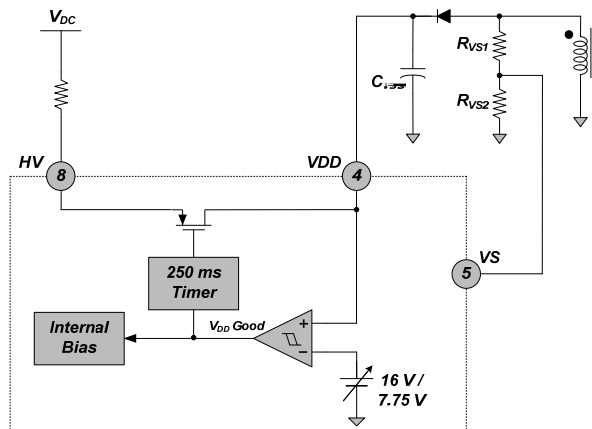


Figure 17. Startup Block

Switching is controlled by current-mode for 20 ms after V_{DD-ON} . During current-mode switching with the flyback or buck-boost topology, output current is only determined by output voltage. Therefore, the output voltage increases with constant slope, regardless of line voltage variation. Short-LED Protection (SLP) is enabled after the 15 ms SLP blanking time so that the output

where, n_{PS} is the primary-to-secondary turn ratio and R_S is a sensing resistor connected between the source terminal of the MOSFET and ground.

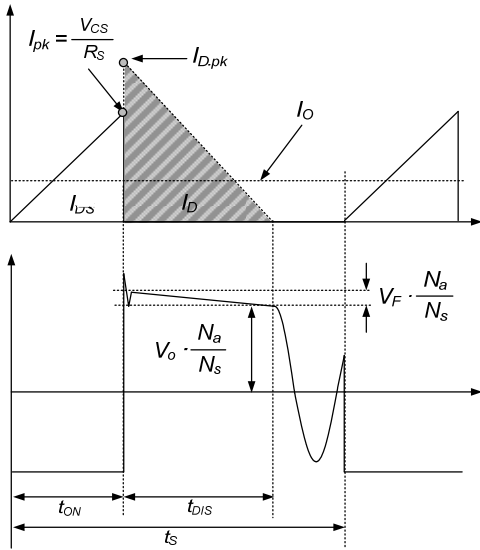
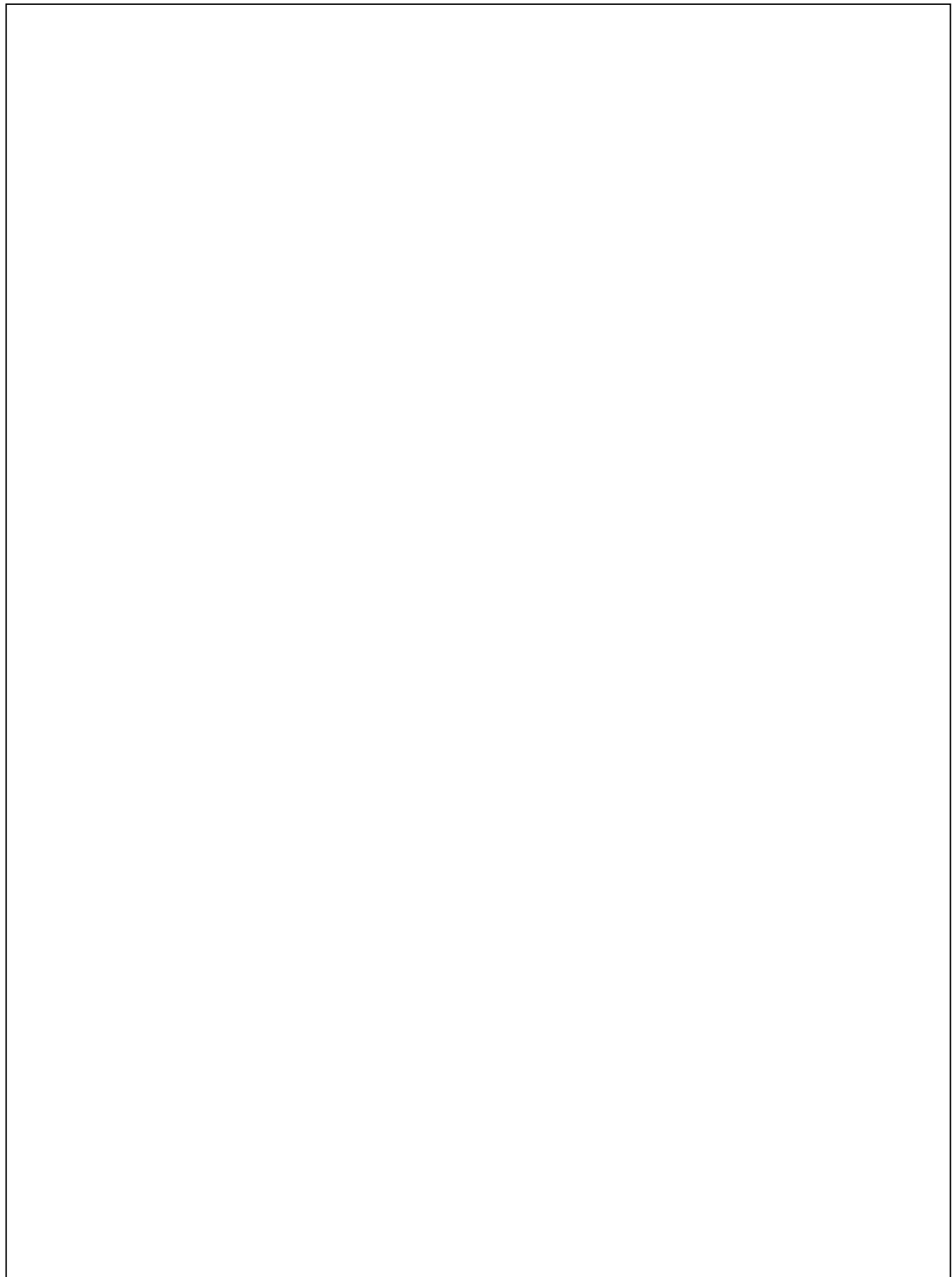


Figure 20. Key Waveforms for Primary-Side Regulation

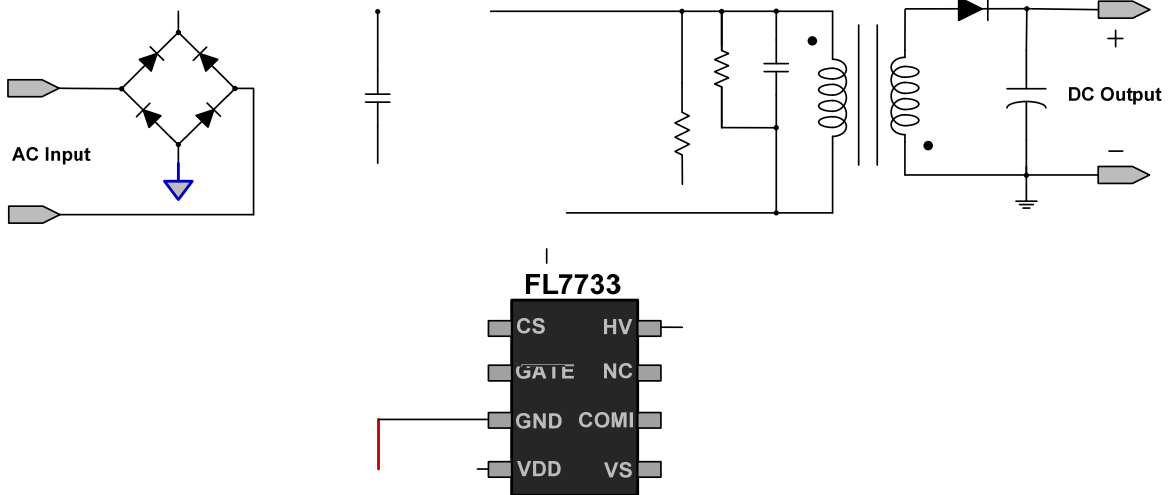
The output of the current calculation is compared with an internal precise voltage reference to generate an error voltage (V



PCB Layout Guidance

PCB layout for a power converter is as important as circuit design because PCB layout with high parasitic inductance or resistance can lead to severe switching noise with system instability. PCB should be designed to minimize switching noise into control signals.

1. The signal ground and power ground should be separated and connected only at one position (GND pin) to avoid ground loop noise. The power ground path from the bridge diode to the sensing resistors should be short and wide.
2. Gate-driving current path (GATE – R_{GATE} – MOSFET – R_{CS} – GND) must be as short as possible.
3. Control pin components; such as C_{COM1}, C_{VS}, and R_{VS2}; should be placed close to the assigned pin and signal ground.
4. High-voltage traces related to the drain of MOSFET and RCD snubber should be kept far way from control circuits to avoid unnecessary interference.
5. If a heat sink is used for the MOSFET, connect this heat sink to power ground.
6. The auxiliary winding ground should be connected closer to the GND pin than the control pin components' ground.



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