Primary-Side-Regulated LED Driver with Power Factor Correction

FL7733A

Description

The FL7733A is a highly integrated PWM controller with advanced Primary Side Regulation (PSR) technique to minimize components in

PIN DESCRIPTION

Pin No.	Name	Description
1	CS	. This pin connects a current−sense resistor to detect the MOSFET current for constant output current regulation.
2	GATE	

ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V, T_J = −40 to +125°C, unless otherwise specified. Currents are defined as positive into the device and negative out of device.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD-ON}	Turn−On Threshold Voltage		14.5	16.0	17.5	V
V_{DD-OFF}	Turn−Off Threshold Voltage		6.75	7.75	8.75	V
I_{DD-OP}	Operating Current	C_L = 1 nF, f = f_{MAX-CC}	3		5	mA
I_{DD-ST}	Startup Current	V_{DD} = V_{DD-ON} − 1.6 V	−		100	μA
$V_{VDD-OVP}$	V_{DD} Over−Voltage Protection Level		23	24	25.5	V
GATE SECTION						
V_{OL}	Output Voltage Low	T_A = 25°C, V_{DD} = 20 V, I_{DD_GATE} = 1 mA	−	−	1.5	

ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V, T_J = −40 to +125°C, unless otherwise specified. Currents are defined as positive into the device and negative out of device.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
CURRENT−SENSE SECTION						
V_{RV}	Reference Voltage	T_A = 25°C	1.485	1.500	1.515	V
t_{LEB}	Leading−Edge Blanking Time (Note 5)		−	300	−	ns
t_{MIN}	Minimum On Time in CC (Note 5)	V_{COMI} = 0 V	−	500	−	ns
t_{PD}	Propagation Delay to GATE Output		50	100	150	ns
$V_{CS−HIGH−CL}$	High Current Limit Threshold		0.9	1.0	1.1	V
$V_{CS−LOW−CL}$	Low Current Limit Threshold		0.16	0.20	0.24	V
$t_{LOW−CM}$	Low Current Mode Operation Time at Startup (Note 5)		−	20	−	ms
$V_{CS−SRSP}$	V_{CS} Threshold Voltage for Sensing Resistor Short Protection		−	−	0.1	V
$V_{CS−OCP}$	V_{CS} Threshold Voltage for Over−Current Protection	T_A = 25°C	1.20	1.35	1.50	V
V_{CS} / I_{VS}	Relation of Line Compensation Voltage and V_S Current (Note 5)		−	21.5	−	V/A
OSCILLATOR SECTION						
$f_{MAX−CC}$	Maximum Frequency in CC	T_A = 25°C, V_S = 3.0 V	65	70	75	kHz
$f_{MIN−CC}$	Minimum Frequency in CC	T_A = 25°C, V_S = 0.3 V	24.0	29.5	33.0	kHz
$t_{ON−MAX}$	Maximum Turn−On Time	T_A = 25°C, f = $f_{MAX−CC}$	11.0	13.5	16.0	μs
OVER−TEMPERATURE						

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

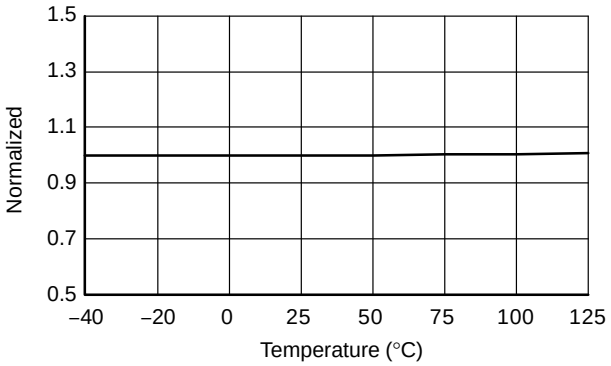

Figure 9. V_{VR} vs. Temperature

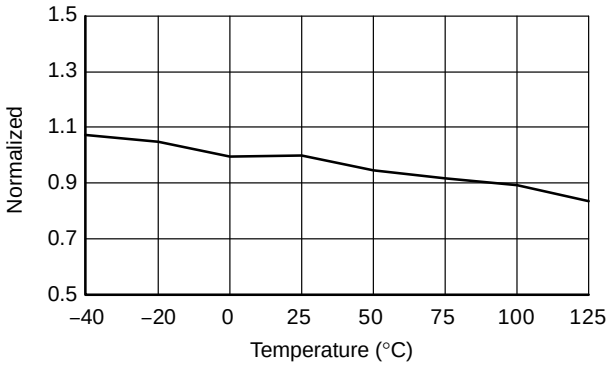

Figure 10. Gm vs. Temperature

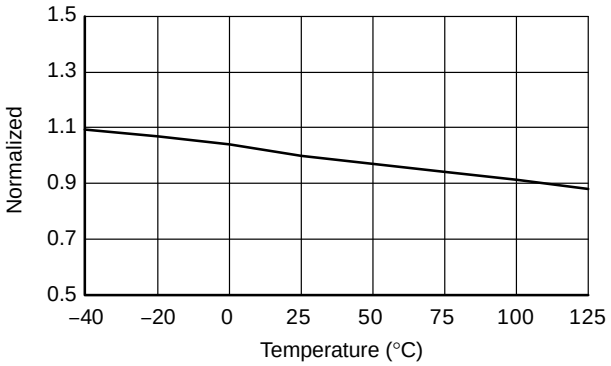

Figure 11. $I_{COMI-SOURCE}$ vs. Temperature

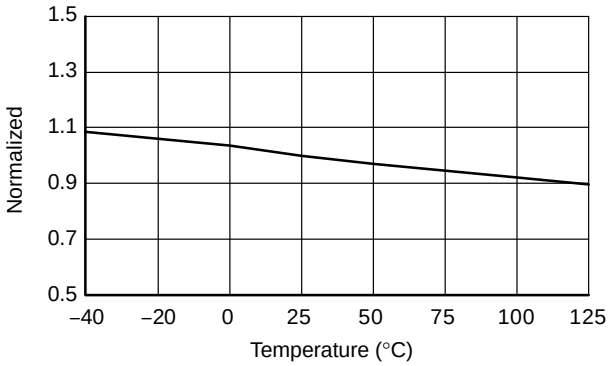

Figure 12. $I_{COMI-SINK}$ vs. Temperature

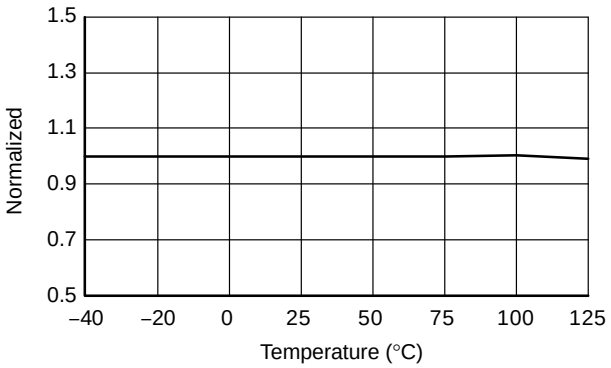

Figure 13. V_{VS-OVP} vs. Temperature

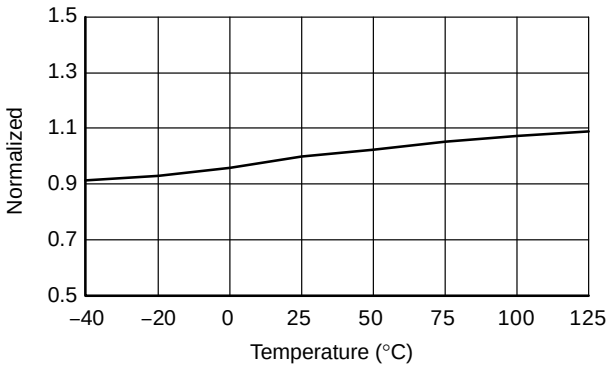

Figure 14. V_{CS-OCP} vs. Temperature

FUNCTIONAL DESCRIPTION

FL7733A is AC DC PWM controller for LED lighting applications. TRUECURRENT technology regulate accurate constant LED current independent of input voltage, output voltage, and magnetizing inductance variations. The DCM control in the oscillator reduces conduction loss and maintains DCM operation over a wide range of output voltage, which implements high power factor correction in a single stage flyback or buck boost topology. A variety of protections, such as LED short / open protection, sensing resistor short / open protection, over current protection, over temperature protection, and cycle by cycle current limitation stabilize system operation and protect external components.

Startup

At startup, an internal high voltage JFET supplies startup current and V_{DD} capacitor charging current, as shown in Figure 15. When V_{DD} reaches 16 V, switching begins and the internal high voltage JFET continues to supply V_{DD} operating current for an initial 250 ms to maintain V_{DD} voltage higher than $V_{DD\ OFF}$. As the output voltage increases, the auxiliary winding becomes the dominant V_{DD} supply current source.

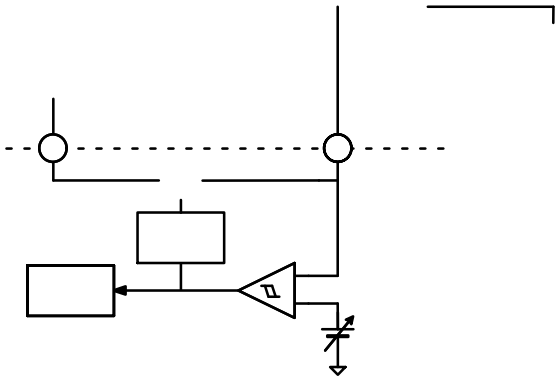

Figure 15. Startup Block

$$\frac{t_{DIS}}{t_S} \cdot V_{CS} = 0.25 \quad \text{(eq. 2)}$$

$$I_O = 0.125 \cdot \frac{n_{PS}}{R_S} \quad \text{(eq. 3)}$$

where, n_{PS} is the primary to secondary turn ratio and R_S is a sensing resistor connected between the source terminal of the MOSFET and ground.

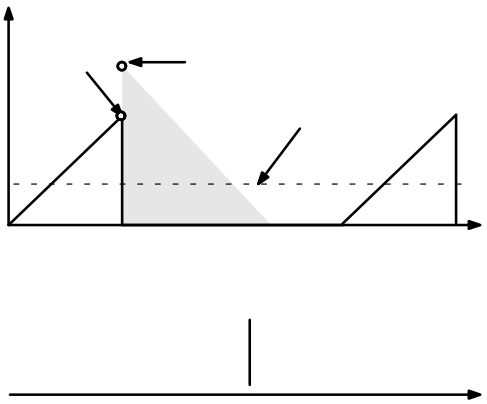

Figure 18. Key Waveforms for Primary−Side Regulation

Under−Voltage Lockout (UVLO)

The V_{DD} turn on and turn off thresholds are fixed internally at 16 V and 7.75 V, respectively. During startup, the V_{DD} capacitor must be charged to 16 V through the high voltage JFET to enable the FL7733A. The V_{DD} capacitor continues to supply V_{DD} until auxiliary power is delivered from the auxiliary winding of the main transformer. V_{DD} should remain higher than 7.75 V during this startup process. Therefore, the V_{DD} capacitor must be adequate to keep V_{DD} over the UVLO threshold until the auxiliary winding voltage is above 7.75 V.

Over−Current Protection (OCP)

When an output diode or secondary winding are shorted, switch current with extremely high di/dt can flow through the MOSFET even by minimum turn on time. The FL7733A is designed to protect the system against this excessive current. When the CS voltage across the sensing resistor is higher than 1.35 V, the OCP comparator output shuts down GATE switching.

In a sensing resistor open condition, the sensing resistor voltage can't be detected and output current is not regulated properly. If the sensing resistor is damaged open circuit, the parasitic capacitor in the CS pin is charged by internal CS current sources. Therefore, the V_{CS} level is built up to the OCP threshold voltage and then switching is shut down immediately.

Over−Temperature Protection (OTP)

The temperature sensing circuit shuts down PWM output if the junction temperature exceeds 150°C. The hysteresis temperature after OTP triggering is 10°C.

PCB LAYOUT GUIDANCE

PCB layout for a power converter is as important as circuit design because PCB layout with high parasitic inductance or resistance can lead to severe switching noise with system instability. PCB should be designed to minimize switching noise into control signals.

1. The signal ground and power ground should be separated and connected only at one position (GND pin) to avoid ground loop noise. The power ground path from the bridge diode to the sensing resistors should be short and wide.
2. Gate driving current path (GATE – R_{GATE} – MOSFET – R_{CS} – GND) must be as short as possible.
3. Control pin components; such as C_{COMI}, C_{VS}, and R_{VS2}; should be placed close to the assigned pin and signal ground.
4. High voltage traces related to the drain of MOSFET and RCD snubber should be kept far way from control circuits to avoid unnecessary interference.
5. If a heat sink is used for the MOSFET, connect this heat sink to power ground.
6. The auxiliary winding ground should be connected closer to the GND pin than the control pin components' ground.

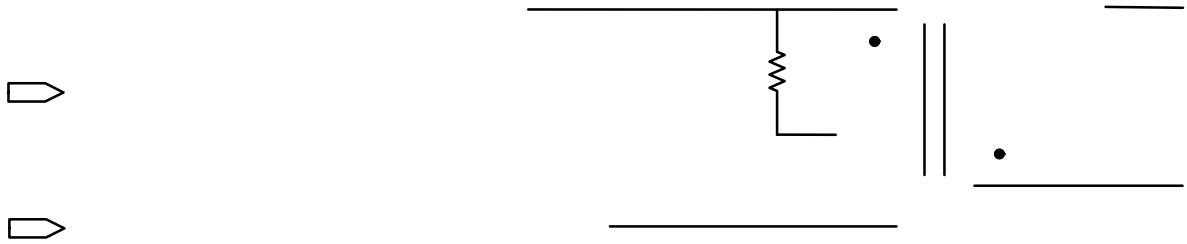

Figure 26. Layout Example

SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017