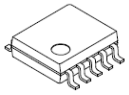
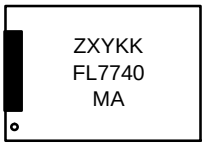
C a -V age P i a -Side-Reg a i PWM C e f P e Fac C ec i

FL7740



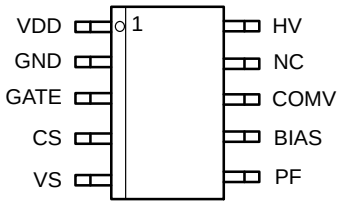
SOIC10
CASE 751EE

MARKING DIAGRAM



Z = Plant code
X = 1 digit year code
Y = 1 digit week code
KK = 2 digit lot traceability code
M = Package code
A = Product version

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

Description

The FL7740 provides accurate CV regulation in the steady state with differentiated dynamic function to minimize overshoot and undershoot of output voltage in line and load transient condition. Standby power is less than 0.3 W for smart lighting application and power factor is higher than 0.9 even at half load condition when enabling PF optimizer for wide output power scalability.

Startup time is less than 0.2 sec with built−in high voltage startup circuit and output voltage quickly reaches to the target CV level by loop gain transition technique during startup.

Various protections such as Overload, output diode short, sensing resistor short, output short and output over voltage protection guarantee high system reliability.

Features

- Wide Universal Input Range (90 V_{AC} ~ 305 V_{AC})
- Precise CV Regulation in the Steady State: < ±3 %
- CV Regulation in the load Transient: < ±10 %
- Overshoot−Less Fast HV Start Up Time (< 0.2 s)
- Low Standby Power
- PF Higher than 0.9 at High−Line and Half load by PF Optimizer
- Pulse−by−Pulse Current Limit
- Output Short Protection
- Output Over Voltage Protection
- Output Diode Short Protection
-

- Off Line Appliances Requiring Power Factor Correction

FL7740

FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	VDD	IC Supply	IC operating current and MOSFET driving current are supplied using this pin.
2	GND	Ground	Controller ground pin.
3	GATE	PWM Driver Output	This pin uses the internal totem−pole output driver to drive the power MOSFET.
4	CS	Current Sense	Connected to a current sense resistor to detect the MOSFET current for pulse−by− pulse current limit.
5	VS	Voltage Sense	This pin is connected to the auxiliary winding of the transformer via a resistor divider to detect the output voltage.
6	PF	Power Factor	This pin is connected to a resistor to optimize power factor.
7	BIAS	Internal Circuit BIAS	Bypass pin for the internal supply, which powers all control circuitry on the IC.
8	COMV	Loop Compensation	This pin is connected to a capacitor between COMV and GND for compensation.
9	NC	No Connection	
10	HV	High Voltage	This pin is connected to the rectified input voltage via a resistor for fast startup.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Units
$V_{HV(MAX)}$	HV Pin Voltage Range	560	V
$V_{MV(MAX)}$	VDD, GATE Pin Voltage Range	−0.3 to 30	V
$V_{LV(MAX)}$	COMV, PF, BIAS, VS, CS Pin Voltage Range	−0.3 to 6	V
$V_{LV(PULSE)}$	VS, CS Pin Negative Pulse Voltage at I_{LV} < 0.2 A and t_{PULSE} < 300 ns	−1.5	V
$P_{D(MAX)}$	Maximum Power Dissipation (T_A < 50°C)	663	mW
$T_{J(max)}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	−55 to 150	°C
$R_{\theta JA}$	Junction−to−Ambient Thermal Impedance	158	°C/W
$R_{\theta JC}$	Junction−to−Case Thermal Impedance	39	°C/W
ESD_{HBM}	ESD Capability, Human Body Model (Note 2)	2	kV
ESD_{CDM}	ESD Capability, Charged Device Model (Note 2)	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality

ELECTRICAL CHARACTERISTICS (continued)
V_{DD} = 18 V and T_J = −40 ~ 125°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
HW Section						
I_{HV-LC}	Leakage Current after Startup			1	10	μA
t_{R-JFET}	JFET Regulation Time at Startup	Design guaranteed	400	500	600	ms
$V_{DD-JFET-HL}$	V_{DD} High Limit during JFET Regulation		17.5	19.0	20.5	V
$V_{DD-JFET-LL}$	V_{DD} Low Limit during JFET Regulation		15.5	17.0	18.5	V
PWM Section						
$T_{ON-MIN-MIN}$	Min. Turn−on Time Min. Limit	Design guaranteed		0.40		μs
$T_{ON-MIN-MAX}$	Min. Turn−on Time Max. Limit	Design guaranteed		2.0		μs
T_{ON-MAX}	Max. Turn−on Time	Design guaranteed		23.3		μs
Oscillator Section						
f_{MAX}	Max. Frequency		60	65	70	kHz
f_{MIN}	Min. Frequency		0.72	0.80	0.88	kHz
Current Sense Section						
t_{LEB}	Leading−Edge Blanking Time	Design guaranteed		300		ns
t_{PD}	Propagation Delay to GATE	Design guaranteed	50	100	150	ns
Voltage Sense Section						
$t_{DIS-BNK}$	t_{DIS} Blanking Time at VS Sampling	Design guaranteed	0.95	1.00	1.05	μs
$V_{VS-CLAMP}$	VS Clamping Voltage	I_{VS}=1 mA I_{VS}=10 μA	−0.1		0.35	V
V_{REF}	Reference Voltage		3.465	3.5	3.535	V
$CV_{REGULATION}$	CV Regulation Tolerance	V_{VS} = 3.5 V, T_J = 25°C V_{VS} = 3.5 V, T_J = −40~125°C	−0.7 −1.2		+0.7 +1.2	%
g_M	Transconductance		16	20	24	μmho
$I_{COMV-SINK}$	COMV Sink Current	V_{VS} = 4 V	8	10	12	μA
$I_{COMV-SOURCE}$	COMV Source Current	V_{VS} = 3 V	8	10	12	μA
$V_{COMV-HGH}$	COMV High Voltage		4.7			V
$V_{COMV-LOW}$	COMV Low Voltage				0.1	V
Start Sequence Section						
$t_{SOFT-START}$	Soft Start Time	Design guaranteed		25.6		ms
$t_{SS1-MIN}$	SS1 Minimum Time	Design guaranteed		2		ms
$t_{SS1-MAX}$	SS1 Maximum Time	Design guaranteed		100		ms
t_{SS21}						

ELECTRICAL CHARACTERISTICS (continued)
V_{DD} = 18 V and T_J = −40 ~ 125°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Protection Section						
t_{AR}	Auto Restart Delay Time	Design guaranteed		3		s
$V_{VS-OS-H}$						

TYPICAL CHARACTERISTICS

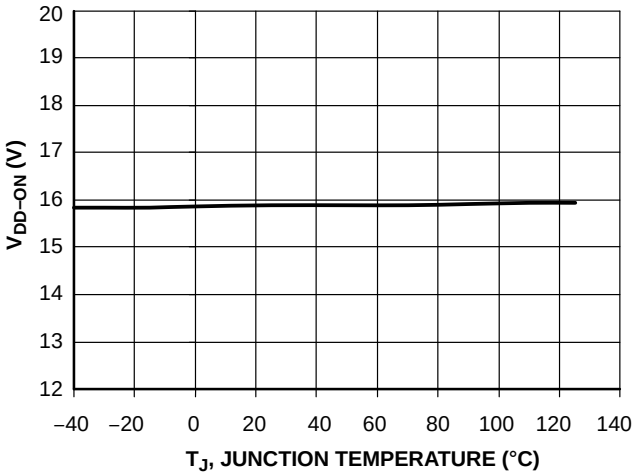


Figure 3. V_{DD-ON} vs. Temperature

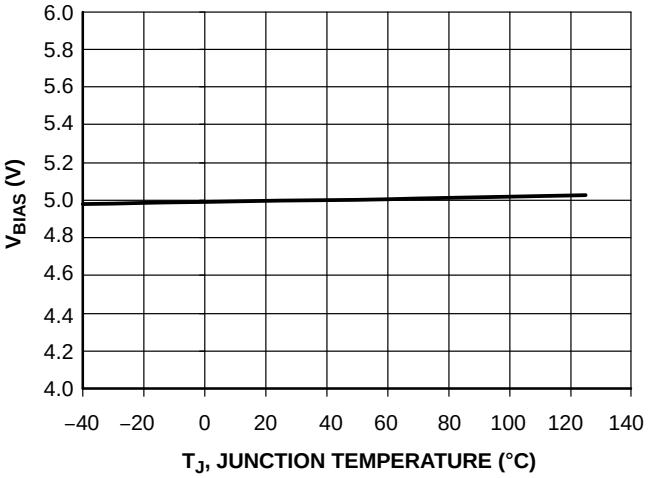


Figure 4. V_{BIAS} vs. Temperature

Figure 5. V20FL7740

TYPICAL CHARACTERISTICS (continued)

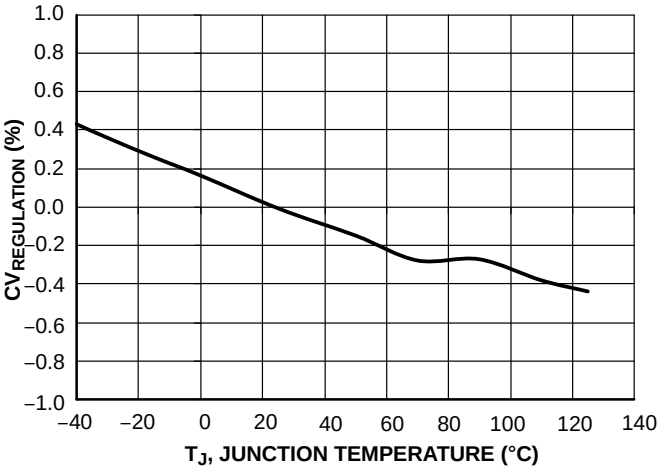


Figure 9. $CV_{REGULATIO\ N}$ vs. Temperature

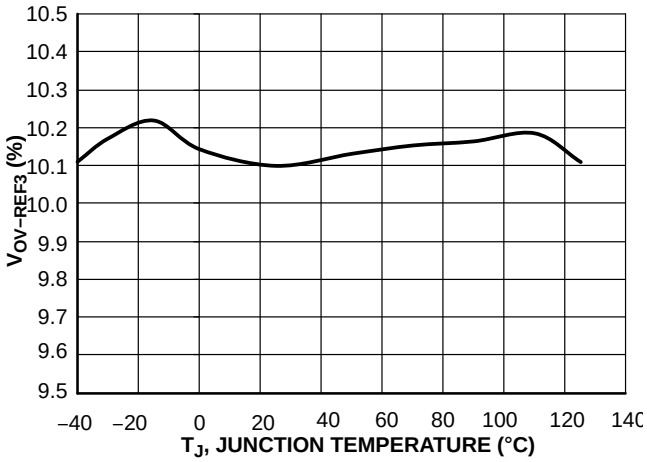


Figure 10. $VO_{V-REF}3$ vs. Temperature

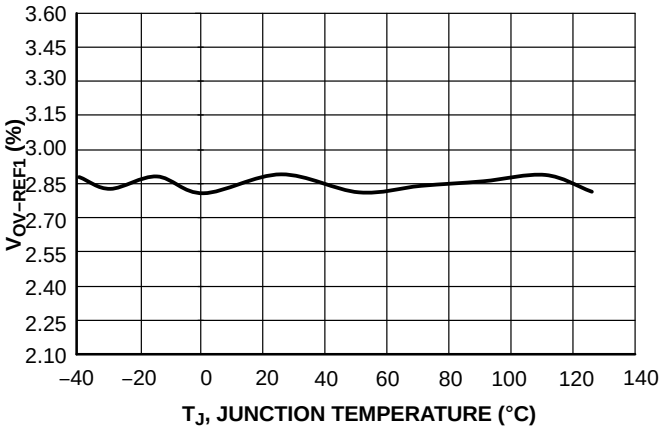


Figure 11. VOV_{-REF1} vs. Temperature

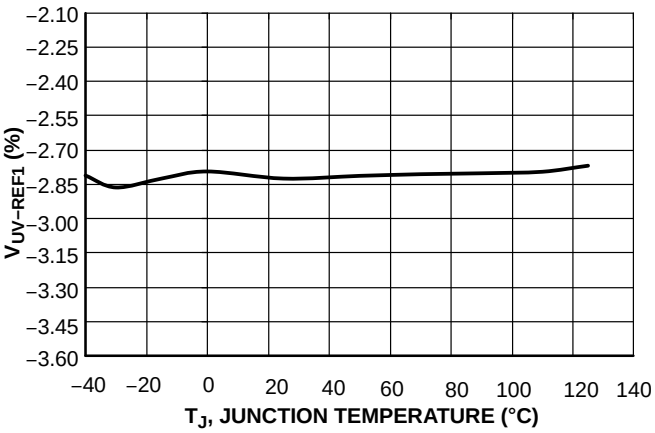


Figure 12. $V_{UV-REF1}$ vs. Temperature

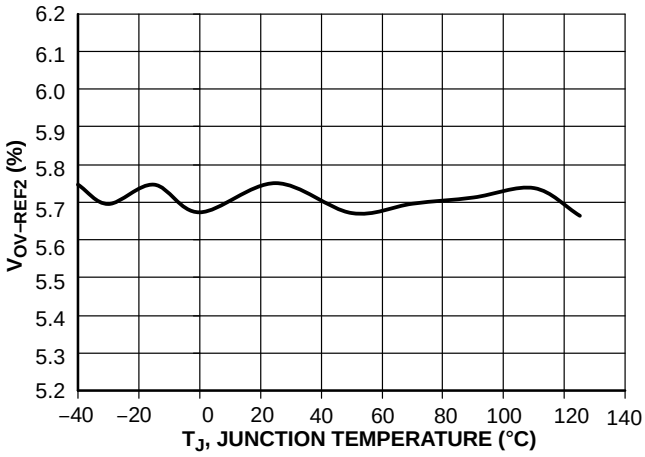
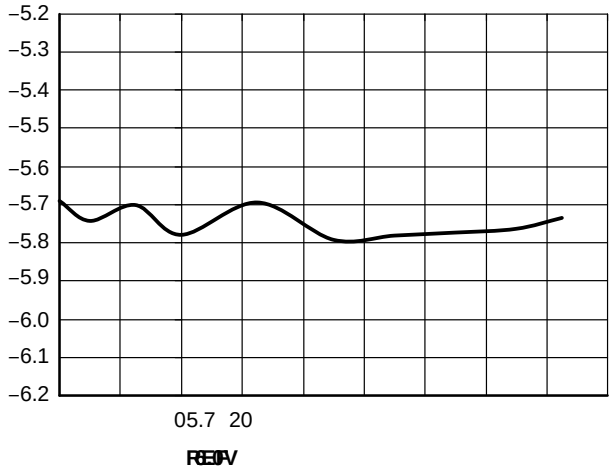


Figure 13. $_{VOV-REF2}$ vs. Temperature



APPLICATION INFORMATION

General

FL7740 is high power factor flyback controller with accurate primary side constant voltage regulation for smart LED lighting and ac−dc adapter, TV & monitors application. Precise output voltage detection and dynamic function manage good CV regulation. Startup is fast with internal HV biasing circuit with overshoot−less gain control. It guarantees high system reliable protection functions such as output over voltage, output short, over load, over current and thermal shut down protections.

Constant Voltage Regulation

VS pin detects output voltage information (= V_{EAV}) during secondary side diode conduction time and internal gm amplifier regulates the detected voltage at 3.5 V.

Dynamic Response at Load Transient

At load transient condition, V_{EAV} is shortly out of regulation due to the narrow PFC loop bandwidth. When V_{EAV}

Primary Side Constant Voltage Regulation

FL7740

Digital PF Optimizer

As line voltage increases and output load decreases, PF is degraded due to the effect of EMI filter capacitor charging/discharging current. Input current is the sum of EMI Filter capacitor current and flyback input current. Whether the flyback input current is exactly in−phase sinusoidal current with line voltage, 90° phase shifted EMI filter cap current worsens displacement factor of the overall system input current.

The **onsemi**'s proprietary PF optimizer accurately compensates the EMI filter capacitor current and improves PF more than 0.1 at high line and half load condition.

The calculation coefficient in the PF optimizer is externally programmable by supplying a certain level of voltage at PF pin with external resistive divider from 5 V BIAS pin. Before 1st switching, FL7740 converts the PF voltage into digital value without switching noise and keeps the digital value for the coefficient until UVLO is triggered.

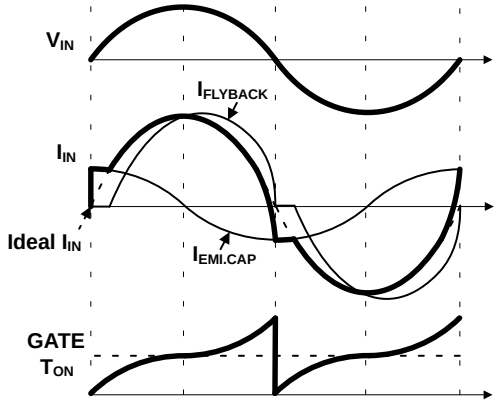


Figure 21. With PF Optimizer

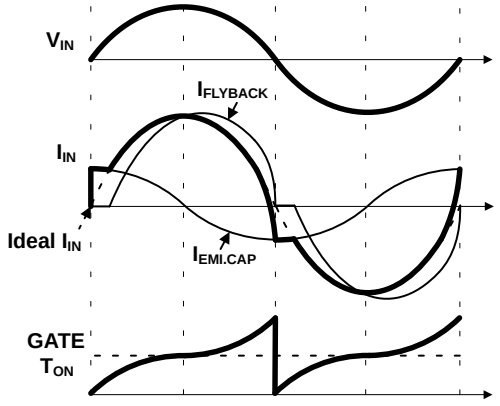


Figure 22. With PF Optimizer

Recommended V_{PF} is in Equation 1, where L_M is magnetizing inductance and C_{EMI} is total EMI filter capacitance.

$$V_{PF} = 5 \times 10^9 \times L_M \times C_{EMI} + 1.5 \qquad \text{(eq. 1)}$$

As V_{PF} increases, the coefficient in the PF optimizer calculation is larger with better PF, but THD is worse due to the input current distortion at input voltage zero cross. Therefore, V_{PF} adjustment by changing PF resistors is recommended to bring the best PF and THD performance to meet user's target. When V_{PF} is lower than 1.5 V, PF optimizer is disabled.

Protection

- Auto−restart:
  Once protection is triggered, FL7740 terminates switching and internal 3 sec counter makes delay time. In 3 sec, VDD voltage is regulated between 17 V and 19 V by internal HV biasing not to fall in UVLO. After 3 sec, VDD falls down to 7.75 V V_{DD-OFF} and IC is reset with released protection. When VDD voltage is up again to 16 V V_{DD-ON}, FL7740 begins startup sequence.

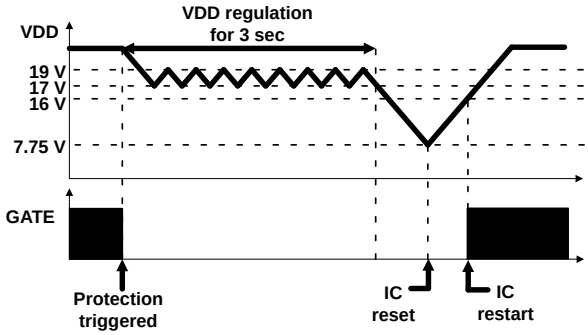


Figure 23. Auto Restart

M4.2 V @7(tion:)]TJ 1.2586 TD0 Tc[@ SET0 / 4.2 V @ Sm74 0 011 T

- Output Over Voltage Protection:
  Output over voltage is hardly triggered due to the powering limit by dynamic function. But, in the abnormal condition, output OVP is triggered when V_{EAV} is higher than 4.0 V @ SET0 / 4.2 V @ SET1 for 4 switching

FL7740