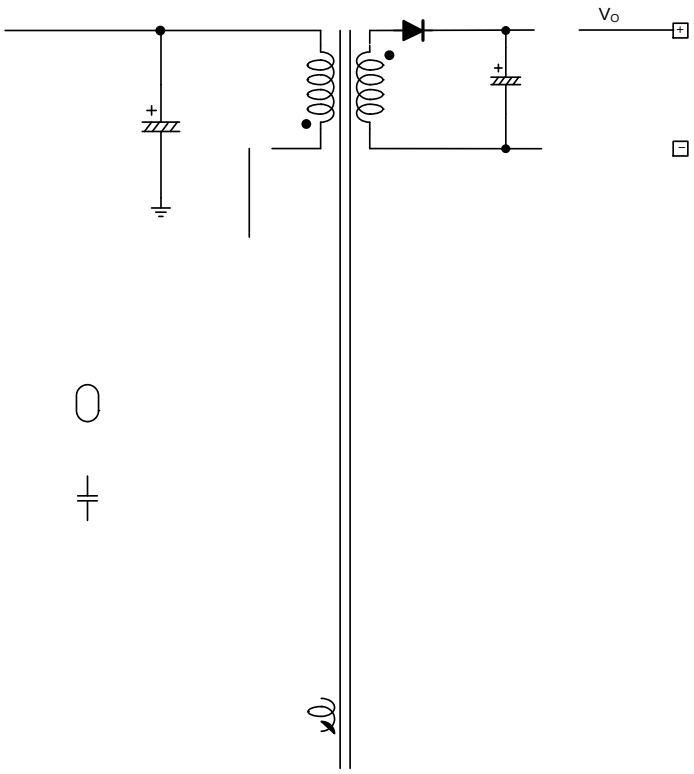
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CSPWM

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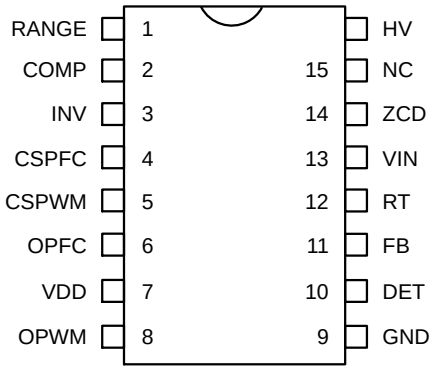

RANGE
1
COMP
2
INV
3
CSPFC
4
CSPWM
5
OPFC
6
VDD
7
OPWM
8
HV
15
NC
14
ZCD
13
VIN
12
RT
11
FB
10
DET
9
GND

(V_{DD} = 15 V and T_A = −40~105°C, unless otherwise noted)

V_{OP}	Continuously Operating Voltage		−	−	25	V
V_{DD-ON}	Turn−On Threshold Voltage		16.5	18.0	19.5	V
$V_{DD-PWM-OFF}$	PWM−Off Threshold Voltage		9	10	11	V
V_{DD-OFF}	Turn−Off Threshold Voltage	T_A = 25°C	6.5	7.5	8.5	V
I_{DD-ST}	Startup Current	$V_{DD} = V_{DD-ON} - 0.16$ V, Gate Open	−	20	30	μA
I_{DD-OP}	Operating Current	V_{DD} = 15 V; OPFC, OPWM = 100 kHz; C_{L-PFC}, C_{L-PWM} = 2 nF	−	−	10	mA
$I_{DD-GREEN}$	Green−Mode Operating Supply Current (Average)	V_{DD} = 15 V, OPWM = 450 Hz, C_{L-PWM} = 2 nF	−	5.5	−	mA
$I_{DD-PWM-OFF}$	Operating Current at PWM−Off Phase	$V_{DD} = V_{DD-PWM-OFF} - 0.5$ V	70	120	170	μA
V_{DD-OVP}	V_{DD} Over−Voltage Protection (Auto Recovery)		23	24	25	V
$t_{VDD-OVP}$	V_{DD} OVP De−bounce Time		100	150	200	μs
$I_{DD-LATCH}$	CSPWM Pin Open Protection Latch−Up Holding Current	V_{DD} = 7.5 V	−	120	−	μA

V_{HV-MIN}	Minimum Startup Voltage on HV Pin		−	−	50	V
I_{HV}	Supply Current Drawn from HV Pin	V_{AC} = 90 V (V_{DC} = 120 V), V_{DD} = 0 V	1.3	−	−	mA
		HV = 500 V, $V_{DD} = V_{DD-OFF}$ +1 V	−	1	−	μA

$V_{VIN-UVP}$	Threshold Voltage for AC Input Under−Voltage Protection		0.95	1.00	1.05	V
$V_{VIN-RE-UVP}$	Under−Voltage Protection Reset Voltage (for Startup)		$V_{VIN-UVP}$ +0.25 V	$V_{VIN-UVP}$ +0.30 V	$V_{VIN-UVP}$ +0.35 V	V
$t_{VIN-UVP}$	Under−Voltage Protection Debounce Time					

(V_{DD} = 15 V and T_A = −40~105°C, unless otherwise noted) (continued)

V_{RATIO}	Clamp High Output Voltage Ratio (Note 4)	V_{INVH} / V_{REF},

(V_{DD} = 15 V and T_A = −40~105°C, unless otherwise noted) (continued)

t_R	PWM Gate Output Rising Time	C_L = 3 nF, V_{DD} = 12 V, 20~80%	−	80	110	ns
t_F	PWM Gate Output Falling Time	C_L = 3 nF, V_{DD} = 12 V, 20~80%	−	40	70	ns

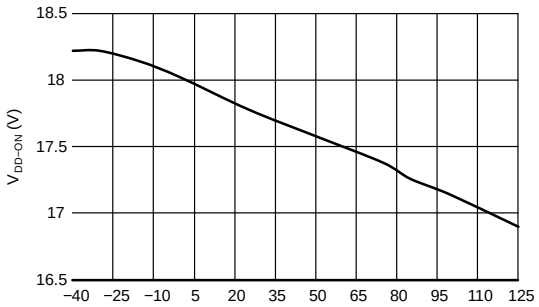
t_{PD}	Delay to Output		−	150	200	ns
V_{LIMIT}	Limit Voltage on CSPWM Pin for Over−Power Compensation	I_{DET} < 75 μA, T_A = 25°C	0.85	0.875	0.90	V
		I_{DET} = 185 μA, T_A = 25°C	0.72	0.75	0.78	
		I_{DET} = 350 μA, T_A = 25°C	0.55	0.59	0.63	
V_{SLOPE}	Slope Compensation (Note 4)	t_{ON} = 45 μs, RANGE = Open	0.25	0.30	0.35	V
		t_{ON} = 0 μs	0.05	0.10	0.15	
$t_{ON−BNK}$	Leading−Edge Blanking Time		−	300		ns
$V_{CS−FLOATING}$	CSPWM Pin Floating V_{CSPWM} Clamped High Voltage	CSPWM Pin Floating	4.5	−	5.0	V
$V_{CS−OV}$	CSPWM Pin Open Protection (Note 4)		−	3	−	V
$t_{CS−H}$	Delay with CSPWM Pin Floating	CSPWM Pin Floating	100	150	200	μs

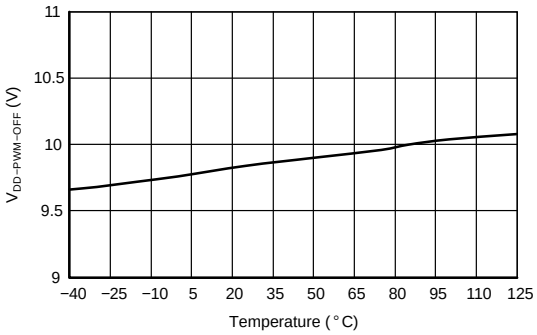
T_{OTP}	Internal Threshold Temperature for OTP (Note 4)		125	140	155	°C
$T_{OTP−HYST}$	Hysteresis Temperature for Internal OTP (Note 4)		−	30	−	°C
I_{RT}	Internal Source Current of RT Pin		90	100	110	μA
$V_{RT−REC}$	Auto Recovery−Mode Triggering Voltage		0.75	0.80	0.85	V
$V_{RT−RE−REC}$	Auto Recovery−Mode Release Voltage		$V_{RT−REC}$ +0.15	$V_{RT−REC}$ +0.20	$V_{RT−REC}$ +0.25	V
$V_{RT−OTP−LEVEL}$	Threshold Voltage for Two−level Debounce Time		0.45	0.50	0.55	V
$t_{RT−OTP−H}$	Debounce Time for OTP		−	10	−	ms
$t_{RT−OTP−L}$	Debounce Time for Externally Triggering	V_{RT} < $V_{RT−OTP−LEVEL}$, T_A = 25°C	70	115	160	μs

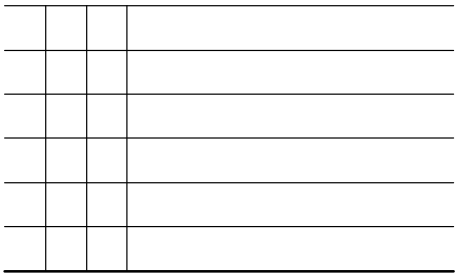
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by design.

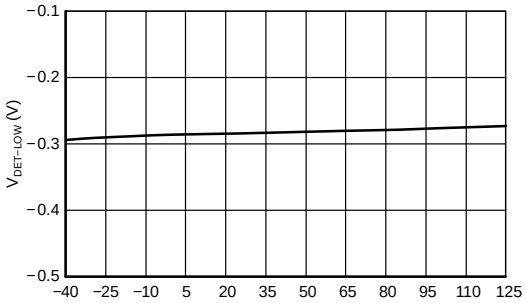
(These characteristic graphs are normalized at T_A = 25°C)

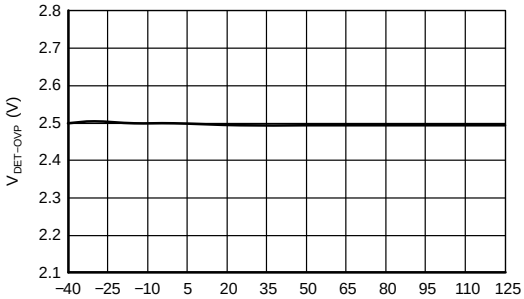






(These characteristic graphs are normalized at T_A = 25°C) (continued)



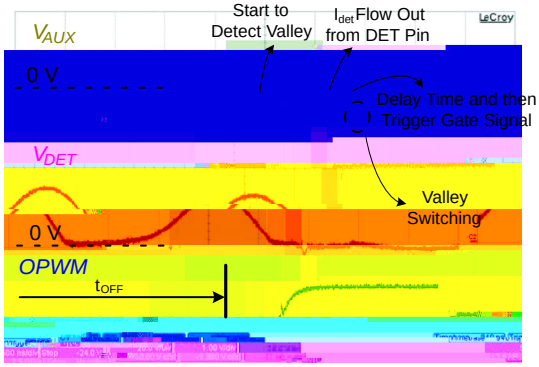


RANGE Pin

A built‐in low voltage MOSFET can be turned on or off according to V_{VIN} voltage level. The drain pin of this

HV Startup and Operating Current (HV Pin)

The HV pin is connected to the AC line through a resistor (refer to Figure 1). With a built‐in high‐voltage startup



High / Low Line Over Power Compensation (DET Pin)

Generally, when the power switch turns off, there is a delay from gate signal falling edge to power switch off. This delay is produced by an internal propagation delay of the controller and the turn‐off delay of PWM switch due to gate resistor and gate‐source capacitor C_{ISS} of PWM switch. At different AC input voltage, this delay produces different maximum output power under the same PWM current limit level. Higher input voltage generates higher maximum output power since applied voltage on primary winding is higher and causes a higher rising slope inductor current. It results in a higher peak inductor current at the same delay. Furthermore, under the same output wattage, the peak switching current at high line is lower than that at low line. Therefore, to make the maximum output power close at different input voltages, the controller needs to regulate V_{LIMIT} voltage of the CSPWM pin to control the PWM switch current.

Referring to Figure 40, during t_{ON} period of the PWM switch, the input voltage is the 5ak indu[peri7 Tm Tc0 Tw(3N)Tj1.445tage on itching is)T0 1a h.

VDD Pin Over Voltage Protection (OVP)

VDD over−voltage protection is used to prevent device damage once VDD voltage is higher than device stress rating voltage. In case of VDD OVP, the controller enters Auto Recovery Mode.

Adjustable Over Temperature Protection and Externally Latch Triggering (RT Pin)

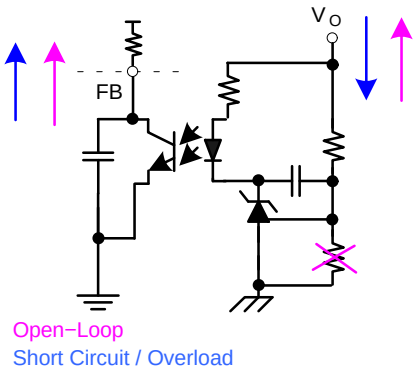
Figure 42 is a typical application circuit with an internal block of RT pin. As shown, a constant current IRT flows out from the RT pin, so the voltage VRT on RT pin can be obtained as IRT current multiplied by the resistor, which consists of NTC resistor and R_{RT} resistor. If the RT pin voltage is lower than 0.8 V and lasts for a debounce time, Auto Recovery Mode is activated.

The RT pin is usually used to achieve over−temperature protection with a NTC resistor and provide external fault triggering for additional protection. Engineers can use an external triggering circuit (e.g. transistor) to pull the RT pin LOW and activate controller Auto Recovery Mode.

Generally, the external fault triggering needs to activate

Open Loop, Short Circuit, and Overload Protection (FB Pin)

Referring to Figure 44, outside of FL7921R, the FB pin is connected to the collector of transistor of an optocoupler. Inside of FL7921R, the FB pin is connected to an internal voltage bias through a resistor of around 5 kΩ.

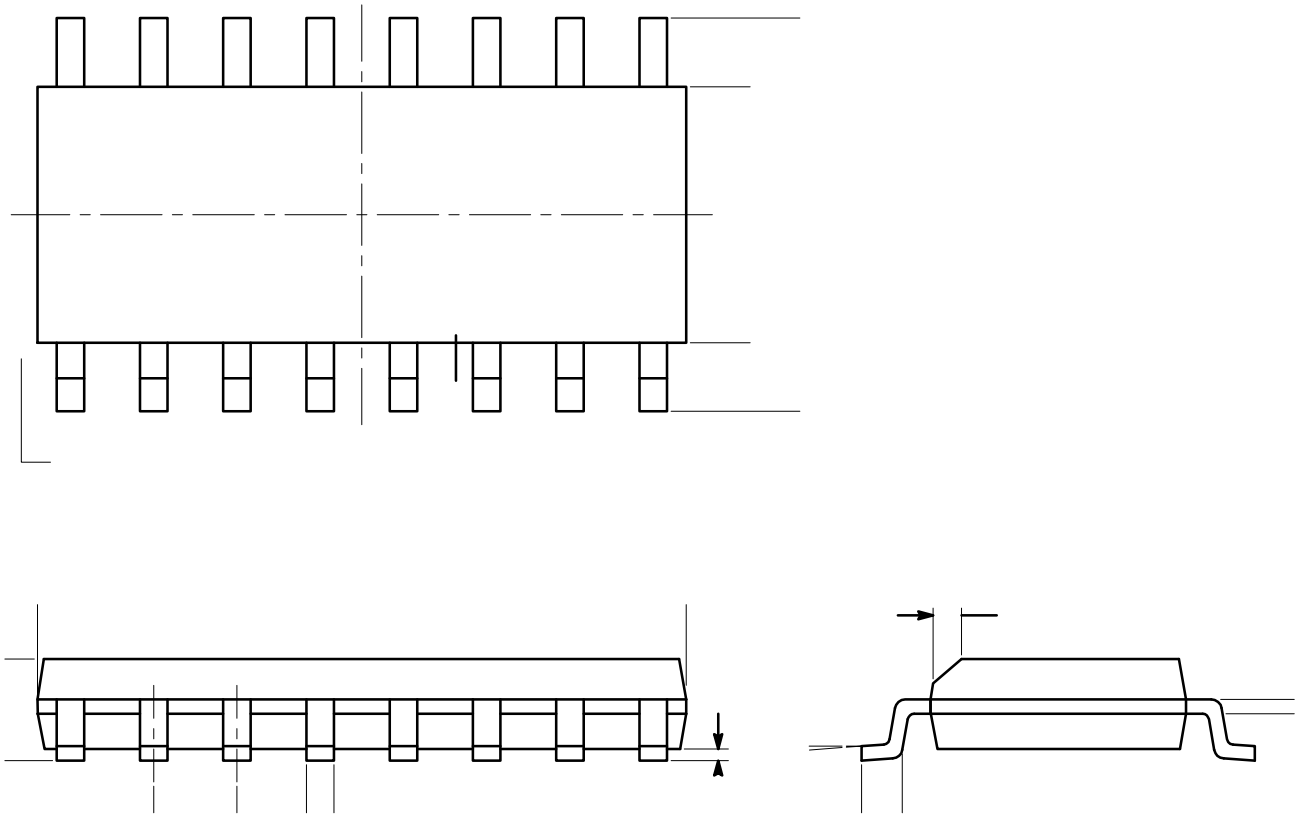


As the output loading is increased, the output voltage is decreased and the sink current of transistor of optocoupler on primary side is reduced so the FB pin voltage is increased by internal voltage bias. In the case of an open−loop, output short−circuit, or overload condition; this sink current is further reduced and the FB pin voltage is pulled to high level by internal bias voltage. When the FB pin voltage is higher than 4.2 V for 50 ms the FB pin protection is activated.

Under Voltage Lockout (UVLO, VDD Pin)

SOIC−16, 150 mils
CASE 751BG
ISSUE O

DATE 19 DEC 2006



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