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Integrated Critical-Mode PFC and Quasi-Resonant Current-Mode PWM Lightning Controller

APPLICATION DIAGRAM



Figure 1. Typical Application

INTERNAL BLOCK DIAGRAM

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CSPWM

Figure 2. Functional Block Diagram

PIN CONFIGURATION



ELECTRICAL	_ CHARACTERISTICS	$(V_{DD} = 15 \text{ V and } T_{\mu})$	_A = −40~105°C, unles	s otherwise noted)
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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DD} Section						
V _{OP}	Continuously Operating Voltage		-	-	25	V
V _{DD-ON}	Turn-On Threshold Voltage		16.5	18.0	19.5	V
V _{DD-PWM-OFF}	PWM–Off Threshold Voltage		9	10	11	V
V _{DD-OFF}	Turn–Off Threshold Voltage	$T_A = 25^{\circ}C$	6.5	7.5	8.5	V
I _{DD-ST}	Startup Current	$V_{DD} = V_{DD-ON} - 0.16 V,$ Gate Open	-	20	30	μΑ
I _{DD-OP}	Operating Current	$\label{eq:VDD} \begin{array}{l} V_{DD} = 15 \text{ V}; \text{ OPFC}, \\ \text{OPWM} = 100 \text{ kHz}; \\ \text{C}_{\text{L-PFC}}, \text{C}_{\text{L-PWM}} = 2 \text{ nF} \end{array}$	-	-	10	mA
I _{DD-GREEN}	Green–Mode Operating Supply Current (Average)	V_{DD} = 15 V, OPWM = 450 Hz, C_{L-PWM} = 2 nF	-	5.5	-	mA
I _{DD-PWM-OFF}	Operating Current at PWM–Off Phase	$V_{DD} = V_{DD-PWM-OFF}$ - 0.5 V	70	120	170	μΑ
V _{DD-OVP}	V _{DD} Over–Voltage Protection (Auto Recovery)		23	24	25	V
t _{VDD-OVP}	V _{DD} OVP De-bounce Time		100	150	200	μs
I _{DD-LATCH}	CSPWM Pin Open Protection Latch–Up Holding Current	V _{DD} = 7.5 V	-	120	_	μΑ

HV Startup Current Source Section

V _{HV-MIN}	Minimum Startup Voltage on HV Pin		_	_	50	V
I _{HV} Supply Current Drawn from HV Pin	$V_{AC} = 90 V$ ($V_{DC} = 120 V$), $V_{DD} = 0 V$	1.3	I	1	mA	
		$ HV = 500 \text{ V}, \\ V_{\text{DD}} = \text{V}_{\text{DD-OFF}} + 1 \text{ V} $	-	1	-	μΑ

VIN and RANGE Section

V _{VIN–UVP}	Threshold Voltage for AC Input Under–Voltage Protection	0.95	1.00	1.05	V
V _{VIN-RE-UVP}	Under-Voltage Protection Reset Voltage (for Startup)	V _{VIN–UVP} +0.25 V	V _{VIN–UVP} +0.30 V	V _{VIN–UVP} +0.35 V	V
	Linden Valtere Destantion Debaumen Time				

 $t_{\mathsf{VIN}-\mathsf{UVP}} \qquad \text{Under-Voltage Protection Debounce Time}$

ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V and $T_A = -40 \sim 105^{\circ}$ C, unless otherwise noted) (continued)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Voltage Error A	mplifier Section					

V _{RATIO}	Clamp High Output Voltage Ratio (Note 4)	V _{INVH} / V _{REF} ,

ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V and T_A = -40~105°C, unless otherwise noted) (continued)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
PWM Output Section						
t _R	PWM Gate Output Rising Time	C _L = 3 nF, V _{DD} = 12 V, 20~80%	-	80	110	ns
t _F	PWM Gate Output Falling Time	C _L = 3 nF, V _{DD} = 12 V, 20~80%	-	40	70	ns

Current Sense Section

t _{PD}	Delay to Output		_	150	200	ns
V _{LIMIT}	Limit Voltage on CSPWM Pin for Over–Power	$I_{DET} < 75 \ \muA, \ T_A = 25^\circC$	0.85	0.875	0.90	V
	Compensation	I _{DET} = 185 μA, T _A = 25°C	0.72	0.75	0.78	
		$I_{DET} = 350 \ \mu A, \ T_A = 25^{\circ}C$	0.55	0.59	0.63	
V _{SLOPE}	Slope Compensation (Note 4)	t _{ON} = 45 μs, RANGE = Open	0.25	0.30	0.35	V
		t _{ON} = 0 μs	0.05	0.10	0.15	
t _{ON-BNK}	Leading-Edge Blanking Time		-	300		ns
V _{CS-FLOATING}	CSPWM Pin Floating V _{CSPWM} Clamped High Voltage	CSPWM Pin Floating	4.5	-	5.0	V
V _{CS-OV}	CSPWM Pin Open Protection (Note 4)		-	3	-	V
t _{CS-H}	Delay with CSPWM Pin Floating	CSPWM Pin Floating	100	150	200	μs

RT Pin Over Temperature Protection Section

T _{OTP}	Internal Threshold Temperature for OTP (Note 4)		125	140	155	°C
T _{OTP-HYST}	Hysteresis Temperature for Internal OTP (Note 4)		-	30	-	°C
I _{RT}	Internal Source Current of RT Pin		90	100	110	μΑ
V _{RT-REC}	Auto Recovery–Mode Triggering Voltage		0.75	0.80	0.85	V
V _{RT-RE-REC}	Auto Recovery–Mode Release Voltage		V _{RT-REC} +0.15	V _{RT-REC} +0.20	V _{RT-REC} +0.25	V
V _{RT-OTP-LEVEL}	Threshold Voltage for Two-level Debounce Time		0.45	0.50	0.55	V
t _{RT-OTP-H}	Debounce Time for OTP		-	10	-	ms
t _{RT-OTP-L}	Debounce Time for Externally Triggering	$V_{RT} < V_{RT-OTP-LEVEL}, T_A = 25^{\circ}C$	70	115	160	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 4. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

(These characteristic graphs are normalized at T_A = 25°C)







Figure 6. Turn Off Threshold Voltage



Figure 5. PWM Off Threshold Voltage

Figure 7. V_{DD} Over $\,$ Voltage Protection Threshold $\,$

Figure 8. Startup Current

Figure 9. Operating Current

Figure 10. PFC Output Feedback Reference Voltage

Figure 11. PFC Gate Output Clamping Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL PERFORMANCE CHARACTERISTICS

(These characteristic graphs are normalized at T_A = 25°C) (continued)







Figure 21. Reference Voltage for Output Over Voltage Protection of DET Pin

Figure 22. Internal Source Current of RT Pin

Figure 23. Over Temperature Protection Threshold Voltage of RT Pin

RANGE Pin

A built in low voltage MOSFET can be turned on or off according to $V_{\rm VIN}$ voltage level. The drain pin of this

PWM Stage

HV Startup and Operating Current (HV Pin) The HV pin is connected to the AC line through a resistor (refer to Figure 1). With a built in high voltage startup



Figure 39. Measured Waveform of Valley Detection

High / Low Line Over Power Compensation (DET Pin)

Generally, when the power switch turns off, there is a delay from gate signal falling edge to power switch off. This delay is produced by an internal propagation delay of the controller and the turn off delay of PWM switch due to gate resistor and gate source capacitor CISS of PWM switch. At different AC input voltage, this delay produces different maximum output power under the same PWM current limit level. Higher input voltage generates higher maximum output power since applied voltage on primary winding is higher and causes a higher rising slope inductor current. It results in a higher peak inductor current at the same delay. Furthermore, under the same output wattage, the peak switching current at high line is lower than that at low line. Therefore, to make the maximum output power close at different input voltages, the controller needs to regulate VLIMIT voltage of the CSPWM pin to control the PWM switch current.

Referring to Figure 40, during t_{ON} period of the PWM switch, the input voltage is the 5ak indu[peri7 Tm Tc0 Tw(3N)Tj1.445tage on itching is)**T0** 1a h.

Protection for PWM Stage

VDD Pin Over Voltage Protection (OVP)

VDD over voltage protection is used to prevent device damage once VDD voltage is higher than device stress rating voltage. In case of VDD OVP, the controller enters Auto Recovery Mode.

Adjustable Over Temperature Protection and Externally Latch Triggering (RT Pin)

Figure 42 is a typical application circuit with an internal block of RT pin. As shown, a constant current IRT flows out from the RT pin, so the voltage VRT on RT pin can be obtained as IRT current multiplied by the resistor, which consists of NTC resistor and R_{RT} resistor. If the RT pin voltage is lower than 0.8 V and lasts for a debounce time, Auto Recovery Mode is activated.

The RT pin is usually used to achieve over temperature protection with a NTC resistor and provide external fault triggering for additional protection. Engineers can use an external triggering circuit (e.g. transistor) to pull the RT pin LOW and activate controller Auto Recovery Mode.

Generally, the external fault triggering needs to activate

Open Loop, Short Circuit, and Overload Protection (FB Pin)

Referring to Figure 44, outside of FL7921R, the FB pin is connected to the collector of transistor of an optocoupler. Inside of FL7921R, the FB pin is connected to an internal voltage bias through a resistor of around 5 k Ω .



Figure 44. FB Pin Open Loop, Short Circuit, and Overload Protection

As the output loading is increased, the output voltage is decreased and the sink current of transistor of optocoupler on primary side is reduced so the FB pin voltage is increased by internal voltage bias. In the case of an open loop, output short circuit, or overload condition; this sink current is further reduced and the FB pin voltage is pulled to high level by internal bias voltage. When the FB pin voltage is higher than 4.2 V for 50 ms the FB pin protection is activated.

Under Voltage Lockout (UVLO, VDD Pin)



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