6617

Description

This third−generation Primary Side Regulation (PSR) and highly integrated PWM controller provides several features to enhance the performance of low−power flyback converters. The proprietary TRUECURRENT® technology of FLS6617 enables precise CC regulation and simplified circuit design for battery−charger applications leading to lower−cost, smaller, and lighter chargers, compared to a conventional design or a linear transformer.

To minimize standby power consumption, the proprietary green mode provides off−time modulation to linearly decrease PWM frequency under light−load conditions. Green mode assists the power supply in meeting power conservation requirements.

By using the FLS6617, a charger can be implemented with few external components and minimized cost. A typical output CV/CC characteristic envelope is shown in Figure 1.

Features

- Low Standby Power under 30 mW
- High−Voltage Startup
- Fewest External Component Counts
- Constant−Voltage (CV) and Constant−Current (CC) Control without Secondary−Feedback Circuitry
- Green−Mode: Linearly Decreasing PWM Frequency with Cycle Skipping
- Fixed PWM Frequency at 50 kHz with Proprietary Frequency Hopping to Solve EMI Problem
- Peak−Current−Mode Control in CV Mode
- Cycle−by−Cycle Current Limiting
- V_{DD} Over−Voltage Protection with Auto Restart
- V_{DD} Under−Voltage Lockout (UVLO)
- Gate Output Maximum Voltage Clamped at 15 V
- Fixed Over−Temperature Protection with Auto Restart
- Available in the 7−Lead SOP Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Battery Chargers for Cellular Phones, Cordless Phones, PDA, Digital Cameras, Power Tools, etc.
- Replaces Linear Transformers and RCC SMPS

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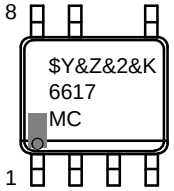
MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
6617	= Specific Device Code

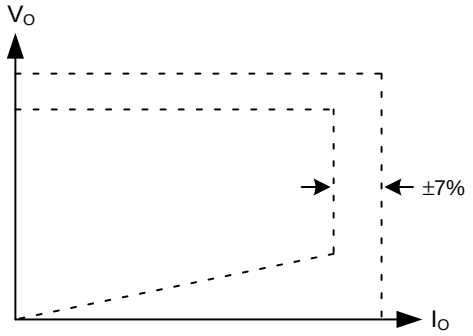


Figure 1. Typical Output V−I Characteristic

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Internal Block Diagram

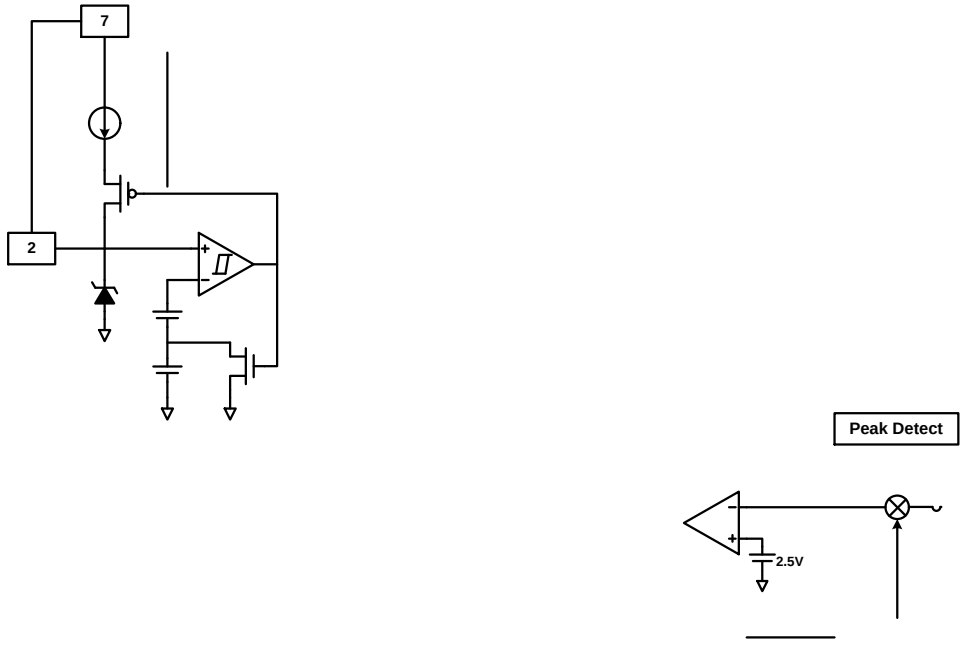


Figure 3. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Units
V_{HV}	HV Pin Input Voltage			500	V
V_{VDD}	DC Supply Voltage (1, 2)			30	V
V_{VS}	VS Pin Input Voltage		−0.3	6.0	V
V_{CS}	CS Pin Input Voltage		−0.3	6.0	V
V_{COMV}	Voltage Error Amplifier Output Voltage		−0.3	6.0	V
V_{COMI}	Current Error Amplifier Output Voltage		−0.3	6.0	V
V_{DS}	Drain−Source Voltage			700	V
I_D	Continuous Drain Current	T_A = 25°C		1	A
		T_A = 100°C		0.6	A
I_{DM}	Pulsed Drain Current			4	A
E_{AS}	Single Pulse Avalanche Energy			50	mJ
I_{AR}	Avalanche Current			1	A
P_D	Power Dissipation (T_A < 50°C)			660	mW
□JA	Thermal Resistance (Junction−to−Air)			147	°C/W
□JT	Thermal Resistance (Junction−to−Case)			11	°C/W
T_J	Operating Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature Range		−55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{DD} = 15 V and T_A = 25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD} Section						
V_{OP}	Continuously Operating Voltage				23	V
V_{DD-ON}	Turn−On Threshold Voltage		15	16	17	V
V_{DD-OFF}	Turn−Off Threshold Voltage		4.5	5.0	5.5	V
I_{DD-OP}	Operating Current			2.5	5.0	mA
$I_{DD-GREEN}$	Green−Mode Operating Supply Current			0.95	1.2	mA
V_{DD-OVP}	V_{DD} Over−Voltage−Protection Level (OVP)			24		V
$t_{D-VDDOVP}$	V_{DD} Over−Voltage−Protection Debounce Time		90	200	350	□s
HV Startup Current Source Section						
V_{HV-MIN}	Minimum Startup Voltage on HV Pin (3)				50	V
I_{HV}	Supply Current Drawn from HV Pin	V_{AC} = 90 V (V_{DC} = 100 V), V_{DD} = 0 V	1	2.0	5.0	mA
I_{HV-LC}	Leakage Current after Startup	HV = 500 V, $V_{DD}=V_{DD-OFF}+1$ V		0.5	3.0	□A
Oscillator Section						
f_{OSC}	Normal Frequency 1	Center Frequency	> Vo * 0.78	44	50	56	kHz
		Frequency Hopping Range		±1.6	±3.4	±5.2	
	Normal Frequency 2	Center Frequency	< Vo * 0.78		36		
		Frequency Hopping Range			±2.5		
$V_{F-JUM-53}$	Frequency Jumping Point		50 kHz → 36 kHz, Vs	1.75	1.95	2.15	V
$V_{F-JUM-35}$			36 kHz → 50 kHz, Vs	2.05	2.25	2.45	V
$f_{OSC-N-MIN}$	Minimum Frequency at No−Load			270	395		

ELECTRICAL CHARACTERISTICS (continued)
Unless otherwise specified, V_{DD} = 15 V and T_A = 25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_N	Green−Mode Starting Voltage on EA_V	f_{OSC} = Normal Frequency 1 − 2 kHz		2.5		V
V_G	Green−Mode Ending Voltage on EA_V	f_{OSC} = 1 kHz		0.5		V
Current Error Amplifier Section						
V_{IR}	Reference Voltage		2.475	2.500	2.525	V
Internal MOSFET Section (Note 4)						
DCY_{MAX}	Maximum Duty Cycle		60	75	85	%V

TYPICAL PERFORMANCE CHARACTERISTICS

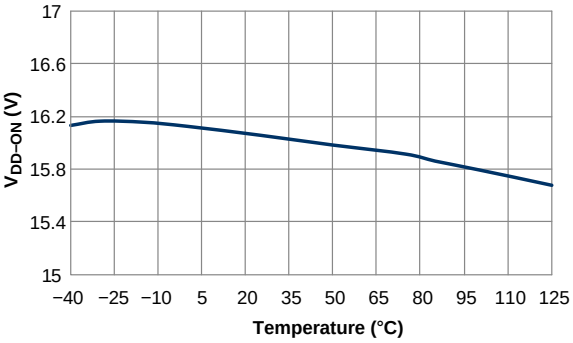


Figure 5. Turn−on Threshold Voltage (V_{DD-ON}) vs. Temperature

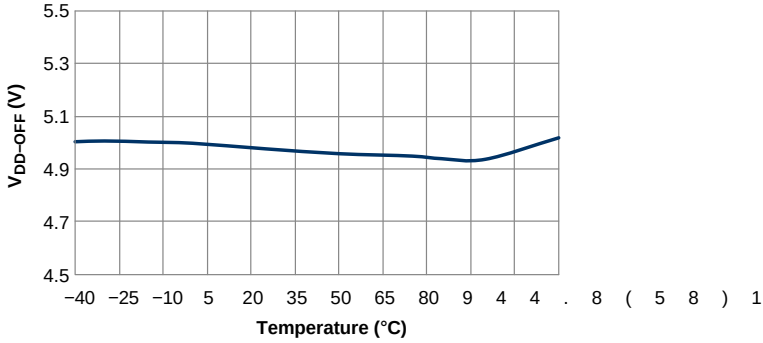


Figure 6. Turn−off Threshold Voltage (V_{DD-OFF}) vs. Temperature

Functional Description

Figure 20 shows the basic circuit diagram of primaryside regulated flyback converter, with typical waveforms shown

Operating Current

The FLS6617 operating current is as small as 2.5 mA, which results in higher efficiency and reduces the V_{DD} hold−up capacitance requirement. Once FLS6617 enters “deep” green mode, the operating current is reduced to 0.95 mA, assisting the power supply in meeting power conservation requirements.

Green−Mode Operation

The FLS6617 uses voltage regulation error amplifier output (V_{COMV}) as an indicator of the output load and modulates the PWM frequency as shown in Figure 22. The switching frequency decreases with cycle skipping as the load decreases. In heavy load conditions, the switching frequency is fixed at 50 kHz. Once V_{COMV} decreases below V_N, the PWM frequency linearly decreases with cycle skipping from 50 kHz to reduce switching losses.

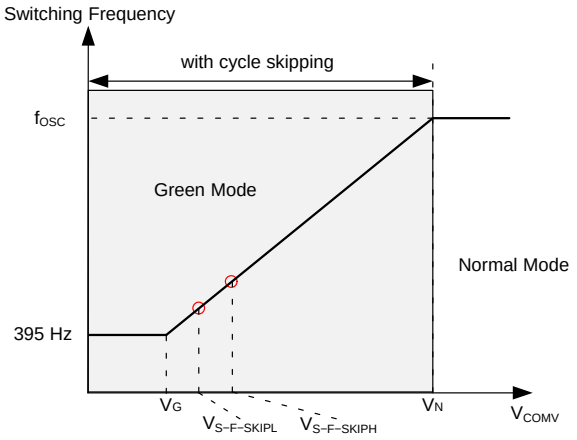


Figure 22. Switching Frequency in Green Mode

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. FLS6617 has a proprietary internal frequency hopping circuit that changes the switching frequency between 44 kHz and 56 kHz.

High−Voltage Startup

Figure 23 shows the HV−startup circuit for FLS6617 applications. The HV pin is connected to the line input or bulk capacitor through a resistor, R_{START} (100 k□ recommended). During startup status, the internal startup circuit is enabled. Meanwhile, line input supplies the current, $I_{STARTUP}$, to charge the hold−up capacitor, CDD, through R_{START}. When the V_{DD} voltage reaches V_{DDON}, the internal startup circuit is disabled, blocking $I_{STARTUP}$ from flowing into the HV pin. Once the IC turns on, C_{DD} is the only energy source to supply the IC consumption current before the PWM starts to switch. Thus, C_{DD} must be large enough to prevent V_{DD} from dropping down to $V_{DD−OFF}$ before the power can be delivered from the auxiliary winding.

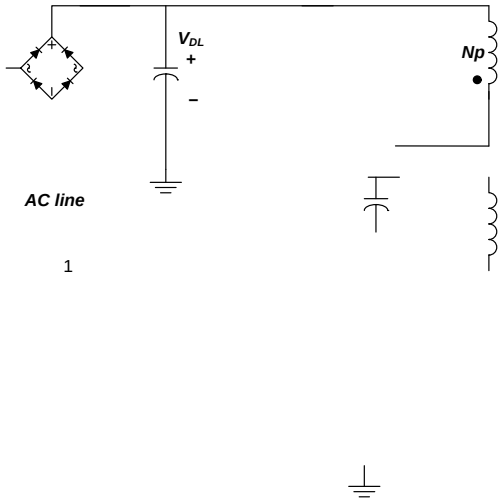


Figure 23. HV Startup Circuit

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