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www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

August 2011

FMS6143A
Three-Channel 6th-Order Standard-Definition VoltagePlus™ Video Filter Driver

Features

- Three 6th-Order 8MHz (SD) Filter
- Drives Single AC- or DC-Coupled Video Loads (150Ω)
- Transparent Input Clamping
- Single Supply: 3.3V
- AC- or DC-Coupled Inputs and Outputs
- DC-Coupled Output Eliminates AC-Coupling Capacitor
- Robust 8.5kV ESD Protection
- Supply Voltage Range: 3.3V to 5.0V
- Lead-Free SOIC-8 Package

Applications

Cab96 T.e

(see Applications section for details).

The outputs can drive AC- or DC-coupled single (150Ω) or dual (75Ω) video loads. DC coupling the outputs removes the need for large output coupling capacitors. The input DC levels are offset approximately +280mV at the output *(see Applications section for details)*.

Related Applications Notes

AN-6024 – FMS6xxx Product Series Understanding Analog Video Signal Clamps, Bias, DC Restore, and AC or DC coupling Methods

AN-6041 – PCB Layout Considerations for Video Filter / Drivers

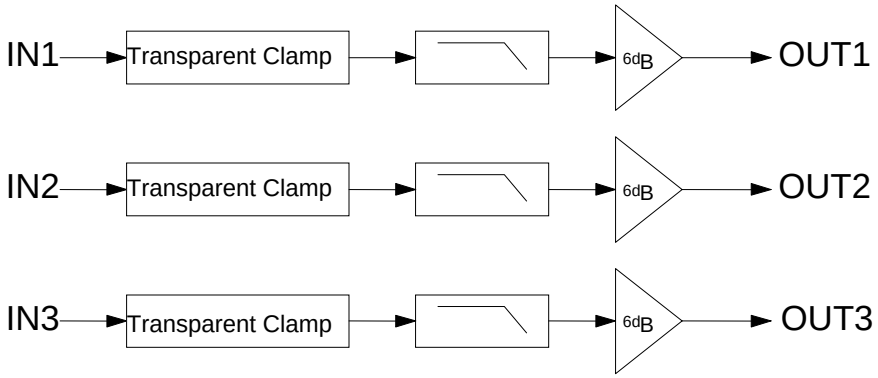


Figure 1. Block Diagram

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method	Quantity
FMS6143ACSX	-40°C to +85°C	8-Lead, Small Outline Integrated Circuit (SOIC)	Reel	5000

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_S	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC}+0.3	V
V_{OUT}	Maximum Output Current, Do Not Exceed		50	mA

Electrostatic Discharge Information

Symbol	Parameter	Min.	Unit
ESD	Human Body Model, JESD22-A114	8.5	kV
	Charged Device Model, JESD22-C101	2.0	

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
$_{JA}$	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		115		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
V_{CC}	Supply Voltage Range	3.14	3.30	5.25	V

DC Electrical Characteristics

Unless otherwise noted; T_A=25°C, V_{CC}=3.3V, R_S=37.5Ω; all inputs are AC coupled with 0.1µF; and all outputs are AC coupled with 220µF into 150Ω load.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_S	Supply Voltage Range	V_S Range	3.14	3.30	5.25	V
I_{CC}	Quiescent Supply Current(1)	V_S=+3.3V, No Load		15	22	mA
		V_S=+5.0V, No Load		19	24	mA
V_{IN}	Video Input Voltage Range	Referenced to GND if DC Coupled		1.4		V_{pp}
PSRR	Power Supply Rejection Ratio	DC (All Channels)		-65		dB

Note:
1. 100% tested at T_A=25°C.

AC Electrical Characteristics

Unless otherwise noted; T_A=25°C, V_{CC}=3.3V, R

Typical Performance Characteristics

Unless otherwise noted, T_A = 25°C, V_{CC} = 3.3V, R_S = 37.5Ω, and AC-coupled output into 150Ω load.

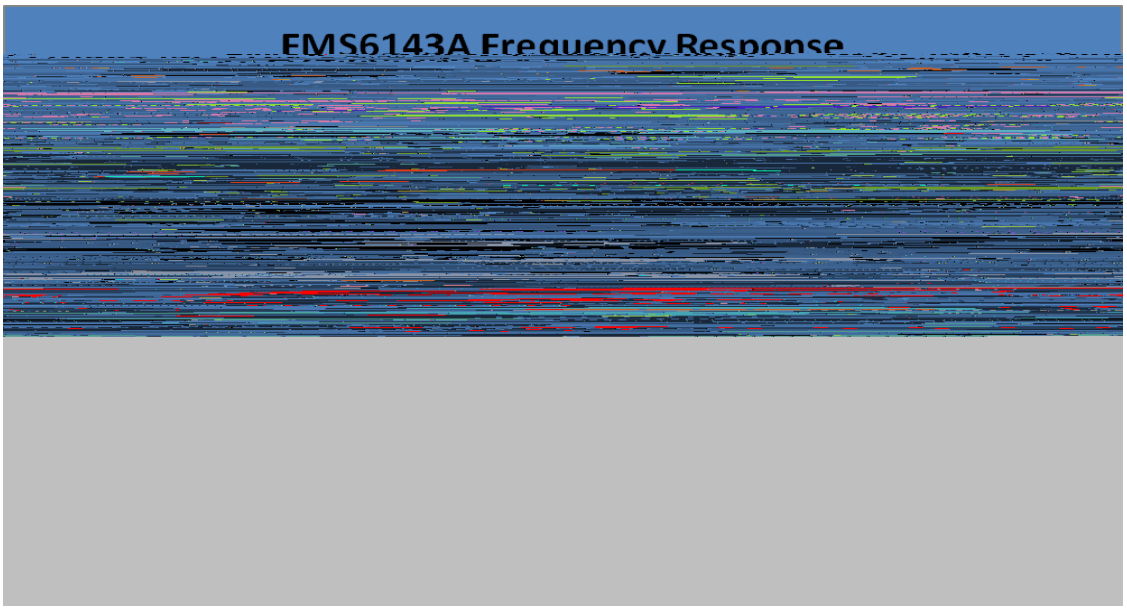


Figure 3. Frequency Response

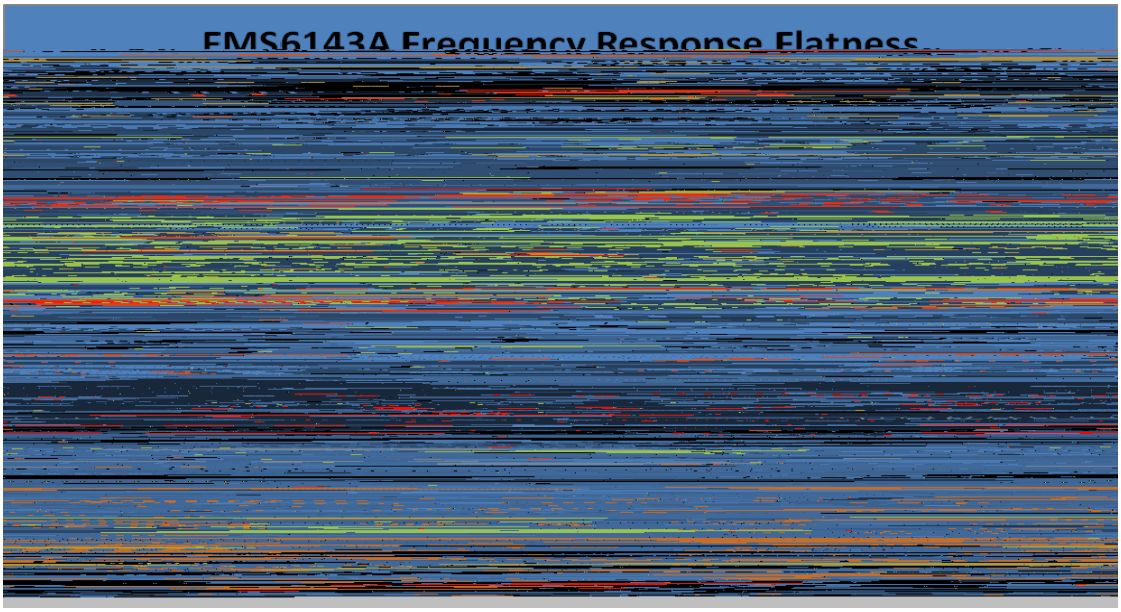


Figure 4. Frequency Response Flatness

Typical Performance Characteristics

Unless otherwise noted, T_A = 25°C, V_{CC} = 3.3V, R_S = 37.5Ω, and AC-coupled output into 150Ω load.

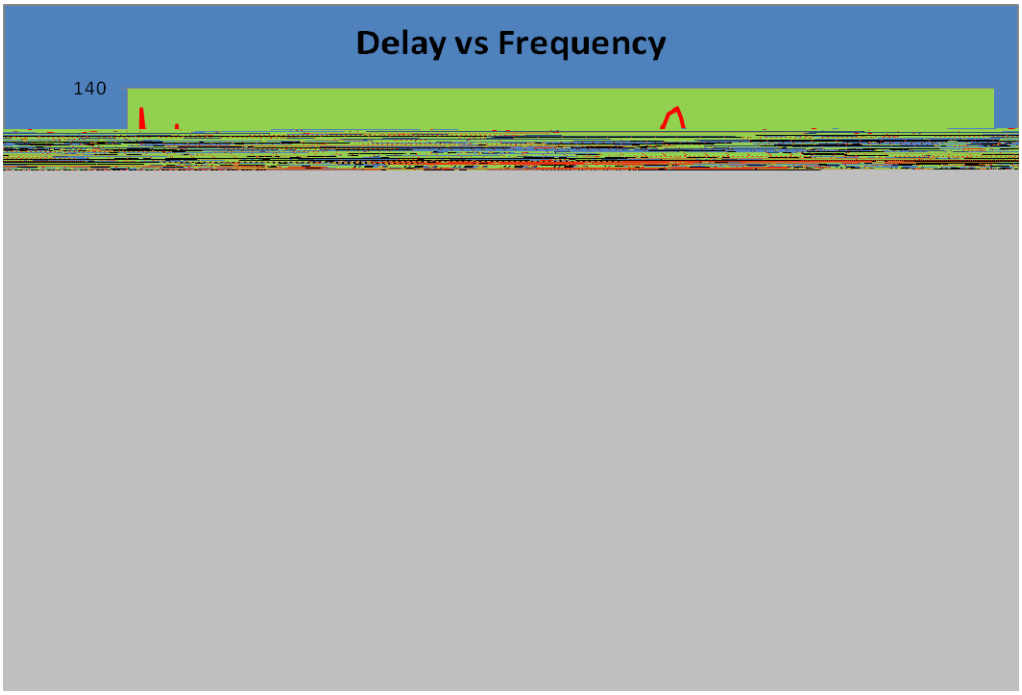


Figure 5. Delay vs. Frequency

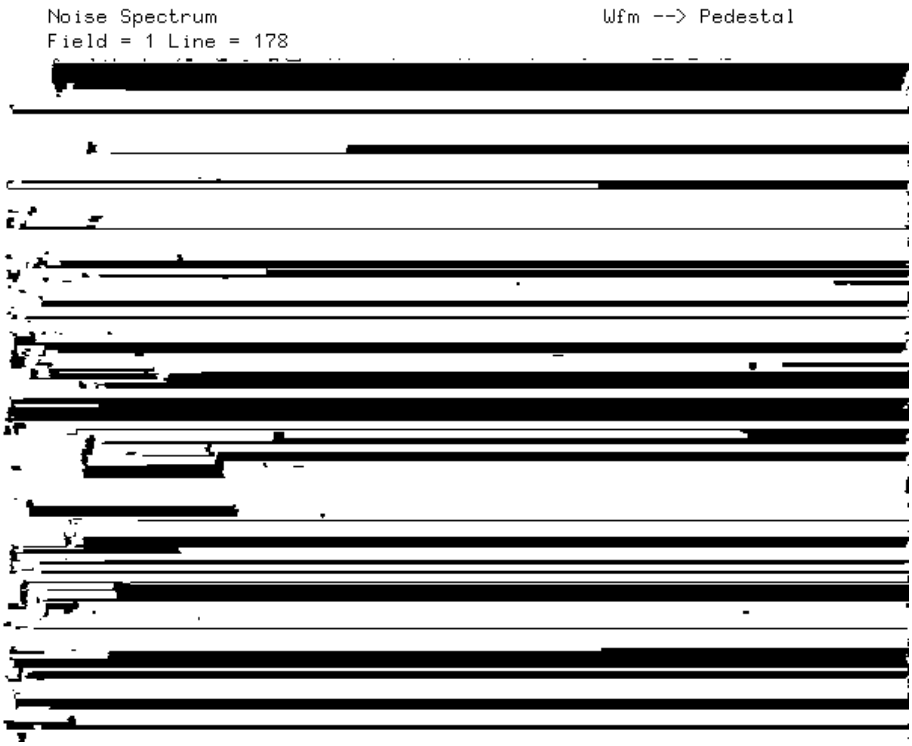


Figure 6. Noise vs. Frequency

Typical Performance Characteristics

Unless otherwise noted, T_A = 25°C, V_{CC} = 3.3V, R_S = 37.5Ω, and AC-coupled output into 150Ω load.

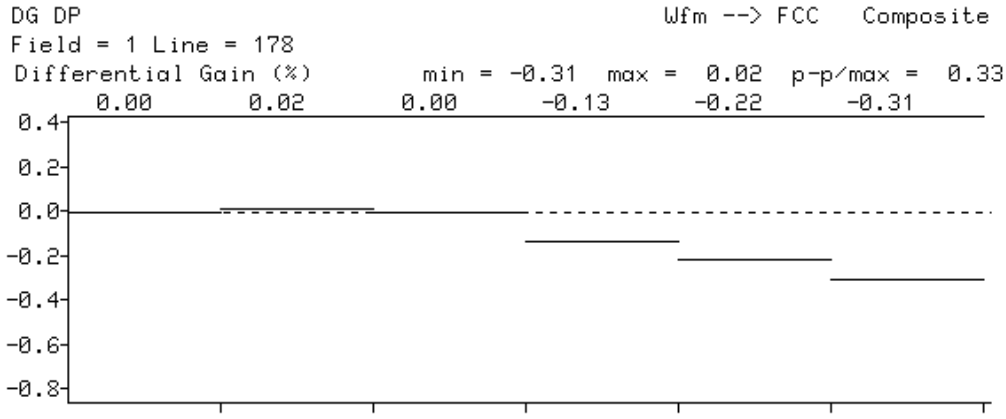


Figure 7. Differential Gain

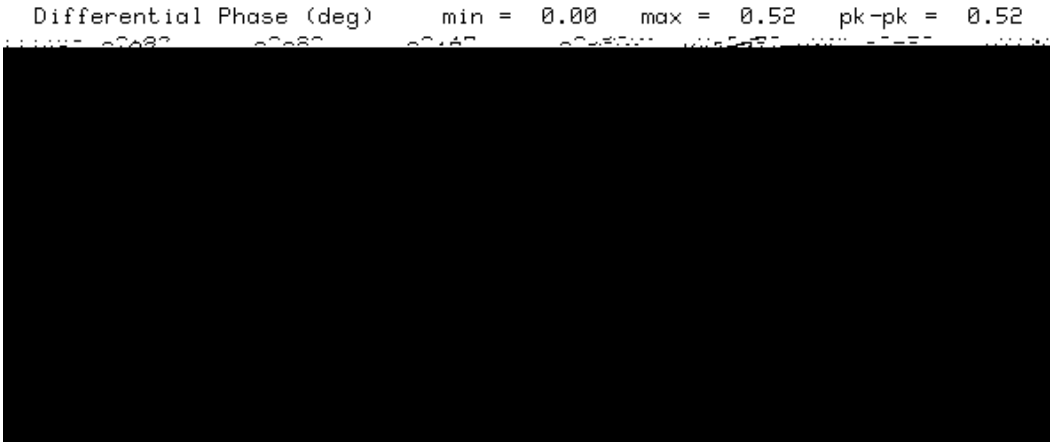


Figure 8. Differential Phase

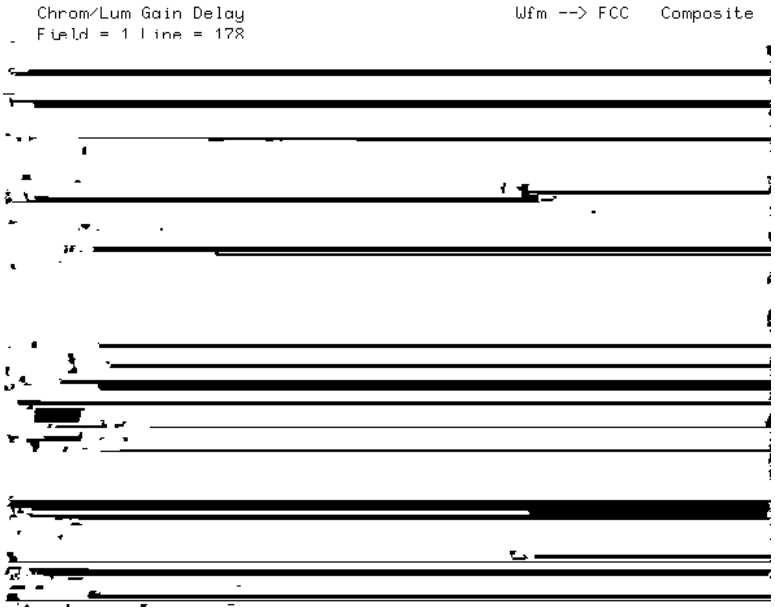
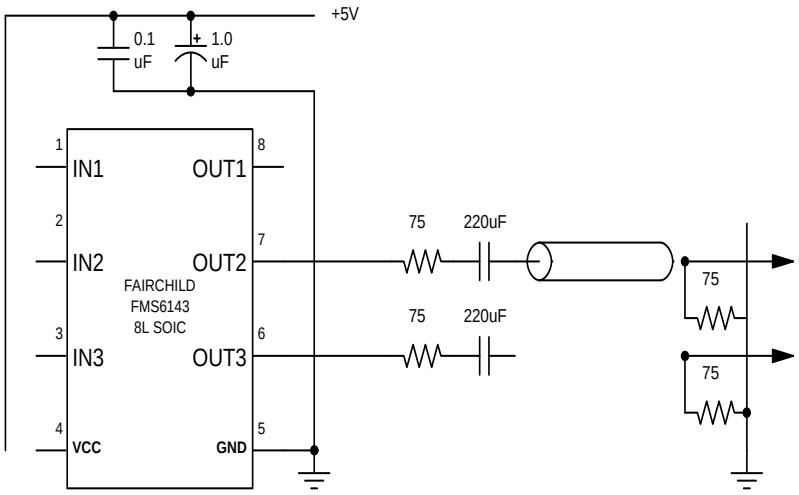


Figure 9. Chroma / Luma Gain & Delay

Applications Information



Application Information

The same method can be used for biased signals, with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is 800kΩ

Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board to guide layout and aide device evaluation. The demo board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

Recommended Routing/Layout Rules

Do not run analog and digital signals in parallel.

Use separate analog and digital power planes to supply power.

Traces should run on top of the ground plane at all times.

No trace should run over ground/power splits.

Avoid routing at 90-degree angles.

Minimize clock and video data trace length differences.

Include 10µF and 0.1µF ceramic power supply bypass capacitors.

Place the 0.1µF capacitor within 2.54mm (0.1in) of the device power pin.

Place the 10µF capacitor within 19.05mm (0.75in) of the device power pin.

For multi-layer boards, use a large ground plane to help dissipate heat.

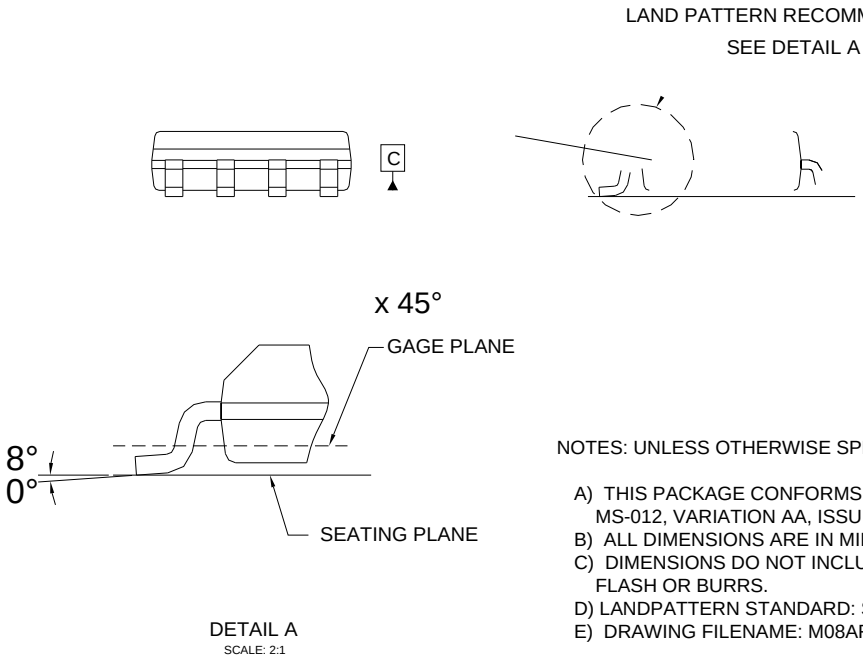
For two-layer boards, use a ground plane that extends beyond the device body at least 12.7mm (0.5in) on all sides. Include a metal paddle under the device on the top layer.

Minimize all trace lengths to reduce series inductance.

Output Considerations

The FMS6143A outputs are DC offset from the input by 150mV; therefore, V_{OUT} = 2 x V_{IN} DC + 150mV. This offset is required to obtain optimal performance from the

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
E) DRAWING FILENAME: M08AREV13

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