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# FMS6143A

## Three-Channel 6<sup>th</sup>-Order Standard-Definition VoltagePlus™ Video Filter Driver

### Features

- Three 6<sup>th</sup>-Order 8MHz (SD) Filter
- Drives Single AC- or DC-Coupled Video Loads (150 )
- Transparent Input Clamping
- Single Supply: 3.3V
- AC- or DC-Coupled Inputs and Outputs
- DC-Coupled Output Eliminates AC-Coupling Capacitor
- Robust 8.5kV ESD Protection
- Supply Voltage Range: 3.3V to 5.0V
- Lead-Free SOIC-8 Package

(see Applications section for details).

The outputs can drive AC- or DC-coupled single (150 ) or dual (75 ) video loads. DC coupling the outputs removes the need for large output coupling capacitors. The input DC levels are offset approximately +280mV at the output (see Applications section for details).

### Applications

Cab96 T.e

### Related Applications Notes

[AN-6024 – FMS6xxx Product Series Understanding Analog Video Signal Clamps, Bias, DC Restore, and AC or DC coupling Methods](#)

[AN-6041 – PCB Layout Considerations for Video Filter / Drivers](#)

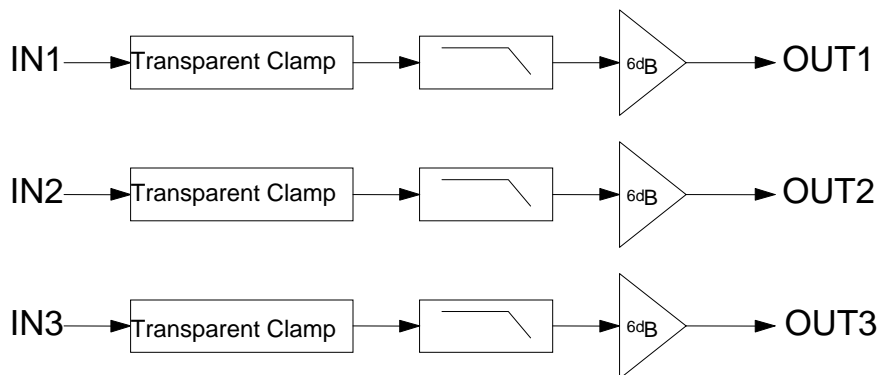
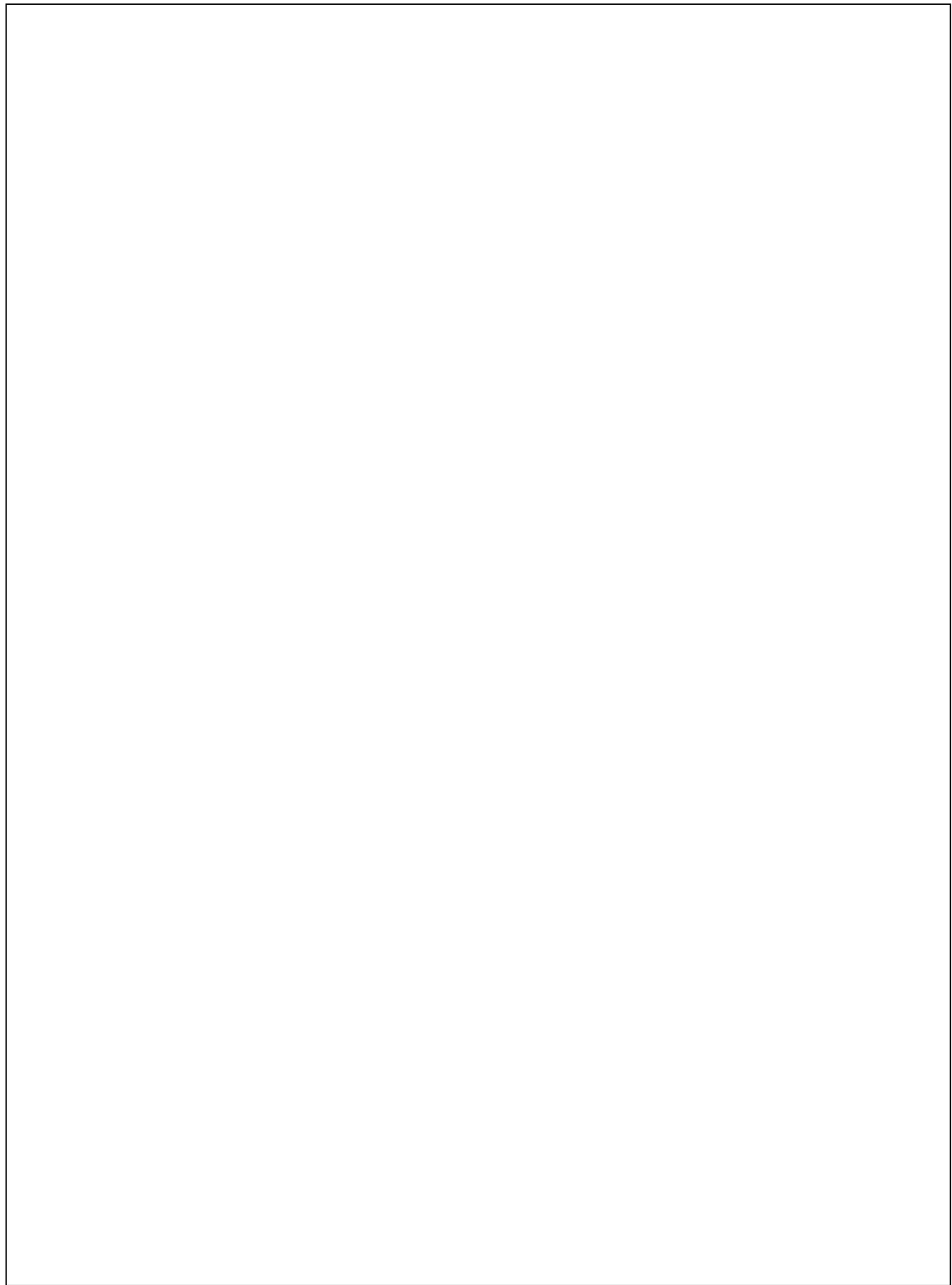


Figure 1. Block Diagram

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method	Quantity
FMS6143ACSX	-40°C to +85°C	8-Lead, Small Outline Integrated Circuit (SOIC)	Reel	5000



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_S$	DC Supply Voltage	-0.3	6.0	V
$V_{IO}$	Analog and Digital I/O	-0.3	$V_{CC}+0.3$	V
$V_{OUT}$	Maximum Output Current, Do Not Exceed		50	mA

## Electrostatic Discharge Information

Symbol	Parameter	Min.	Unit
ESD	Human Body Model, JESD22-A114	8.5	kV
	Charged Device Model, JESD22-C101	2.0	

## Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_J$	Junction Temperature			+150	°C
$T_{STG}$	Storage Temperature Range	-65		+150	°C
$J_A$	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		115		°C/W

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_A$	Operating Temperature Range	-40		+85	°C
$V_{CC}$	Supply Voltage Range	3.14	3.30	5.25	V

## DC Electrical Characteristics

Unless otherwise noted;  $T_A=25^\circ\text{C}$ ,  $V_{CC}=3.3\text{V}$ ,  $R_S=37.5\ \Omega$ ; all inputs are AC coupled with  $0.1\ \mu\text{F}$ ; and all outputs are AC coupled with  $220\ \mu\text{F}$  into  $150\ \Omega$  load.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_S$	Supply Voltage Range	$V_S$ Range	3.14	3.30	5.25	V
$I_{CC}$	Quiescent Supply Current <sup>(1)</sup>	$V_S=+3.3\text{V}$ , No Load		15	22	mA
		$V_S=+5.0\text{V}$ , No Load		19	24	mA
$V_{IN}$	Video Input Voltage Range	Referenced to GND if DC Coupled		1.4		$V_{pp}$
PSRR	Power Supply Rejection Ratio	DC (All Channels)		-65		dB

### Note:

- 100% tested at  $T_A=25^\circ\text{C}$ .

## AC Electrical Characteristics

Unless otherwise noted;  $T_A=25^\circ\text{C}$ ,  $V_{CC}=3.3\text{V}$ , R

## Typical Performance Characteristics

Unless otherwise noted,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V}$ ,  $R_S = 37.5 \Omega$ , and AC-coupled output into  $150 \Omega$  load.

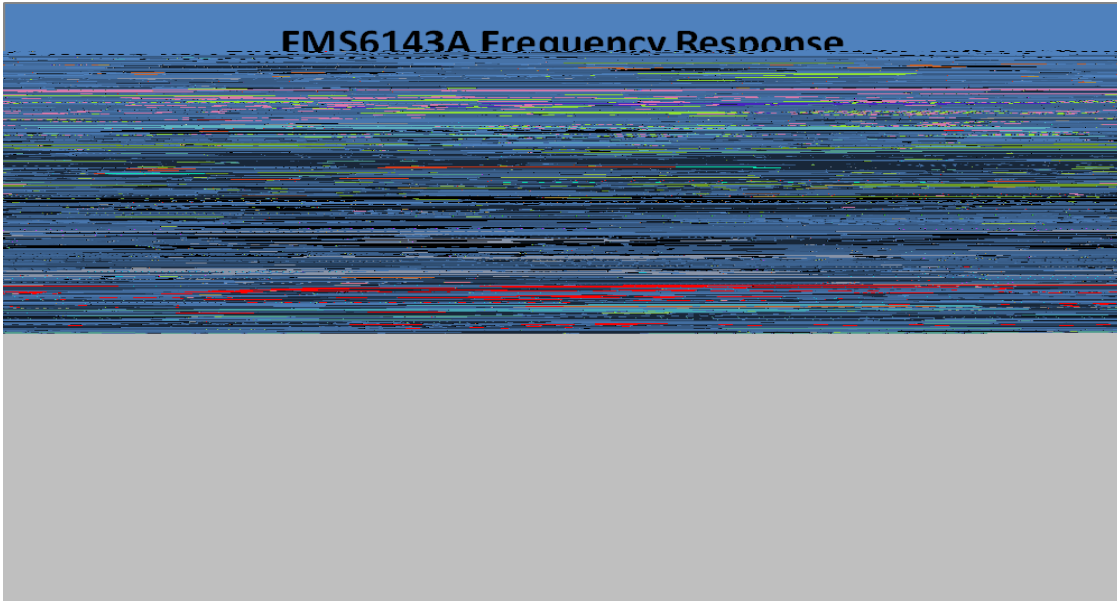


Figure 3. Frequency Response

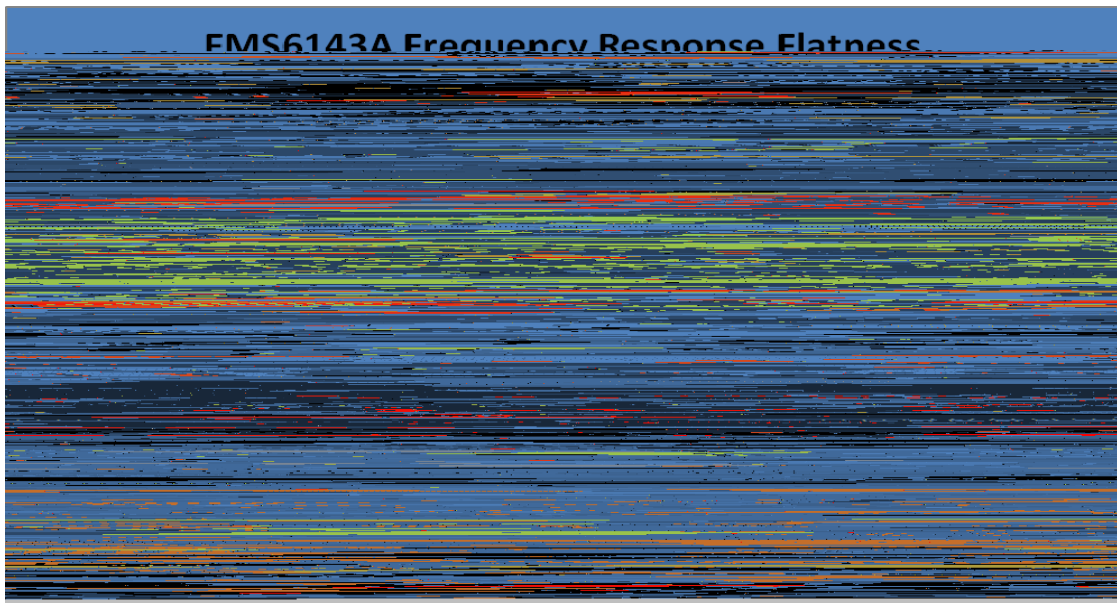


Figure 4. Frequency Response Flatness

## Typical Performance Characteristics

Unless otherwise noted,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V}$ ,  $R_S = 37.5 \Omega$ , and AC-coupled output into 150  $\Omega$  load.

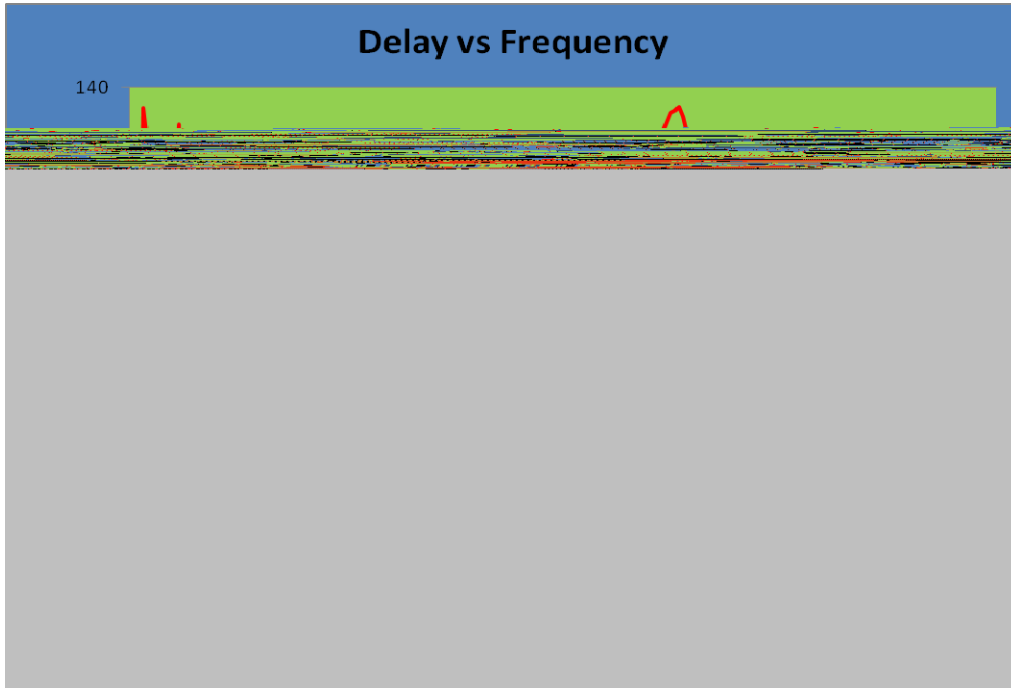


Figure 5. Delay vs. Frequency

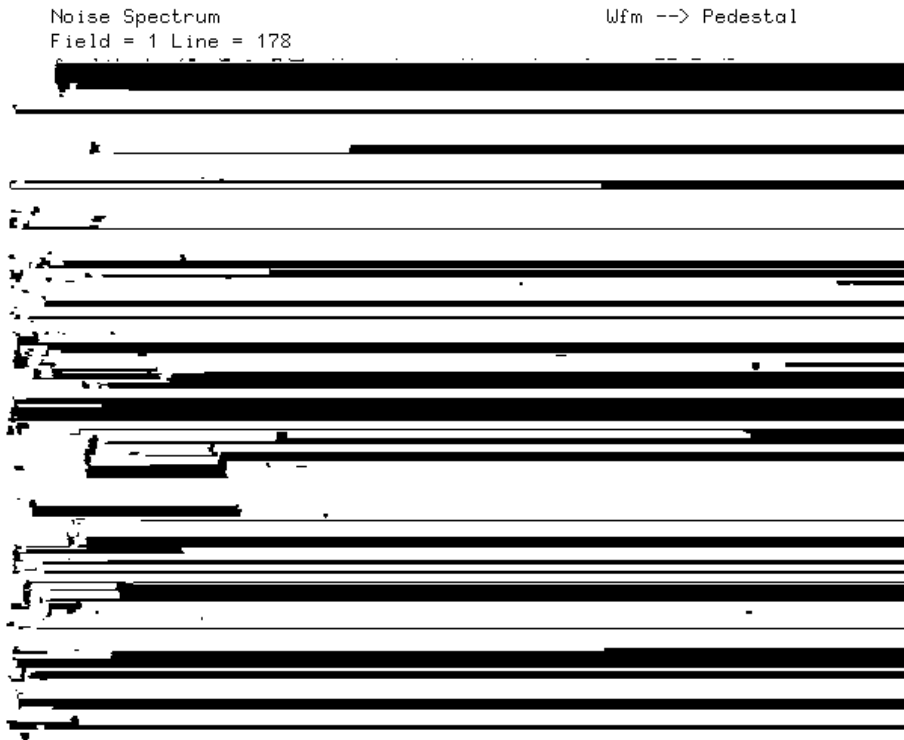


Figure 6. Noise vs. Frequency

## Typical Performance Characteristics

Unless otherwise noted,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V}$ ,  $R_S = 37.5 \Omega$ , and AC-coupled output into 150  $\Omega$  load.

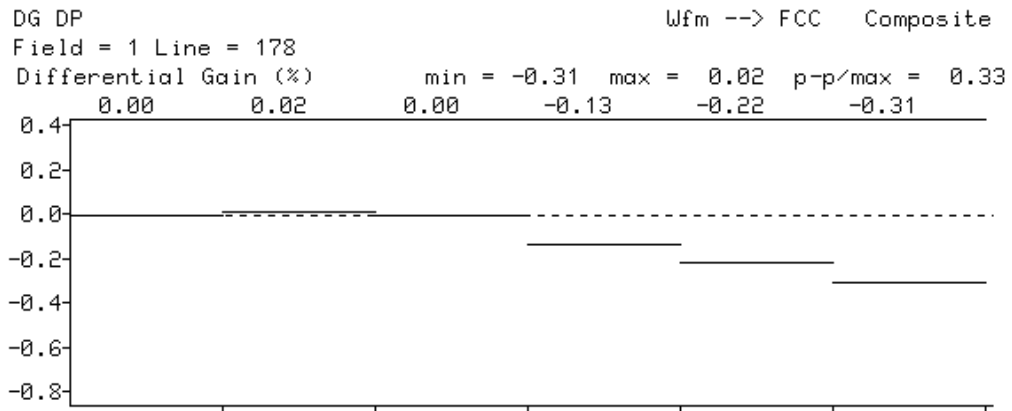


Figure 7. Differential Gain

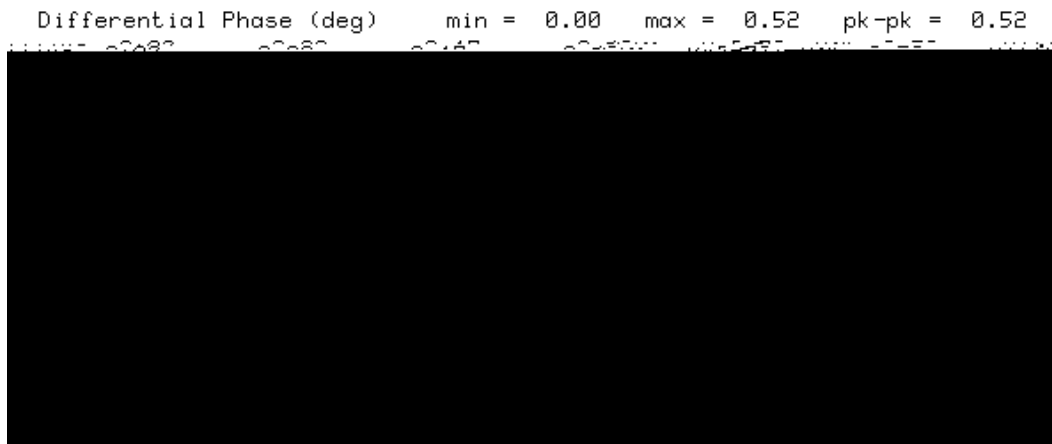


Figure 8. Differential Phase

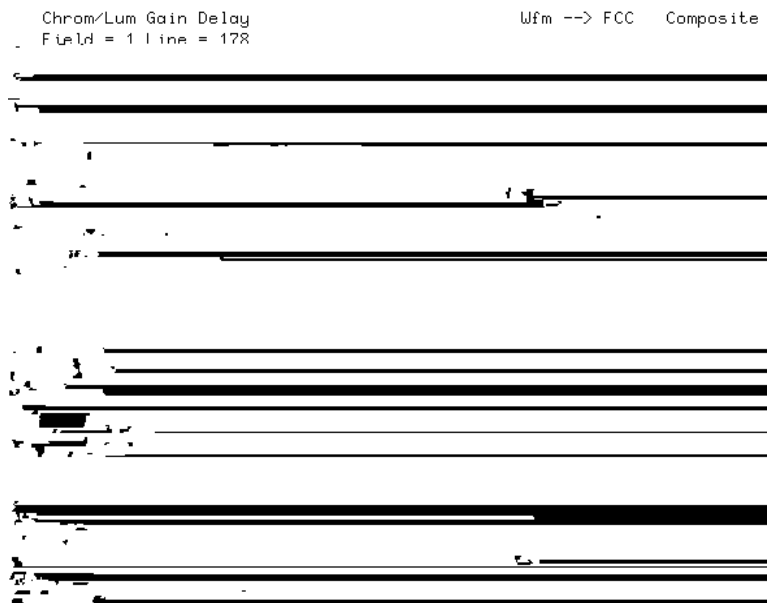
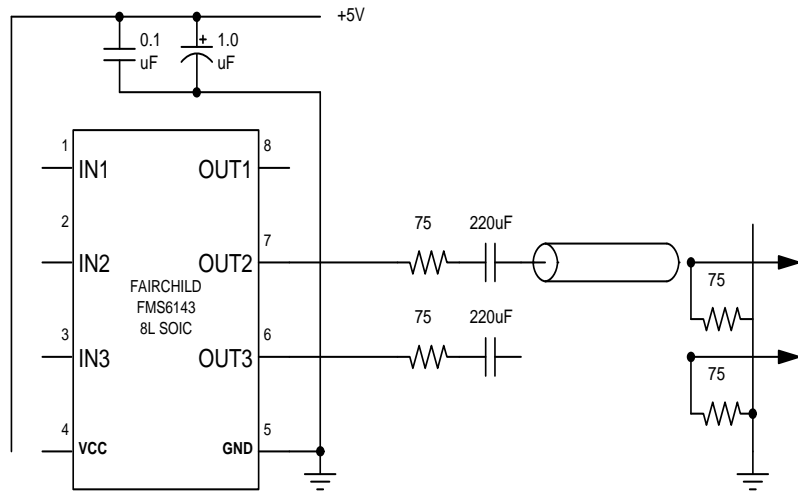


Figure 9. Chroma / Luma Gain & Delay



# Applications Information



## Application Information

The same method can be used for biased signals, with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is 800k

## Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board to guide layout and aid device evaluation. The demo board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

### Recommended Routing/Layout Rules

Do not run analog and digital signals in parallel.

Use separate analog and digital power planes to supply power.

Traces should run on top of the ground plane at all times.

No trace should run over ground/power splits.

Avoid routing at 90-degree angles.

Minimize clock and video data trace length differences.

Include 10 $\mu$ F and 0.1 $\mu$ F ceramic power supply bypass capacitors.

Place the 0.1 $\mu$ F capacitor within 2.54mm (0.1in) of the device power pin.

Place the 10 $\mu$ F capacitor within 19.05mm (0.75in) of the device power pin.

For multi-layer boards, use a large ground plane to help dissipate heat.

For two-layer boards, use a ground plane that extends beyond the device body at least 12.7mm (0.5in) on all sides. Include a metal paddle under the device on the top layer.

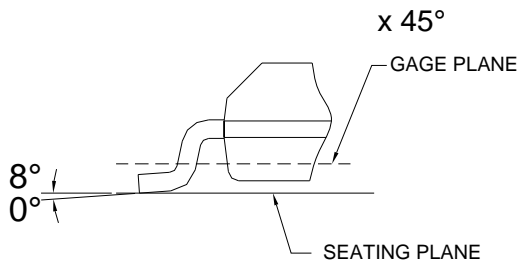
Minimize all trace lengths to reduce series inductance.

### Output Considerations

The FMS6143A outputs are DC offset from the input by 150mV; therefore,  $V_{OUT} = 2 \times V_{IN\ DC} + 150mV$ . This offset is required to obtain optimal performance from the

Physical Dimensions

LAND PATTERN RECOMMENDATION  
SEE DETAIL A



DETAIL A  
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

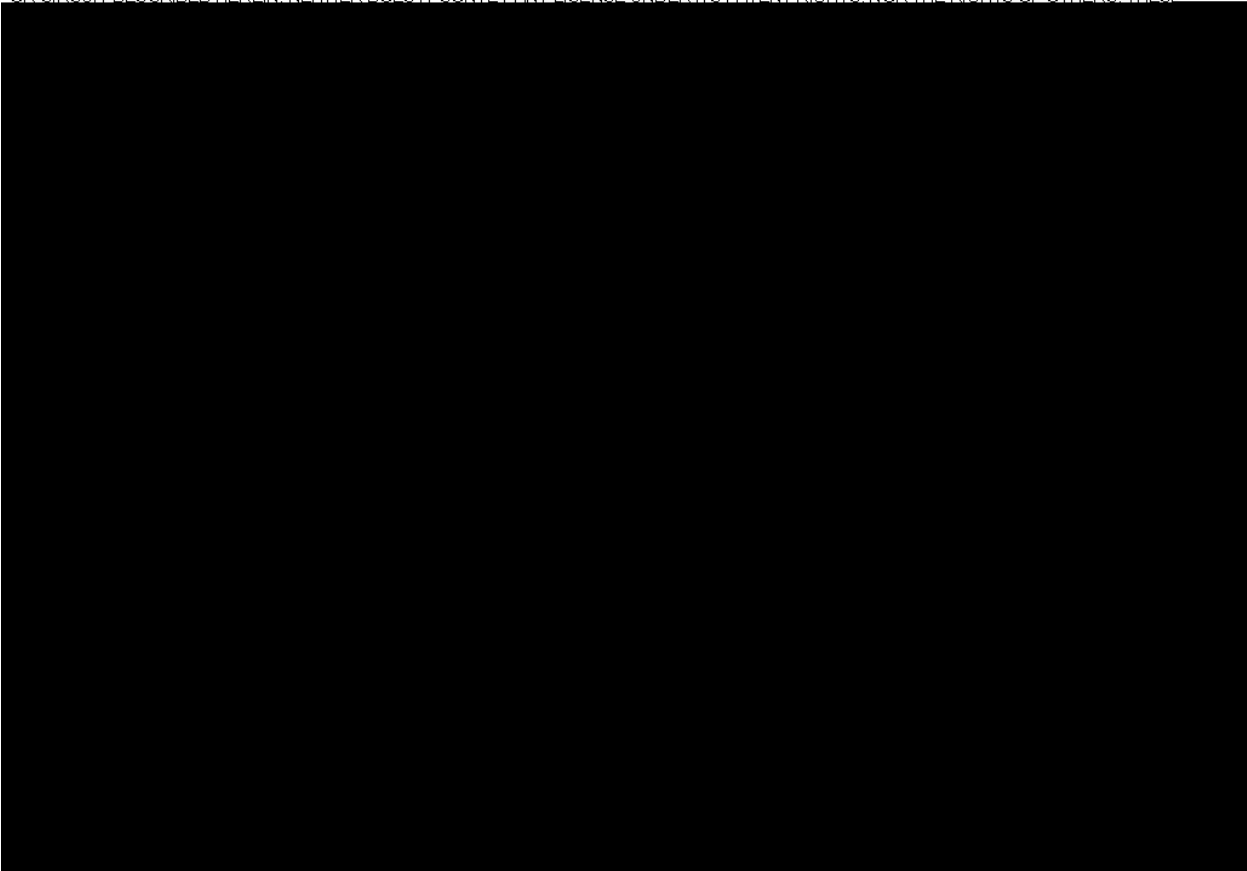
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
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- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
- E) DRAWING FILENAME: M08AREV13



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