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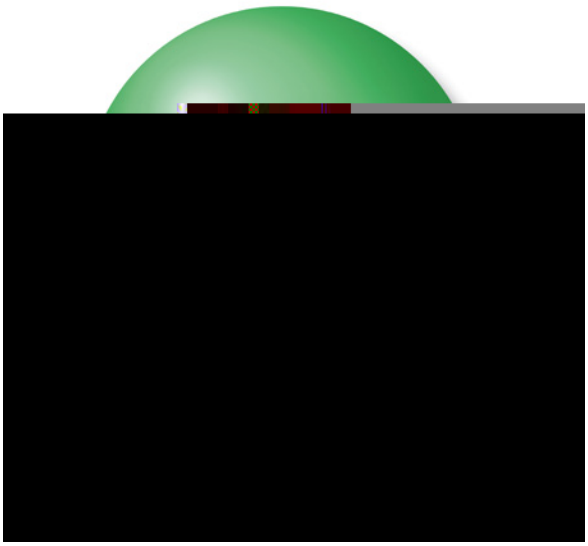

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended.

DC Electrical Characteristics

T_A=25°C, V_{CC} 5 V, V_{IN} = 1 V_{pp}, input bias mode, one-to-one routing, 6 dB gain, all inputs AC coupled with 0.1 µF, unused inputs AC-terminated through 75 Ω to GND, all outputs AC coupled with 220 ΩF into 150 Ω loads, referenced

Applications Information

Digital Interface

The I^2C-compatible interface is used to program output enables, input-to-output routing, input clamp / bias, and output gain. The I^2C address is 0x06 (0000 0110) with the ability to offset it to 0x86 (1000 0110) by tying the ADDR pin HIGH.

Both data and address data, of eight bits each, are written to the I^2C address to access control functions.

There are separate internal addresses for each output. Each output's address includes bits to select an input channel, adjust the output gain, and enable or disable the output amplifier. More than one output can select the same input channel for one-to-many routing. When the outputs are disabled, they are placed in a high-impedance state. This allows multiple FMS6501A devices to be paralleled to create a larger switch matrix. Typical output power-up time is less than 500 ns.

The clamp / bias control bits are written to their own internal addresses, since they should always remain the same regardless of signal routing. They are set based on the input signal connected to the FMS6501A.

All undefined addresses may be written without effect.

Table 1. Output Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
Enable	1 Bit	Write	0	7	Channel Enable: 1=Enable, 0=Power Down(6)
Gain	2 Bits	Write	0	6:5	Channel Gain: 00=6dB, 01=7dB, 10=8dB, 11=9dB
Inx	5 Bits	Write	0	4:0	Input Selected to Drive this Output: 00000=OFF(7), 00001=IN1, 00010=IN2... 01100=IN12

Notes:

6. Power down places the output in a high-impedance state so multiple FMS6501 devices may be paralleled. Power down also de-selects any input routed to the specified output.
7. When all inputs are OFF, the amplifier input is tied to approximately 150 mV and the output goes to approximately 300 mV with the 6 dB gain setting.

Table 2. Output Control Register MAP

Register Name	Register Address	Bit 7	Bit 6	Bit5	Bit4(8)	Bit3	Bit2	Bit1	Bit0
OUT1	0x01	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT2	0x02	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT3	0x03	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT4	0x04	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT5	0x05	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT6	0x06	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT7	0x07	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0

Table 4. semi.com

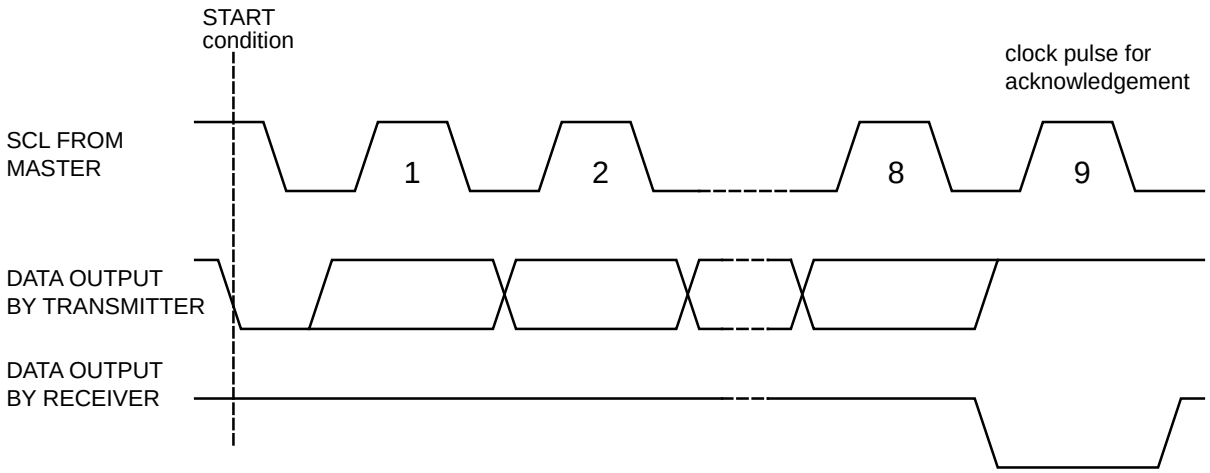

Figure 6. Acknowledgement on the I²C Bus®

I²C Bus Protocol

Before any data is transmitted on the I²C Bus, the device that should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The I²C bus configuration for a data write to the FMS6501 is shown in Figure 7.

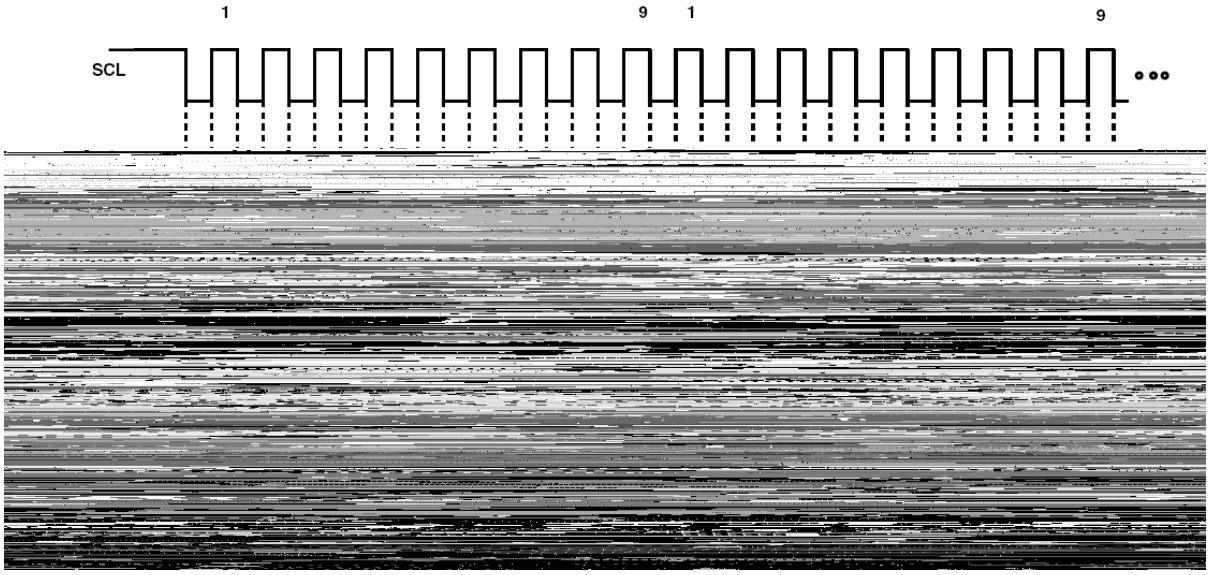

Figure 7. Write a Register Address to the Pointer Register, Then Write Data to the Selected Register

Applications Information

Input Clamp / Bias Circuitry

The FMS6501A accommodates AC- or DC-coupled inputs. Internal clamping and bias circuitry are provided to support AC-coupled inputs. These are selectable through the CLMP bits via the I^2C compatible interface.

For DC-coupled inputs, the device should be programmed to use the bias input configuration. In this configuration, the input is internally biased to 625 mV through a 100 kΩ resistor. Distortion is optimized with the output levels set between 250 mV above ground and 500 mV below the power supply. These constraints, along with the desired channel gain, need to be considered when configuring the input signal levels for input DC coupling.

With AC-coupled inputs, the FMS6501A uses a simple clamp rather than a full DC-restore circuit. For video signals with and without sync (Y, CV, R, G, B); the lowest voltage at the output pins is clamped to ~300 mV above ground when the 6dB gain setting is selected.

If symmetric AC-coupled input signals are used (Chroma, Pb, Pr, Cb, Cr), the bias circuit described above can be used to center them within the input common range. The average DC value at the output is approximately 1.27 V with a 6 dB gain setting. This value changes, depending upon the selected gain setting, as shown in Table 5.

Table 5. Common Mode Voltage

Gain Setting	Clamp Voltage	Bias Voltage
6dB	300 mV	1.27 V
7dB	330 mV	1.43 V
8dB	370 mV	1.60 V
9dB	420 mV	1.80 V

Figure 8 shows the clamp-mode input circuit and the internally controlled voltage at the input pin for AC-coupled inputs.

Figure 8. Clamp Mode Input Circuit

Figure 9 shows the bias mode input circuit and internally controlled voltage at the input pin for AC-coupled inputs.

Figure 9. Bias Mode Input Circuit

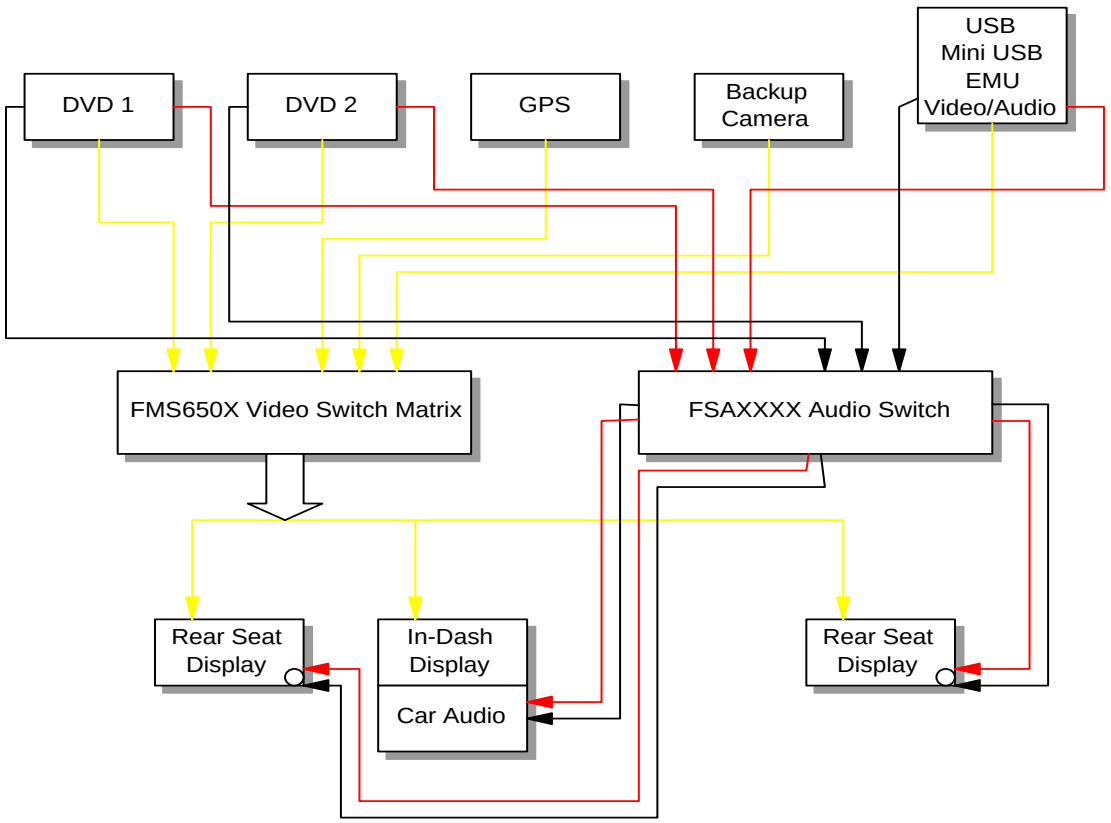

Figure 15. Example of an In-Cabin System

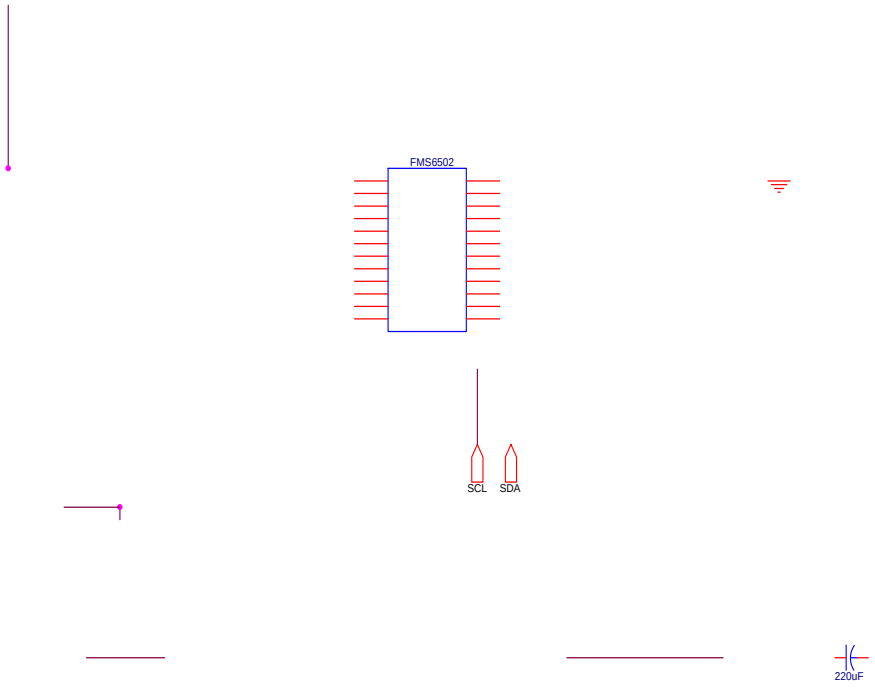

Figure 16. Schematic of an In-Cabin System