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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-).

Features

- 8 x 6 Cross
- Supports S
- Input Clam
- Doubly T
- Program
- AC- or D
- AC- or
- One-to-On
  Switch g
- I^2

Pin Configuration

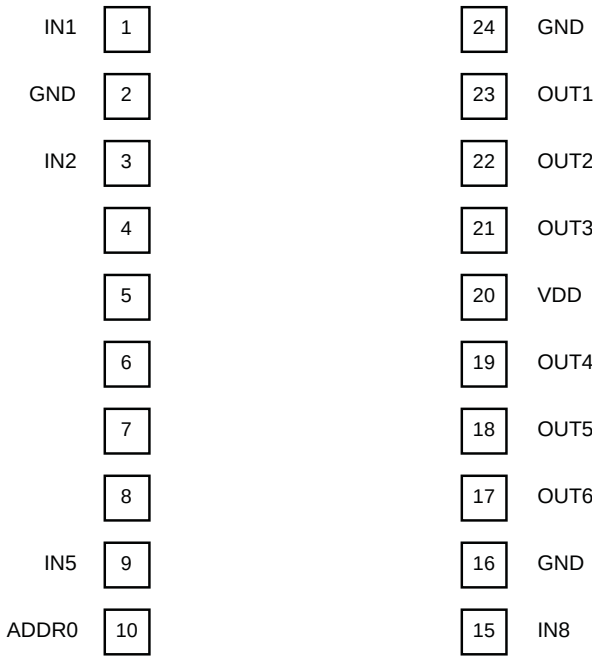

Figure 2. Pin Configuration

Pin Description

Digital Interface

The I^2C-compatibe interface is used to program output enables, input-to-output routing, and input bias configuration. The I^2C address of the FMS6502 is 0x06 (0000 0110) with the ability to offset based upon the values of the ADDR0 and ADDR1 inputs. Offset addresses are defined below:

ADDR1	ADDR0	Binary	Hex
0	0	0000 0110	0x06
0	1	0100 0110	0x46
1	0	1000 0110	0x86
1	1	1100 0110	0xC6

Data and address data of eight bits each are written to the FMS6502 I^2C address register to access control functions.

For efficiency, a single data register is shared between two outputs for input selection. More than one output can select the same input channel for one-to-many routing.

The clamp / bias control bits are written to their own internal address since they should remain the same regardless of signal routing. They are set based on the input signal that is connected to the FMS6502.

All undefined addresses may be written without effect.

Output Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
In-A	4 bits	Write	0	3:0	Input selected to drive this output: 0000=OFF[1], 0001=IN1, 0010=IN2, 1000=IN8
In-B	4 bits	Write	0	7:4	Input selected to drive this output: 0000=OFF[1], 0001=IN1, 0010=IN2, 1000=IN8

Output Control Register MAP

Name	Address	Bit 7	Bit 6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OUT1,2	0x00	B3-Out2	B2-Out2	B1-Out2	B0-Out2	B3-Out1	B2-Out1	B1-Out1	B0-Out1
OUT3,4	0x01	B3-Out4	B2-Out4	B1-Out4	B0-Out4	B3-Out3	B2-Out3	B1-Out3	B0-Out3
OUT5,6	0x02	B3-Out6	B2-Out6	B1-Out6	B0-Out6	B3-Out5	B2-Out5	B1-Out5	B0-Out5

Clamp Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
Clmp	1 bit	Write	0	7:0	Clamp / Bias selection: 1 = Clamp, 0 = Bias

Clamp Control Register Map

Name	Address	Bit 7	Bit 6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLAMP	0x03	Clmp8	Clmp7	Clmp6	Clmp5	Clmp4	Clmp3	Clmp2	Clmp1

Gain Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
Gain	1 bit	Write	0	7:0	Output Gain selection: 0 = 6dB, 1 = 0dB

Gain Control Register Map

Name	Address	Bit 7	Bit 6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GAIN	0x04	Unused	Unused	Gain6	Gain5	Gain4	Gain3	Gain2	Gain1

Note:

1. When the OFF input selection is used, the output amplifier is powered down and enters a high-impedance state.

DC Electrical Characteristics

T_A = 25°C, V_{cc} = 5V, V_{in} = $1V_{pp}$, input bias mode, one-to-one routing, 6dB gain, all inputs AC-coupled with 0.1µF,

I²C BUS Characteristics

T_A = 25°C, V_{cc} = 5V unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{il}	Digital Input Low[1]	SDA,SCL,ADDR	0		1re 3.	I

Note:

1. 100% tested at 25°C.

Figure 3. I²C Bus Timing

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter while the master generates an extra acknowledge-related clock pulse. The slave receiver addressed must generate an acknowledge after

Figure 6. Acknowledgement on the I^2C Bus

Applications Information

Input Clamp / Bias Circuitry

The FMS6502 can accommodate AC- or DC-coupled inputs. Internal clamping and bias circuitry are provided to support AC-coupled inputs. These are selectable through the CLMP bits via the I^2C-compatible interface. For DC-coupled inputs, the device should be programmed to use the 'bias' input configuration. In this configuration, the input is internally biased to 625mV through a 100kΩ resistor. Distortion is optimized with the output levels set between 250mV above ground and 500mV below the power supply.

With AC-coupled inputs, the FMS6502 uses a simple clamp rather than a full DC-restore circuit. For video signals with and without sync; (Y,CV,R,G,B), the lowest voltage at the output pins is clamped to approximately 300mV above ground.

If symmetric AC-coupled input signals are used (Chroma,Pb,Pr,Cb,Cr), the bias circuit can be used to center them within the input common range. The aver-

Crosstalk

Crosstalk is an important consideration when using the FMS6502. Input and output crosstalk represent the two major coupling modes that may be present in a typical application. Input crosstalk is crosstalk in the input pins and switches when the interfering signal drives an open switch. It is dominated by inductive coupling in the package lead frame between adjacent leads. It decreases rapidly as the interfering signal moves further away from the pin adjacent to the input signal selected. Output crosstalk is coupling from one driven output to another active output. It decreases with increasing load impedance as it is caused mainly by ground and power cou-

Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board to guide layout and aid device evaluation. The demo board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

Recommended Routing/Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should run on top of the ground plane at all times.
- No trace should run over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 10µF and 0.1µF ceramic power supply bypass

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

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