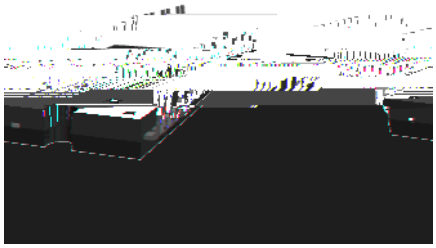


Integrated Power Functions

- – –

Integrated Drive, Protection, and System Control Functions

- – – – – – – –
- – –
- – – – –

Pin Configuration

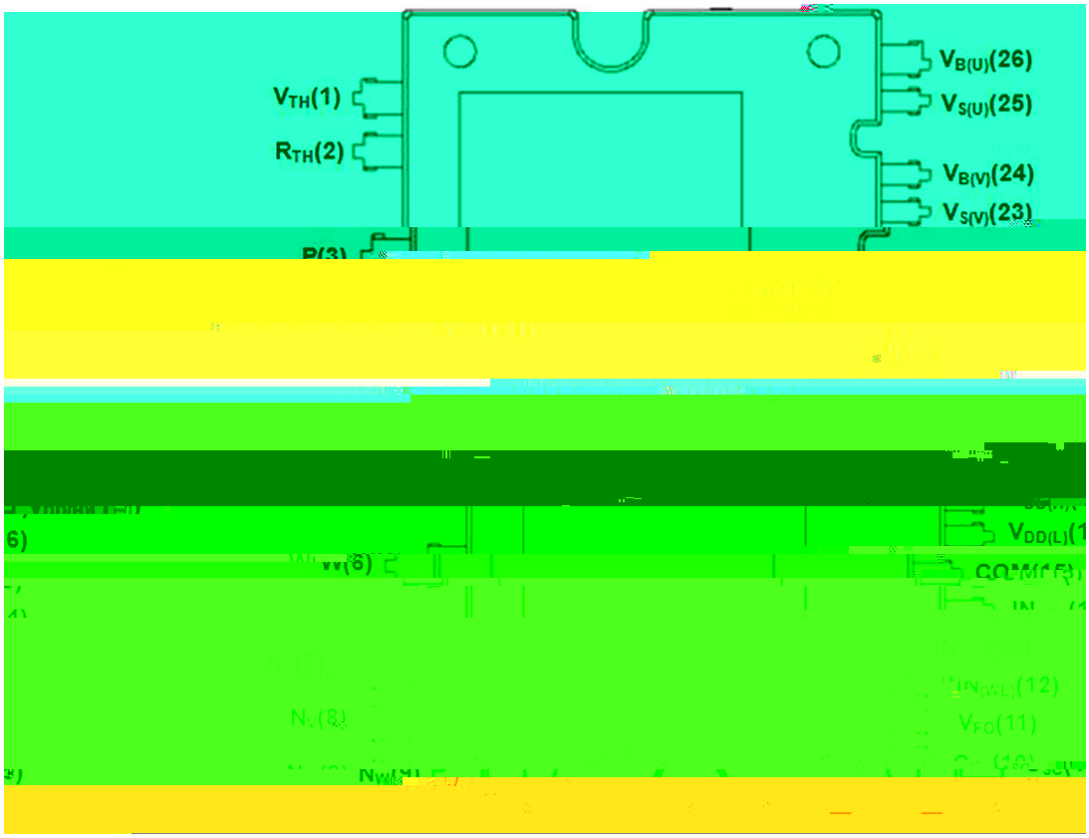
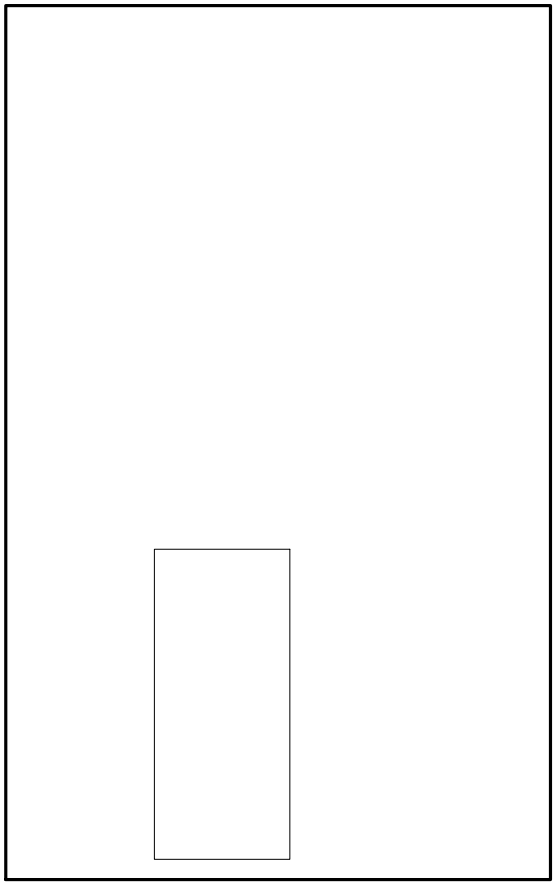


Figure 1. Top View

PIN DESCRIPTIONS

Pin No.	Pin Name	Pin Description
1	V_{TH}	Thermistor Bias Voltage
2	R_{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
3	P	Positive DC−Link Input
4	U	Output for U−Phase
5	V	Output for V−Phase
6	W	Output for W−Phase
7	N_U	Negative DC−Link Input for U−Phase
8	N_V	Negative DC−Link Input for V−Phase
9	N_W	Negative DC−Link Input for W−Phase
10	C_{SC}	Shut Down Input for Short−circuit Current Detection Input
11	V_{FO}	Fault Output
12	$IN_{(WL)}$	Signal Input for Low−Side W−Phase
13	$IN_{(VL)}$	Signal Input for Low−Side V−Phase
14	$IN_{(UL)}$	Signal Input for Low−Side U−Phase
15	COM	Common Supply Ground
16	$V_{DD(L)}$	Low−Side Common Bias Voltage for IC and IGBTs Driving
17	$V_{DD(H)}$	High−Side Common Bias Voltage for IC and IGBTs Driving
18	$IN_{(WH)}$	Signal Input for High−Side W−Phase
19	$IN_{(VH)}$	Signal Input for High−Side V−Phase
20	$IN_{(UH)}$	Signal Input for High−Side U−Phase
21	$VS_{(W)}$	Side V

Internal Equivalent Circuit and Input/Output Pins



NOTES:
1. Inverter high−side is composed of three normal−IGBTs, freewheeling diodes, and one control IC for each IGBT.
2. Inverter low−side is composed of three sense−IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
3. Inverter power side is composed of four inverter DC−link input terminals and three inverter output terminals.

Figure 2. Internal Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C, unless otherwise specified)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART				
V_{PN}	Supply Voltage	Applied between P – N_U, N_V, N_W	450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P – N_U, N_V, N_W	500	V
V_{CES}	Collector – Emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	T_C = 25°C, T_J < 150°C	15	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C = 25°C, T_J < 150°C, Under 1 ms Pulse Width (Note 4)	30	A
P_C	Collector Dissipation	T_C = 25°C per One Chip (Note 4)	38	W
T_J	Operating Junction Temperature		–40 ~ 150	°C
CONTROL PART				
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$, $V_{DD(L)}$ – COM	20	V
V_{BS}	High–Side Control Bias Voltage	Applied between $V_{B(U)}$ – $V_{S(U)}$, $V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – COM	–0.3 ~ V_{DD} + 0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} – COM	–0.3 ~ V_{DD} + 0.3	V

ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

Symbol		Parameter	Conditions		Min.	Typ.	Max.	Unit
INVERTER PART								
$V_{CE(SAT)}$		Collector – Emitter Saturation Voltage	$V_{DD} = V_{BS}$ = 15 V V_{IN} = 5 V	I_C = 15 A, T_J = 25°C	–	1.60	2.20	V
V_F		FWDi Forward Voltage	V_{IN} = 0 V	I_F = 15 A, T_J = 25°C	–	2.00	2.60	V
HS	t_{ON}	Switching Times	V_{PN} = 300 V, $V_{DD} = V_{BS}$ = 15 V, I_C = 15 A T_J = 25°C V_{IN} = 0 V ↔ 5 V, Inductive Load (Note 6)		0.40	0.80	1.30	μs
	$t_{C(ON)}$				–	0.20	0.50	μs
	t_{OFF}				–	0.85	1.35	μs
	$t_{C(OFF)}$				–	0.25	0.55	μs
	t_{rr}				–	0.10	–	μs
LS	t_{ON}		V_{PN} = 300 V, $V_{DD} = V_{BS}$ = 15 V, I_C = 15 A T_J = 25°C V_{IN} = 0 V ↔ 5 V, Inductive Load (Note 6)		0.45	0.85	1.35	μs
	$t_{C(ON)}$				–	0.25	0.55	μs
	t_{OFF}				–	0.90	1.40	μs
	$t_{C(OFF)}$				–	0.25	0.55	μs
	t_{rr}				–	0.15	–	μs
I_{CES}		Collector – Emitter Leakage Current	$V_{CE} = V_{CES}$		–	–	1	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. t_{ON}

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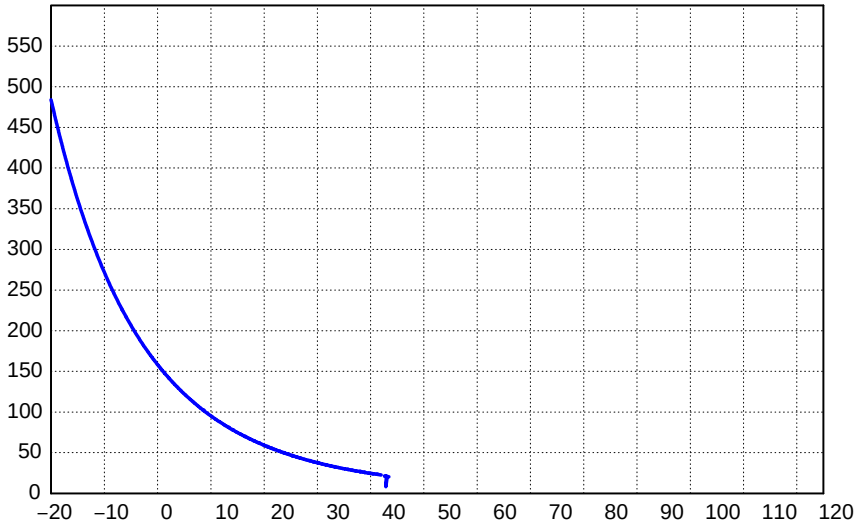

Figure 5. R T Curve of The Built In Thermistor

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P – N_U, N_V, N_W	–	300	400	V
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$, $V_{DD(L)}$ – COM	13.5	15.0	16.5	V
V_{BS}	High−Side Bias Voltage	Applied between $V_{B(U)}$ – $V_{S(U)}$, $V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$	13.0	15.0	18.5	V
dV_{DD} / dt, dV_{BS} / dt	Control Supply Variation		−1	–	1	V / μs
t_{dead}	Blanking Time for Preventing Arm – Short	For each input signal	1	–	–	μs
f_{PWM}	PWM Input Signal	−40°C ≤ T_C ≤ 125°C, −40°C ≤ T_J ≤ 150°C	–	–	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W – COM (Including Surge−Voltage)	−4	–	4	V
$PW_{IN(ON)}$	Minimun Input Pulse Width	V_{DD} = V_{BS} = 15 V, I_C ≤ 15 A, Wiring Inductance between $N_{U, V, W}$ and DC Link N < 10 nH (Note 9)	0.5	–	–	μs
$PW_{IN(OFF)}$			0.5	–	–	
$PW_{IN(ON)}$	Minimun Input Pulse Width	V_{DD} = V_{BS} = 15 V, I_C ≤ 30 A, Wiring Inductance between $N_{U, V, W}$ and DC Link N < 10 nH (Note 9)	1.2	–	–	μs
$PW_{IN(OFF)PW}$						

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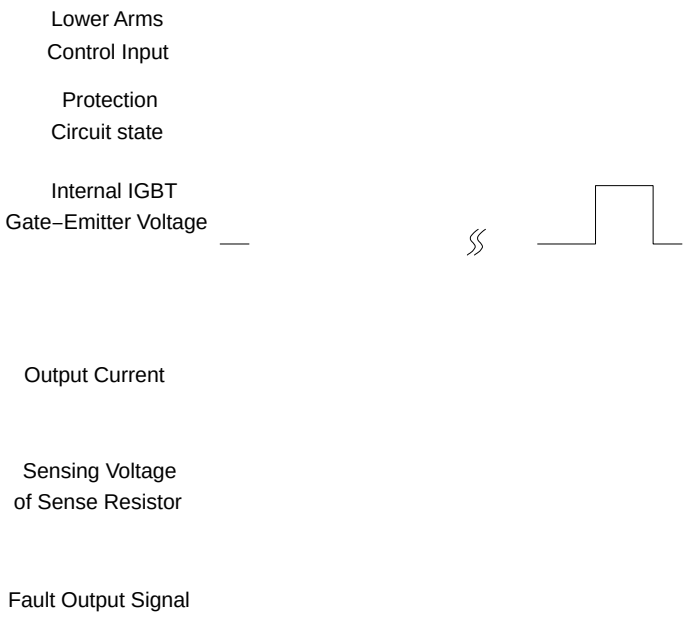

(with the external sense resistance and RC filter connection)
c1 : Normal operation: IGBT ON and carrying current.
c2 : Short−circuit current detection (SC trigger).
c3 : All low−side IGBTs gate are hard interrupted.
c4 : All low−side IGBTs turn OFF.
c5 : Fault output operation starts with a fixed pulse width according to the condition of the external capacitor C_{FOD}.
c6 : Input HIGH: IGBT ON state, but during the active period of fault output, the IGBT doesn't turn ON.
c7 : Fault output operation finishes, but IGBT doesn't turn on until triggering the next signal from LOW to HIGH.
c8 : Normal operation: IGBT ON and carrying current.

Figure 12. Short Circuit Current Protection (Low Side Operation only)

Figure 14. Typical Application Circuit

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Shipping
FNA41560T2	FNA41560T2	SPMAA−C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL FORM TYPE (Pb−Free)	12 Units / Rail