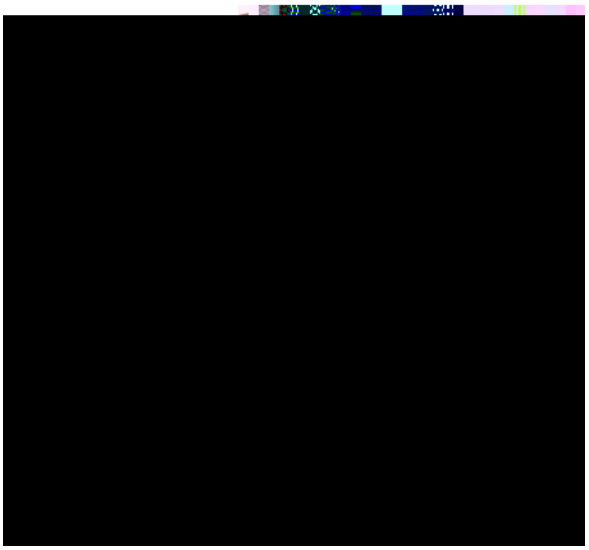


Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

April 2017

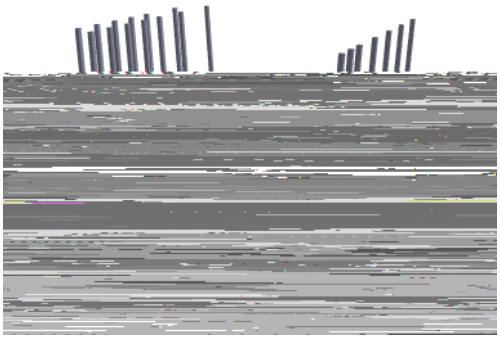
FNA51560TD3

Motion SPM® 55 Series

Features

- UL Certified No. E209204 (UL1557)
- 600 V - 15 A 3-Phase IGBT Inverter Including Control IC for Gate Drive and Protections
- Low-Loss, Short-Circuit Rated IGBTs
- Built-In Bootstrap Diodes in HVIC
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Active-HIGH interface, works with 3.3 / 5 V Logic, Schmitt-trigger Input
- HVIC for Gate Driving, Under-Voltage and Short-Circuit Current Protection
- Fault Output for Under-Voltage and Short-Circuit Current Protection
- Inter-Lock Function to Prevent Short-Circuit
- Shut-Down Input
- HVIC Temperature-Sensing Built-In for Temperature Monitoring
- Optimized for 5 kHz Switching Frequency
- Isolation Rating: 1500 V_{rms} / min.

Applications



Integrated Power Functions

- 600 V - 15 A IGBT inverter for three phase DC / AC power conversion (Please refer to Figure 3)

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting
  control circuit Under-Voltage Lock-Out (UVLO) protection
- For inverter low-side IGBTs: gate drive circuit, Short-Circuit Protection (SCP)
  control supply circuit Under-Voltage Lock-Out (UVLO) protection
- Fault signaling: corresponding to UVLO (low-side supply) and SC faults
- Input interface: High-active interface, works with 3.3 / 5 V logic, Schmitt trigger input
- Built in Bootstrap circuitry in HVIC

Pin Configuration

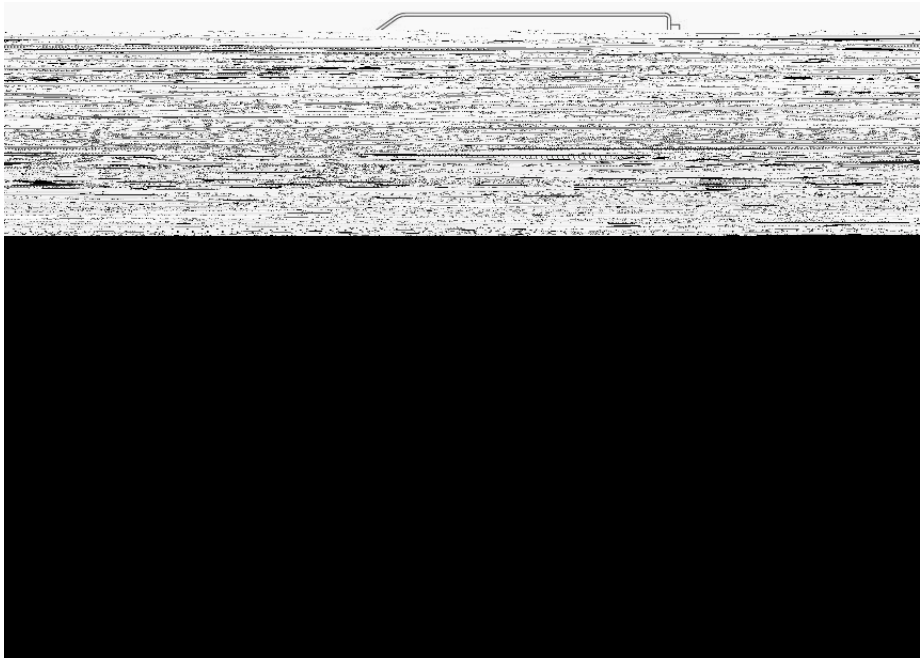


Figure 2. Top View

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	P	Positive DC-Link Input

Absolute Maximum Ratings (T_J = 25°C, unless otherwise specified.)

Inverter Part

Symbol	Parameter	Conditions	Rating	Unit
V_{PN}	Supply Voltage	Applied between P - N_U, N_V, N_W	450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P - N_U, N_V, N_W	500	V
V_{CES}	Collector - Emitter Voltage		600	V
*± I_C	Each IGBT Collector Current	T_C = 25°C, T_J 150°C	15	A
*± I_{CP}	Each IGBT Collector Current (Peak)	T_C = 25°C, T_J 150°C, Under 1 ms Pulse Width	30	A
*P_C	Collector Dissipation	T_C = 25°C per Chip	27	W
T_J	Operating Junction Temperature	(Note 5)	-40 ~ 150	°C

Note:

5. The maximum junction temperature rating of the power chips integrated within the Motion SPM® 55 product is 150 C.

Control Part

Symbol	Parameter	Conditions	Rating	Unit
V_{DD}	Control Supply Voltage	Applied between V_{DD}		

Total System

Thermal Resistance

Note:

6. For Marking " * ", These Value had been made an acquisition by the calculation considered to design factor.

7. For the measurement point of case temperature (T_C), please refer to Figure 2.

Bootstrap Diode Part

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{BS}	Bootstrap Diode Resitance	V_{DD} = 15V, T_C = 25°C	-	280	-	

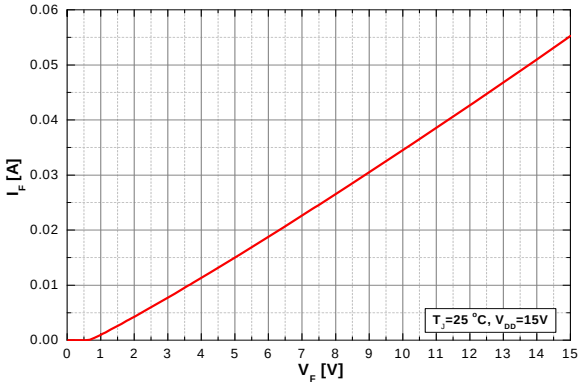


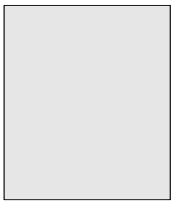
Figure 6. Built-In Bootstrap Diode Charaterstics

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P - N_U, N_V, N_W	-	300	400	V
V_{DD}	Control Supply Voltage	Applied between V_{DD} - COM	14.0	15	16.5	V
V_{BS}	High - Side Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	13.0	15	18.5	V
dV_{DD} / dt, dV_{BS} / dt	Control Supply Variation		-1	-	1	V / s
t_{dead}	Blanking Time for Preventing Arm - Short	For each input signal	1.5	-	-	s
f_{PWM}	PWM Input Signal	- 40 C T_J 150°C	-	-	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W - COM (Including surge voltage)	-4		4	V
$P_{WIN(ON)}$	Minimun Input Pulse Width	(Note 9)	0.7	-	-	s
$P_{WIN(OFF)}$			0.7	-	-	

Note:

10. This product might not make response if input pulse width is less than the recommanded value.



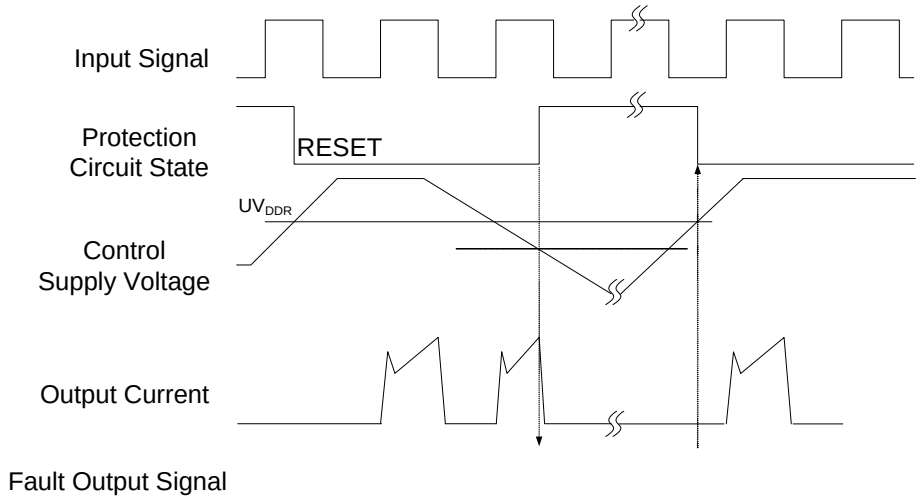
Note:

11. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the SPM 55 product integrates 10 k (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

Figure 7. Recommended MCU I/O Interface Circuit

Mechanical Characteristics and Ratings

Time Charts of Protective Function



a1 : Control supply voltage rises: After the voltage rises UV_{DDR}, the circuits start to operate when next input is applied.

a2 : Normal operation: IGBT ON and carrying current.

a3 : Under voltage detection (UV_{DDD}).

a4 : IGBT OFF in spite of control input condition.

a5 : Fault output operation starts.

a6 : Under voltage reset (UV_{DDR}).

a7 : Normal operation: IGBT ON and carrying current.

Figure 10. Under-Voltage Protection (Low-Side)

b1 : Control supply voltage rises: After the voltage reaches UV_{BSR}, the circuits start to operate when next input is applied.

b2 : Normal operation: IGBT ON and carrying current.

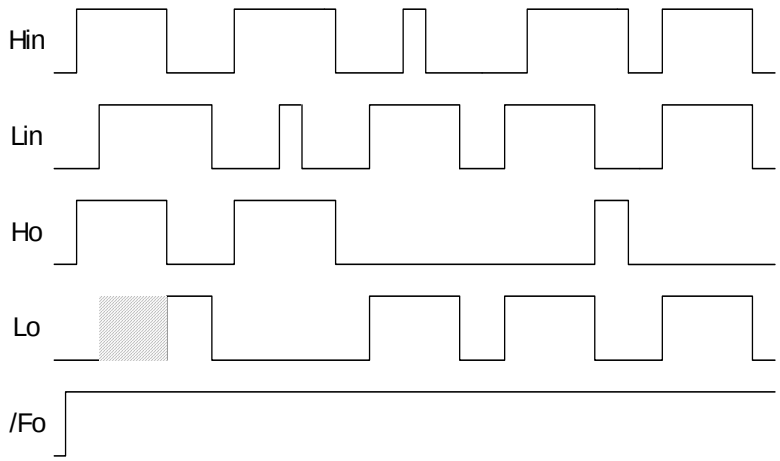
b3 : Under voltage detection (UV_{BSD}).

b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.

b5 : Under voltage reset (UV_{BSR})

b6 : Normal operation: IGBT ON and carrying current

Figure 11. Under-Voltage Protection (High-Side)



d1 : High Side First - Input - First - Output Mode

d2 : Low Side Noise Mode : No Lo

d3 : High Side Noise Mode : No Ho

d4 : Low Side First - Input - First - Output Mode

d5 : In - Phase Mode : No Ho

Figure 12. Inter-Lock Function

HIN : High-side Input Signal

LIN : Low-side Input Signal

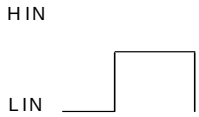
HO : High-Side Output Signal

LO : Low-Side Output Signal

CSC : Over Current Detection Input

VF : Fault Out Function

Figure 13. Fault-Out Function By Over Current Protection



HIN : High-side Input Signal
LIN : Low-side Input Signal
HO : High-Side Output Signal
LO : Low-Side Output Signal
CSC : Over Current Detection Input
VF : Shutdown Input Function

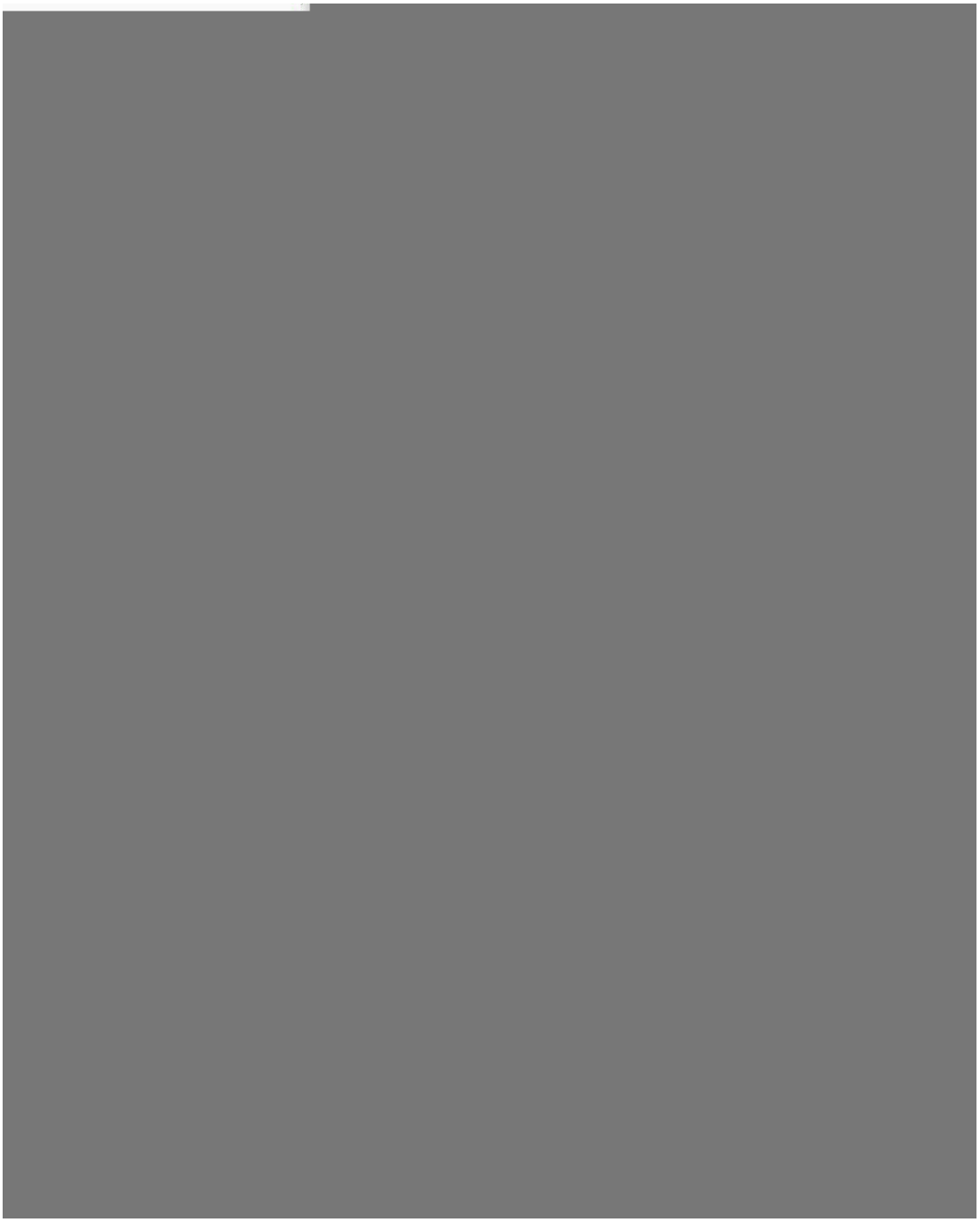
Figure 14. Shutdown Input Function By External Command

Note:

1) To avoid malfunction, the wiring of each input should be as short as possible. (less than 2 ~ 3 cm)

2) By virtue of integrating an application specific type of HVIC inside the SPM®

Detailed Package Outline Drawings (FNA51560TD3, Long Lead)



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