



FNC42060F, FNC42060F2

PIN CONFIGURATION

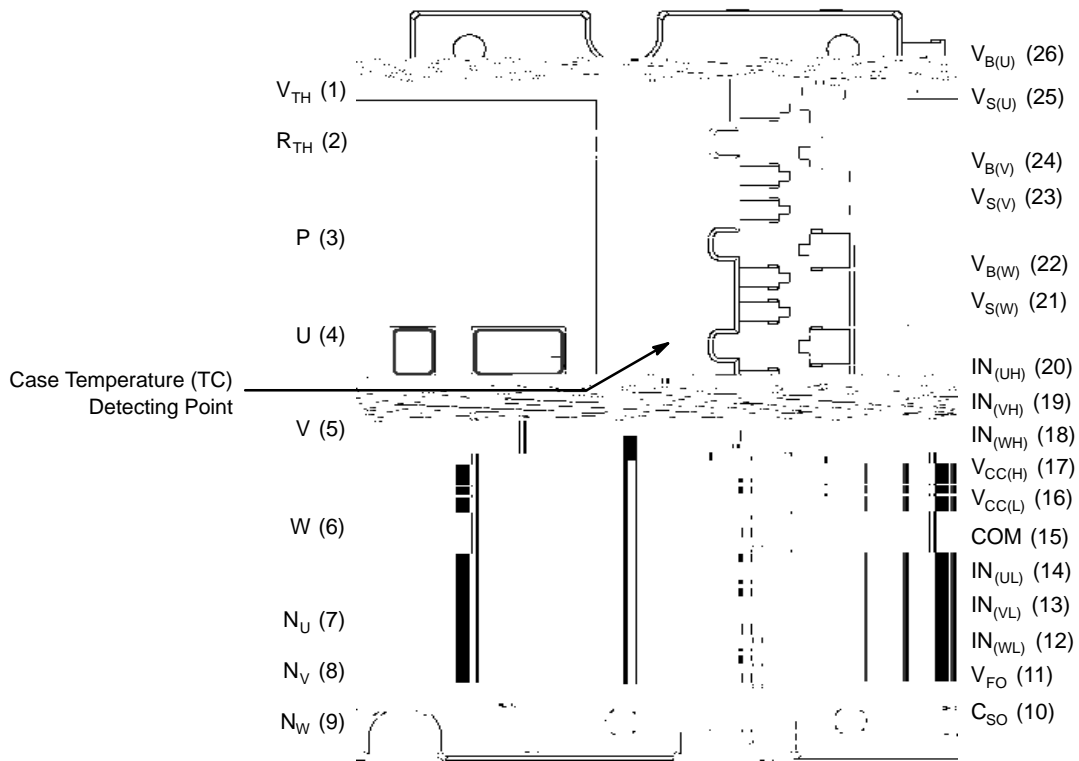


Figure 1. Top View

PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Description
1	V _{TH}	Thermistor Bias Voltage
2	R _{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
3	P	Positive DC-Link Input
4	U	Output for U-Phase
5	V	Output for V-Phase
6	W	Output for W-Phase
7	N _U	Negative DC-Link Input for U-Phase
8	N _V	Negative DC-Link Input for V-Phase
9	N	

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PIN DESCRIPTIONS (continued)

Pin Number	Pin Name	Pin Description
19	IN(VH)	Signal Input for High-Side V-Phase
20	IN(UH)	Signal Input for High-Side U-Phase
21	V _{S(W)}	High-Side Bias Voltage Ground for W-Phase IGBT Driving
22	V _{B(W)}	High-Side Bias Voltage for W-Phase IGBT Driving
23	V _{S(V)}	High-Side Bias Voltage Ground for V-Phase IGBT Driving
24	V _{B(V)}	High-Side Bias Voltage for V-Phase IGBT Driving
25	V _{S(U)}	High-Side Bias Voltage Ground for U-Phase IGBT Driving
26	V _{B(U)}	High-Side Bias Voltage for U-Phase IGBT Driving

INTERMEDIATE High-Side Bias Voltage for V-Phase IGBT Driving

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ABSOLUTE MAXIMUM RATINGS ($T_J = 25\text{ C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Rating	Unit
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INVERTER PART

V_{PN}	Supply Voltage	Applied between P – N_U , N_V , N_W	450	V
$V_{PN(\text{Surge})}$	Supply Voltage (Surge)	Applied between P – N_U , N_V , N_W	500	V
V_{CES}	Collector–Emitter Voltage		600	V
$+I_C$	Each IGBT Collector Current	$T_C = 25\text{ C}$, $T_J < 150\text{ C}$	20	A
$+I_{CP}$	Each IGBT Collector Current (Peak)	$T_C = 25\text{ C}$, $T_J < 150\text{ C}$, Under 1 ms Pulse Width	40	A
P_C	Collector Dissipation	$T_C = 25\text{ C}$ per Chip	50	W
T_J	Operating Junction Temperature	(Note 4)	–40–150	C

CONTROL PART

V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)} - \text{COM}$	20	V
V_{BS}	High–Side Control Bias Voltage	Applied between $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$	20	V

V

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ELECTRICAL CHARACTERISTICS (T_J = 25 C unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
INVERTER PART							
V _{CE(SAT)}	Collector-Emitter Saturation Voltage	V _{CC} = V _{BS} = 15 V V _{IN} = 5 V	I _C = 20 A, T _J = 25 C	-	1.85	2.35	V
V _F	FWDi Forward Voltage	V _{IN} = 0 V	I _F = 20 A, T _J = 25 C	-	1.95	2.45	V
HS	t _{ON}	Switching Times	V _{PN} = 300 V, V _{CC} = V _{BS} = 15 V, I _C = 20 A, T _J = 25 C V _{IN} = 0 V 5 V, Inductive Load (Note 6)	0.45	0.75	1.25	μs
	t _{C(ON)}			-	0.20	0.45	μs
	t _{OFF}			-	0.70	1.20	μs
	t _{C(OFF)}			-	0.15	0.40	μs
	t _{rr}			-	0.15	-	μs
LS	t _{ON}				0.75	1.25	

C(OFF)

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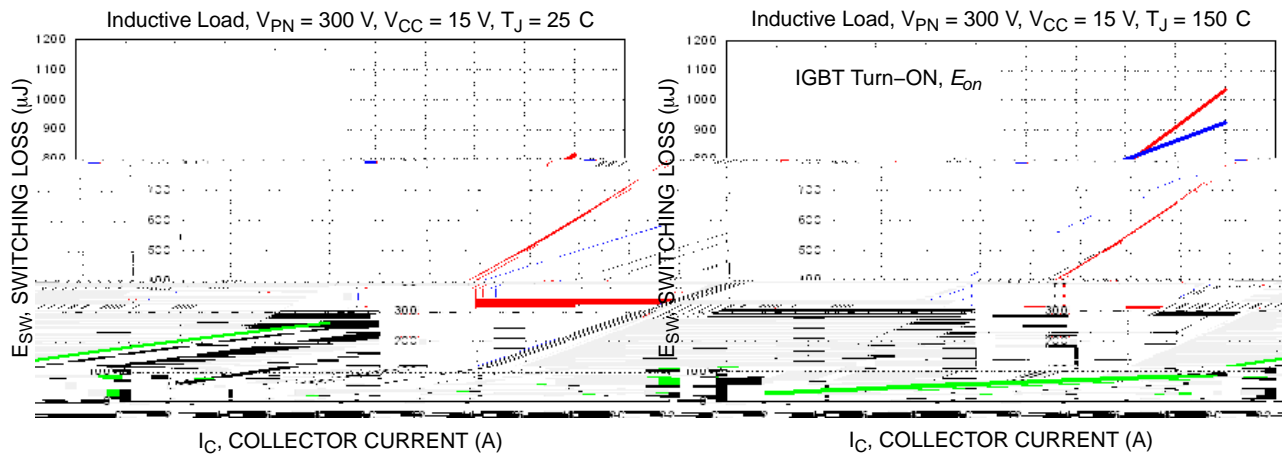


Figure 4. Switching Loss Characteristics (Typical)

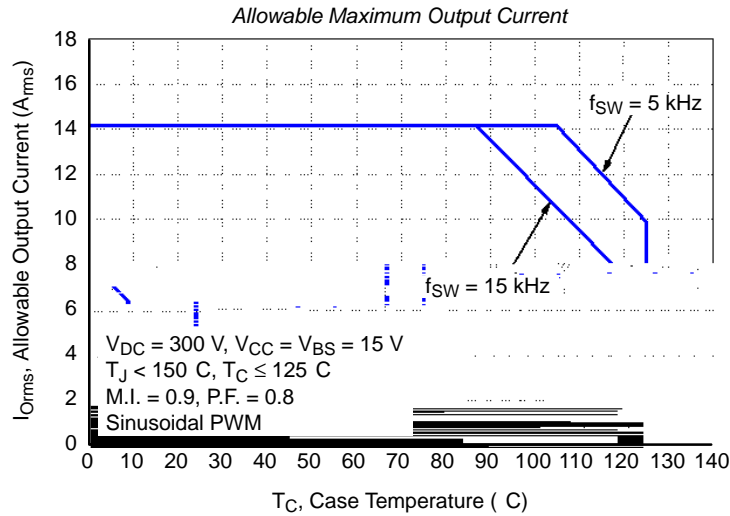
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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PN}	Supply Voltage	Applied between P – N_U , N_V , N_W	–	300	400	V
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)} - COM$	13.5	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$	13.0	15.0	18.5	V
dV_{CC}/dt , dV_{BS}/dt	Control Supply Variation		–1	–	1	V / μ s
t_{dead}	Blanking Time for Preventing Arm-Short	For each input signal	1.5	–	–	μ s
f_{PWM}	PWM Input Signal	$-40\text{ C} < T_J < 150\text{ C}$	–	–	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U , N_V , $N_W - COM$ (Including Surge-Voltage)	–4	–	4	V
$P_{WIN(ON)}$	Minimum Input Pulse Width	(Note 10)	0.7	–	–	μ s
$P_{WIN(OFF)}$			0.7	–	–	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

10. This product might not make response if input pulse width is less than the recommended value.



NOTE:

11. This allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition.

Figure 7. Allowable Maximum Output Current

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MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions	Min	Typ	Max	Unit	
Device Flatness	See Figure 8	0	–	+120	μm	
Mounting Torque	Mounting Screw: M3 See Figure 9	Recommended 0.7 N _j m	0.6	0.7	0.8	N _j m
		Recommended 7.1 kg _j cm	6.2	7.1	8.1	kg _j cm
Weight		–	11.00	–	g	

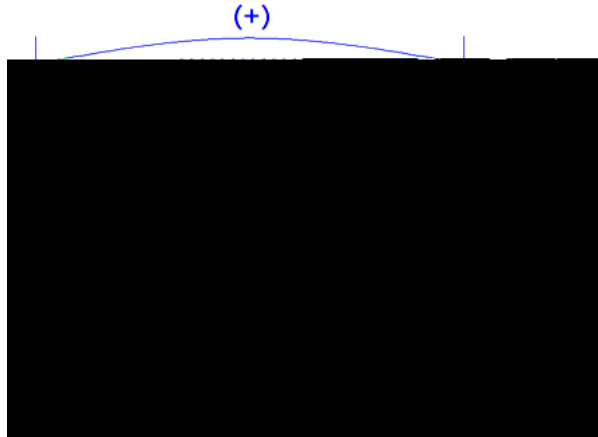
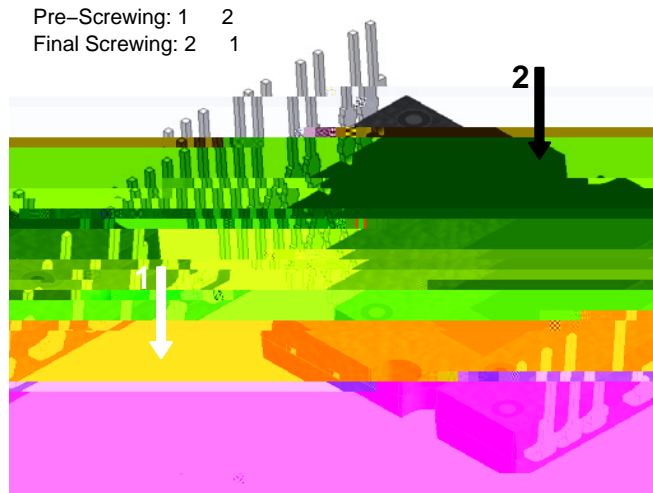


Figure 8. Flatness Measurement Position



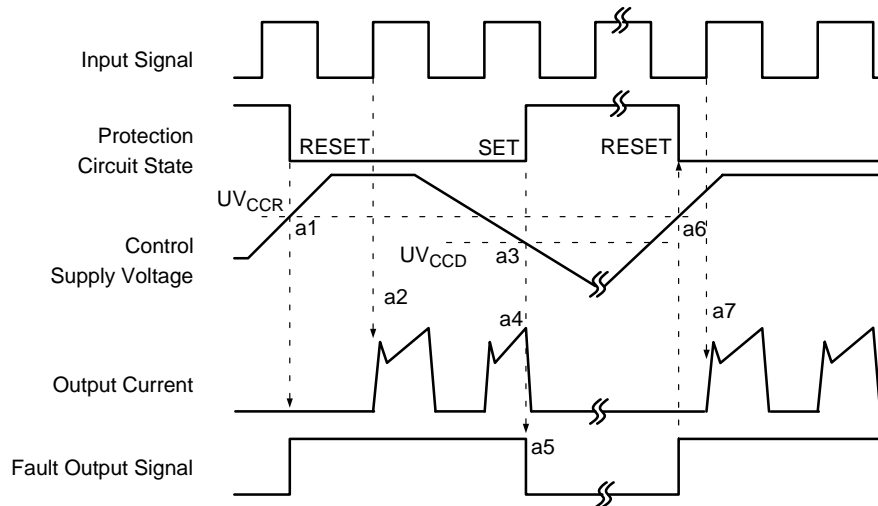
NOTES:

- 12. Do not make over torque when mounting screws. Much mounting torque may cause ceramic cracks, as well as bolts and Al heat-sink destruction.
- 13. Avoid one side tightening stress. Figure 9 shows the recommended torque order for mounting screws. Uneven mounting can cause the ceramic substrate of the SPM 45 package to be damaged. The pre-screwing torque is set to 20–30% of maximum torque rating.

Figure 9. Mounting Screws Torque Order

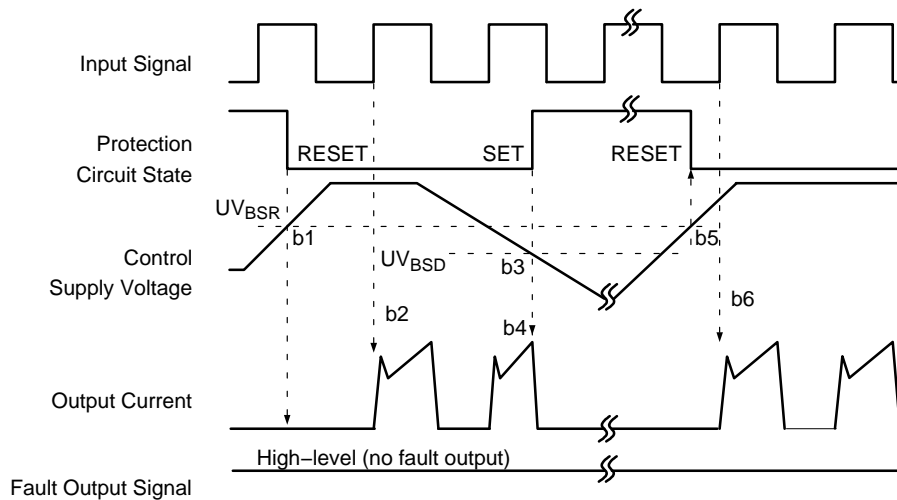
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TIME CHARTS OF PROTECTIVE FUNCTION



- a1: Control supply voltage rises: after the voltage rises UV_{CCR} , the circuits start to operate when next input is applied.
- a2: Normal operation: IGBT ON and carrying current.
- a3: Under-voltage detection (UV_{CCD}).
- a4: IGBT OFF in spite of control input condition.
- a5: Fault output operation starts.
- a6: Under-voltage reset (UV_{CCR}).
- a7: Normal operation: IGBT ON and carrying current.

Figure 10. Under-Voltage Protection (Low-Side)



- b1: Control supply voltage rises: after the voltage reaches UV_{BSR} , the circuits start to operate when next input is applied.
- b2: Normal operation: IGBT ON and carrying current.
- b3: Under-voltage detection (UV_{BSD}).
- b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5: Under-voltage reset (UV_{BSR}).
- b6: Normal operation: IGBT ON and carrying current.

Figure 11. Under-Voltage Protection (High-Side)

NOTES:

- 15. To avoid malfunction, the wiring of each input should be as short as possible (less than 2–3 cm).
- 16. By virtue of integrating an application–specific type of HVIC

Figure 14. Typical Application Circuit

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ORDERING INFORMATION

Device	Device Marking	Package	Shipping
FNC42060F	FNC42060F	SPMAA-A26	12 Units / Rail
FNC42060F2	FNC42060F2	SPMAA-C26	12 Units / Rail

SPM is a registered trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

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PACKAGE DIMENSIONS

SPMAA-A26 / 26LD, PDD STD, CERAMIC TYPE, STANDARD DUAL FORM
CASE MODFA
ISSUE 0

NOTES: UNLESS OTHERWISE

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