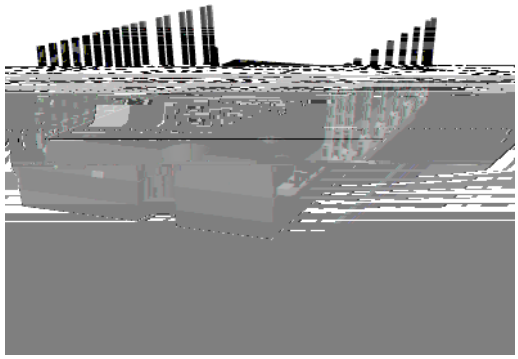
Motion SPM® 45 Series

FND42060F2

General Description

FND42060F2 is an advanced Motion SPM 45 module providing a fully−featured, high−performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built−in IGBTs to minimize EMI and losses,

drive the module's robust short−circuit−rated



PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Description
1	V_{TH}	Thermistor Bias Voltage
2	R_{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
3	P	Positive DC Link Input
4	U	Output for U Phase
5	V	Output for V Phase
6	W	Output for W Phase
7	N_U	Negative DC Link Input for U Phase
8	N_V	Negative DC Link Input for V Phase
9	N_W	Negative DC Link Input for W Phase

INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS

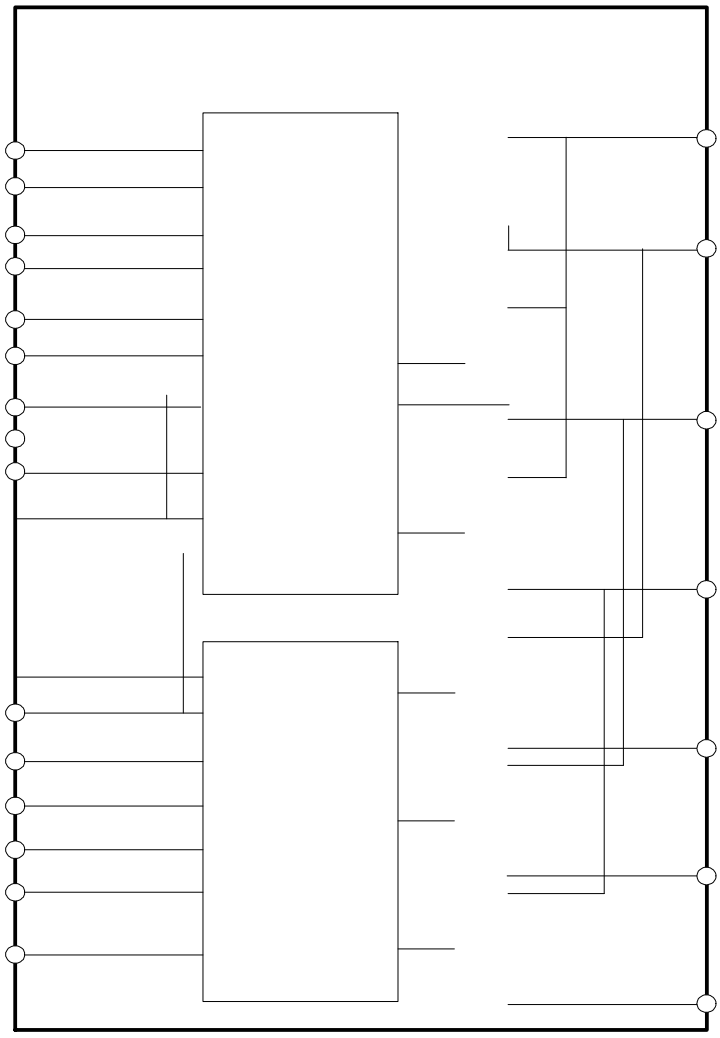


Figure 3. Internal Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART				
V_{PN}	Supply Voltage	Applied between P N_U, N_V, N_W	450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P N_U, N_V, N_W	500	V
V_{CES}	Collector Emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	T_C = 25°C, $T_J \leq$ 150°C	20	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C = 25°C, $T_J \leq$ 150°C, Under 1 ms Pulse Width	40	A
P_C	Collector Dissipation	T_C = 25°C per Chip	50	W
T_J	Operating Junction Temperature	(Note 2)	40 ~ 150	°C
CONTROL PART				
V_{CC}	Control Supply VTINGS			

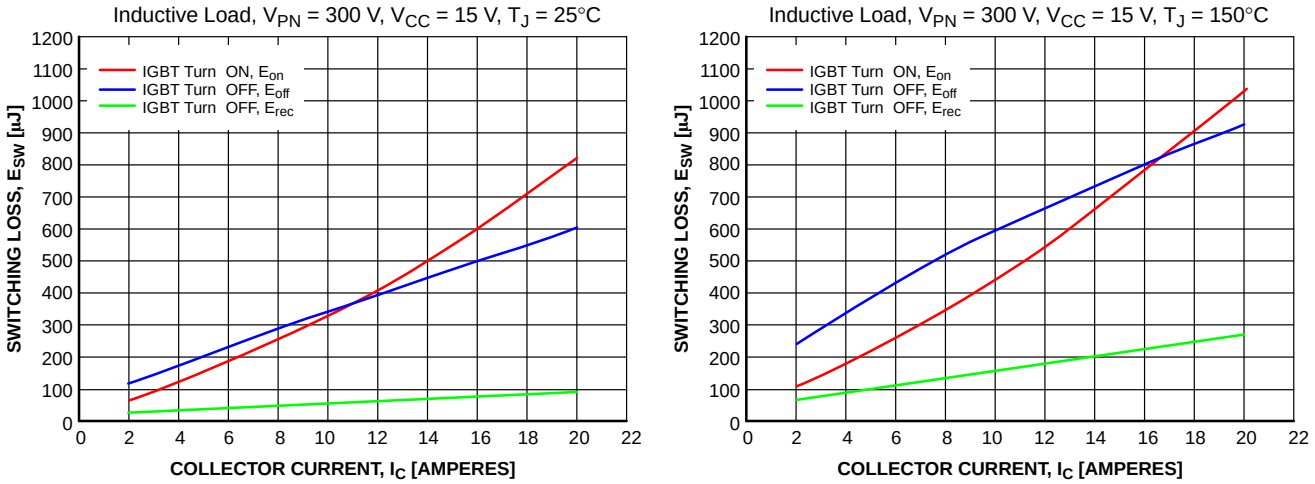


Figure 5. Switching Loss Characteristics (Typical)

CONTROL PART

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{QCCH}	Quiescent V_{CC} Supply Current	$V_{CC(H)}$ = 15 V, $IN_{(UH,VH.WH)}$ = 0 V	$V_{DD(H)}$ COM			0.10	mA
I_{QCCL}		$V_{CC(L)}$ = 15 V, $IN_{(UL,VL,WL)}$ = 0 V	$V_{CC(L)}$ COM			2.65	mA
I_{PCCH}	Operating V_{CC} Supply Current	$V_{CC(L)}$ = 15 V, f_{PWM} = 20 kHz, duty = 50%, Applied to one PWM Signal Input for High Side	$V_{CC(H)}$ COM			0.15	mA
I_{PCCL}		$V_{CC(L)}$ = 15 V, f_{PWM} = 20 kHz, duty = 50%, Applied to one PWM Signal Input for Low Side	$V_{CC(L)}$ COM			4.00	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15 V, $IN_{(UH,VH.WH)}$ = 0 V	$V_{B(U)}$ $V_{S(U)}$, $V_{B(V)}$ $V_{S(V)}$, $V_{B(W)}$ $V_{S(W)}$,			0.30	mA
I_{PBS}	Operating V_{BS} Supply Current	V_{DD} = V_{BS} = 15 V, f_{PWM} = 20 kHz, duty = 50%, Applied to one PWM Signal Input for High Side	$V_{B(U)}$ $V_{S(U)}$, $V_{B(V)}$ $V_{S(V)}$, $V_{B(W)}$ $V_{S(W)}$,			2.00	mA
V_{FOH}	Fault Output Voltage	V_{SC} = 0 V, V_{FO} Circuit: 10 kΩ to 5 V Pull up		4.5			V
V_{FOL}		V_{SC} = 1 V, V_{FO} Circuit: 10 kΩ to 5 V Pull up				0.5	V
$V_{SC(ref)}$	Short Circuit Trip Level	V_{CC} = 15 V (Note 5)		0.45	0.50	0.55	V
UV							

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P N_U, N_V, N_W		300	400	V
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$ COM, $V_{CC(L)}$ COM	13.5	15.0	16.5	V
V_{BS}	High Side Bias Voltage	Applied between $V_{B(U)}$ $V_{S(U)}$, $V_{B(V)}$ $V_{S(V)}$, $V_{B(W)}$ $V_{S(W)}$	13.0	15.0	18.5	V
dV_{CC}/dt, dV_{BS}/dt	Control Supply Variation		1		1	V/μs
t_{dead}	Blanking Time for Preventing Arm Short	For Each Input Signal	1.5			μs
f_{PWM}	PWM Input Signal	40°C < T_J < 150°C			20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W COM (Including Surge Voltage)	4		4	V
$PW_{IN(ON)}$	Minimum Input Pulse Width	(Note 7)	0.7			μs
$PW_{IN(OFF)}$			0.7			

7. This product might not make response if input pulse width is less than the recommended value.

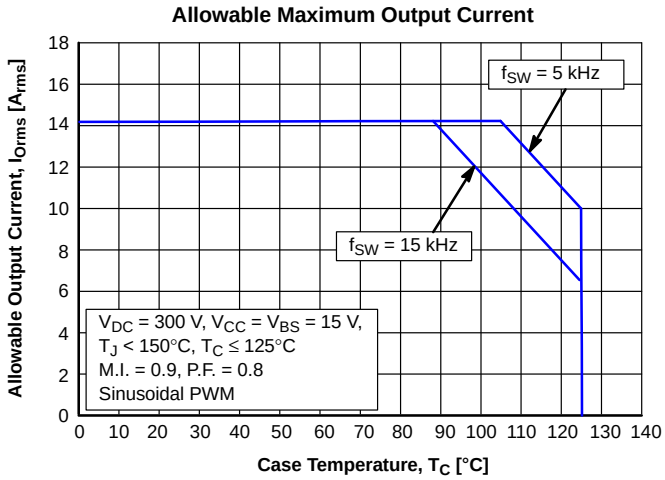


Figure 8. Allowable Maximum Output Current

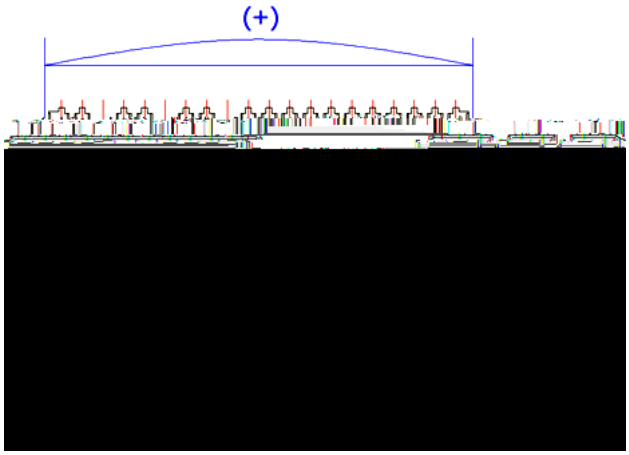
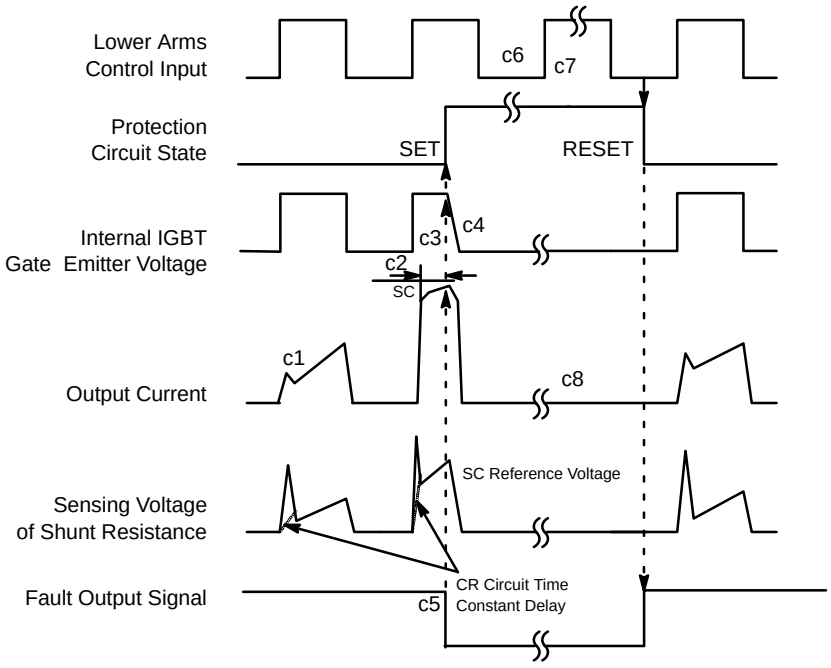


Figure 9. Flatness Measurement Position



(with the external sense resistance and CR connection)

c1: Normal operation: IGBT ON and carrying current.

c2: Short circuit current detection (SC trigger).

c3: Hard IGBT gate interrupt.

c4: IGBT turns OFF.

c5: Input “LOW”:IGBT OFF state.

c6: Input “HIGH”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON.

c7: IGBT OFF state.

Figure 14. Short−Circuit Protection (Low−Side Operation Only)

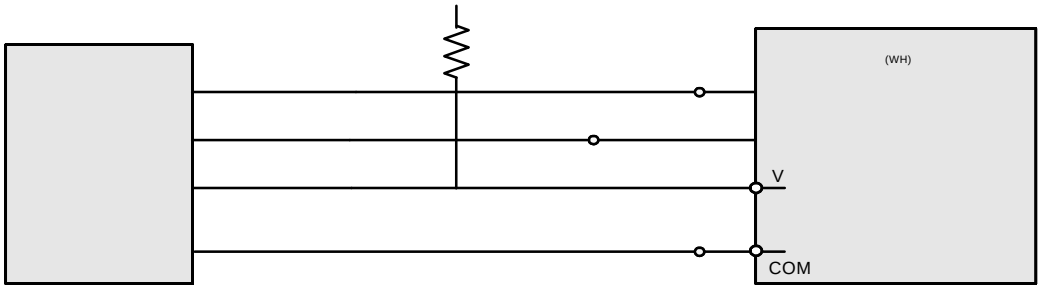


Figure 15. Recommended MCU I/O Interface Circuit

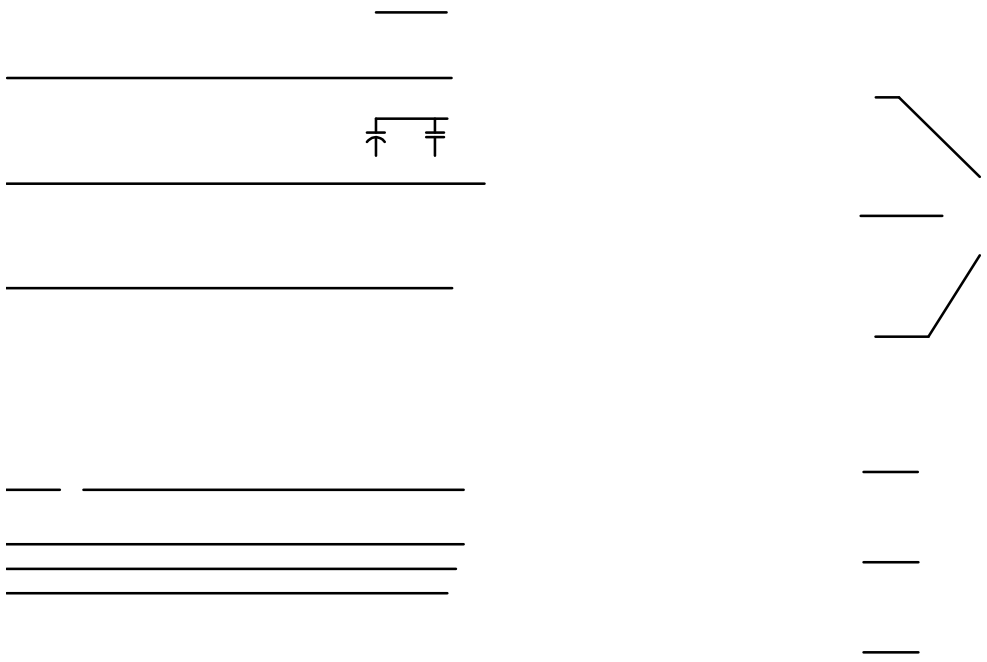


Figure 16. Typical Application Circuit