





EMI DOCT R



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	V _{DD1}	Input Supply Voltage
2	V _I	Input Data
3		LED Anode – must be left unconnected
4	GND1	Input Ground
5	GND2	Output Ground
6	V _O	Output Data
7	NC	Not Connected
8	V _{DD2}	Output Supply Voltage

Absolute Maximum Ratings (T_A = 25°C unless otherwise specified.)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
T _{STG}	Storage Temperature	-40 to +125	°C
T _{OPR}	Operating Temperature	-40 to +100	°C
T _{SOL}	Lead Solder Temperature	260 for 10 sec	°C
	Reflow Temperature Profile (Refer to Relow Profile)		
V _{DD1}	Input Supply Voltage	0 to 6.0	V
V _I	Input Voltage	-0.5 to V _{DD1} + 0.5	V
I _I	Input DC Current	-10 to +10	mA
V _{DD2}	Output Supply Voltage	0 to 6.0	V
V _D	Output Voltage	-0.5 to V _{DD2} + 0.5	V
I _O	SOL		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

- A 0.1µF bypass capacitor must be connected between pins 1 and 4, and 5 and 8
- Pin 3 must be left unconnected

Electrical Characteristics ($T_A = -40^\circ\text{C}$ to 100°C and $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$, all typicals are at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$)



Isolation Characteristics ($T_A = -40^\circ\text{C}$ to $+100^\circ\text{C}$ unless otherwise specified.)

Switching Characteristics ($T_A = -40^\circ\text{C}$ to 100°C and $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$, all typicals are at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Delay Time to Logic Low Output	$C_L = 15\text{pF}$		21	40	ns
t_{PLH}	Propagation Delay Time to Logic High Output	$C_L = 15\text{pF}$		23	40	ns
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $					
	FOD0710	PW = 80ns, $C_L = 15\text{pF}$		2	8	ns
	FOD0720	PW = 40ns, $C_L = 15\text{pF}$		2	8	ns
	FOD0721	PW = 40ns, $C_L = 15\text{pF}$		2	6	ns
Data Rate	FOD0710				12.5	Mb/s
	FOD0720, FOD0721				25	Mb/s
t_{PSK}	Propagation Delay Skew	$C_L = 15\text{pF}^{(3)}$			20	ns
t_R	Output Rise Time (10%–90%)			5		ns
t_F	Output Fall Time (90%–10%)			4.5		ns
$ CM_H $	Common Mode Transient Immunity at Output High	V_I				

Notes:

- t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
- Common mode transient immunity at output high is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode impulse signal. V_{cm} , to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable (negative dV_{cm}/dt on the trailing edge of the common pulse signal, V_{cm} , to assure that the output will remain low.

Typical Performance Curves

Figure 1. Typical Output Voltage vs. Input Voltage

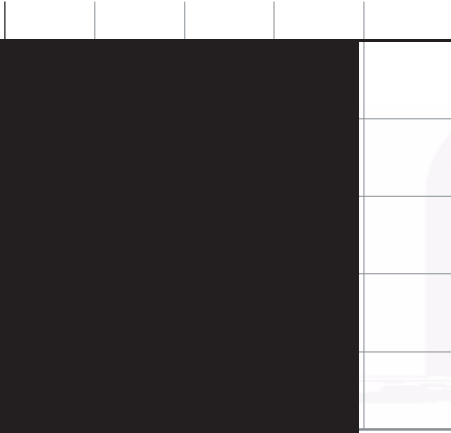
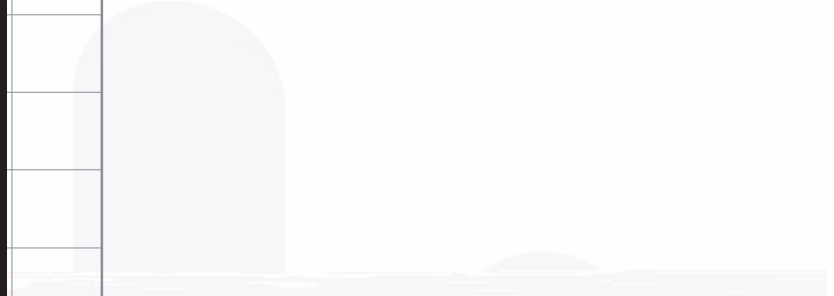


Figure 2. Typical Input Voltage Switching Threshold vs. Input Supply Voltage



Temperature

Figure 4. Typical Pulse Width Distortion vs. Ambient Temperature (FOD0710)

Temperature

Figure 6. Typical Pulse Width Distortion vs. Ambient Temperature (FOD0721/FOD0720)



Typical Performance Curves (Continued)

Figure 13. Typical Rise and Fall Time vs. Output Load Capacitance (FOD0721/FOD0720)


Figure 14. Typical Input Supply Current vs. Frequency



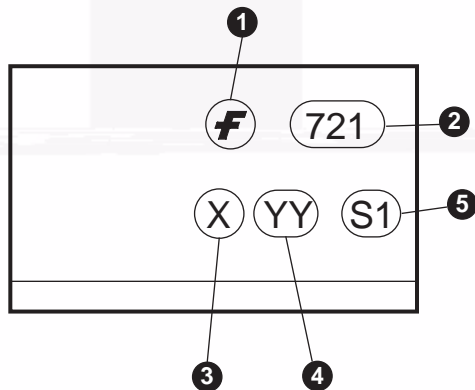
Figure 15. Typical Output Supply Current vs. Frequency

Ordering Information

Option	Order Entry Identifier	Description
No Suffix	FOD0721	Shipped in Tubes (50 units per tube)
R2	FOD0721R2	Tape and Reel (2500 units per reel)

 All packages are lead free per JEDEC: J-STD-020B standard.

Marking Information



Definitions	
1	Fairchild logo
2	Device number
3	One digit year code, e.g., '8'
4	Two digit work week ranging from '01' to '53'
5	Assembly package code

Carrier Tape Specification

Note:

All dimensions are in millimeters.

Reflow Profile

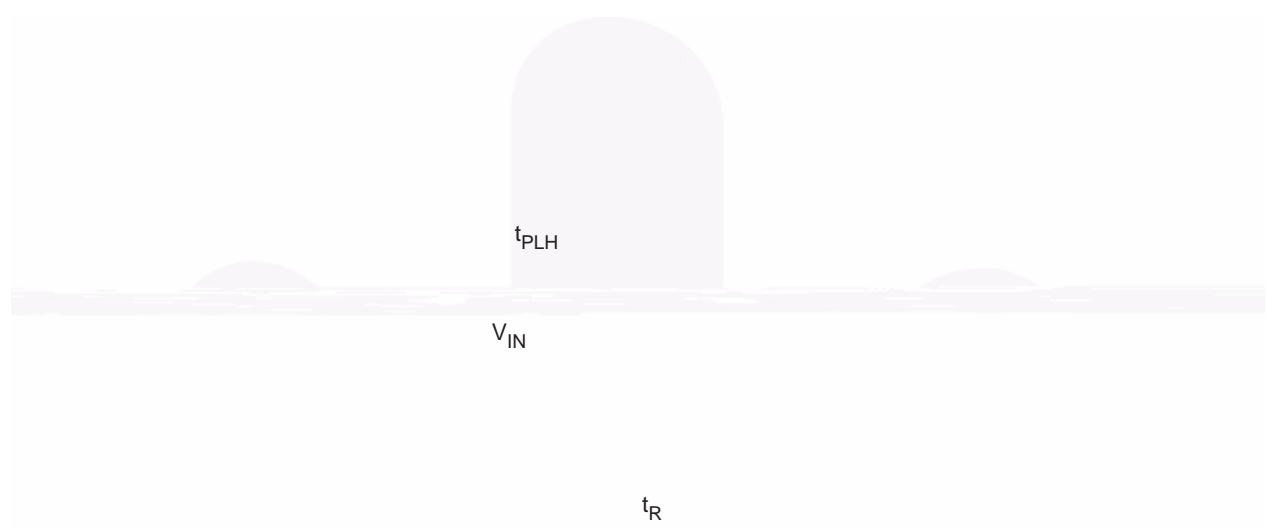


Figure 16. Test Circuit for Propagation Delay Time and Rise Time, Fall Time

Figure 17. Test Circuit for Instantaneous Common Mode Rejection Voltage

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