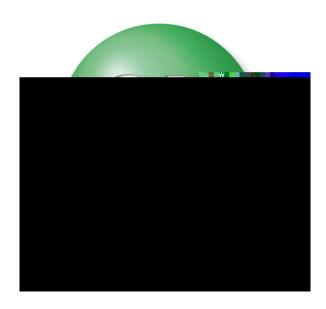


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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild www.onsemi.com.

EMIC NDUCT R

Pin Definitions

Number	Name	Function Description
1	ANODE	Anode
3	CATHODE	Cathode
4	GND	Output Ground
5	V_{O}	Output Voltage
6	V_{CC}	Output Supply Voltage

Safety and Insulation Ratings for Mini-Flat Package (SO5 Pin)

As per IEC60747-5-2 (Pending Certification). This optocoupler is suitable for "safe electrical insulation" only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Тур.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For rated main voltage < 150Vrms		I-IV		
	For rated main voltage < 300Vrms		1-111		
	Climatic Classification		40/85/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V_{PR}	Input to Output Test Voltage, Method b, VIORM x 1.875 = V_{PR} , 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	1060			
V_{PR}	Input to Output Test Voltage, Method a, VIORM x 1.5 = V_{PR} , Type and Sample Test with t_m = 60 sec, Partial Discharge < 5 pC	848			
V_{IORM}	Max Working Insulation Voltage	565			V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	4000			V_{peak}
	External Creepage	5.0			mm
	External Clearance	5.0			mm
	Insulation thickness	0.5			mm
T _{Case}	Safety Limit Values, Maximum Values allowed in the event of a failure, Case Temperature	150			°C
R_{IO}	Insulation Resistance at T_S , $V_{IO} = 500V$	10 ⁹			Ω

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
T _{STG}	Storage Temperature	-40 to +125	°C
T _{OPR}	Operating Temperature	-40 to +85	°C
T_J	Junction Temperature	-40 to +125	°C
T _{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10sec	°C
IF	Forward Current	50	mA
V_{R}	Reverse Voltage	5.0	V
V_{CC}	Supply Voltage	0 to 7.0	V
V_{O}	Output Voltage	-0.5 to V _{CC} +0.5	V
I_{O}	Average Output Current	50	mA
PD_{I}	Input Power Dissipation ⁽¹⁾⁽²⁾	100	mW
PD_O	Output Power Dissipation ⁽¹⁾⁽²⁾	85	mW

Recommended Operating Conditions

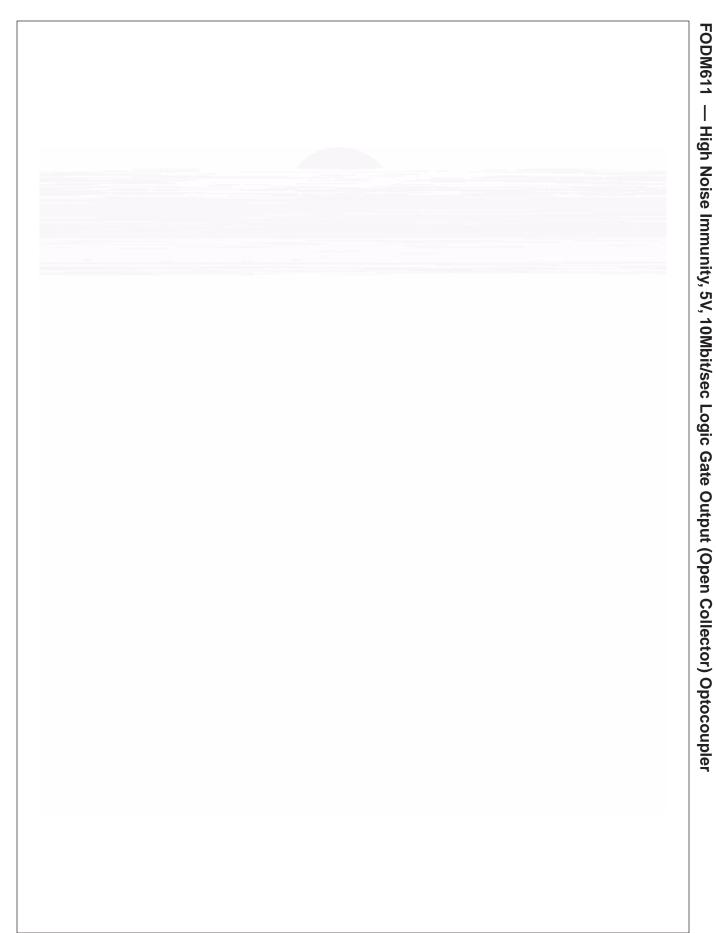
The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	-40	+85	٥C
V_{CC}	Supply Voltages ⁽³⁾	4.5	5.5	V
V_{FL}				

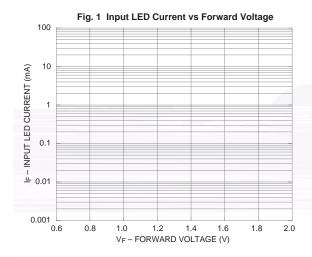
Isolation Characteristics (T_A=25°C)

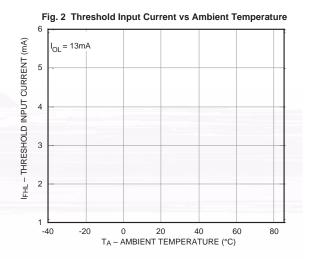
Notes:

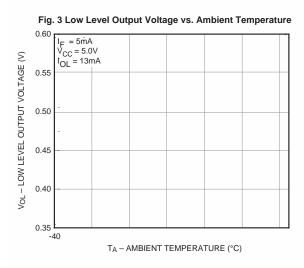
- 1. No derate required to 85°C.
- 2. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.
- 3. 0.1µF bypass capacitor must be connected between pins 4 and 6.
- 4. Device is considered a two terminal device: Pins 1 and 3 are shorted, and Pins 4, 5, and 6 are shorted together.
- 5. 3,750 VAC_{RMS} for 1 minute duration is equivalent to 4,500 VAC_{RMS} for 1 second duration.

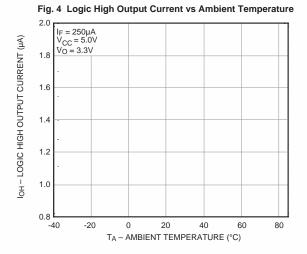


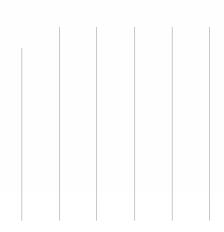
Typical Performance Curves











Typical Performance Curves (Continued)

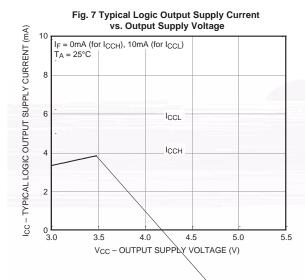


Fig. 8 Typical Propagation Delay vs. Ambient Temperature

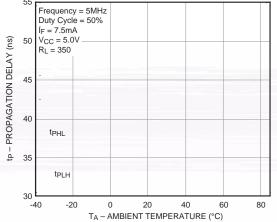


Fig. 9 Pulse Width Distortion vs. Ambient Temperature

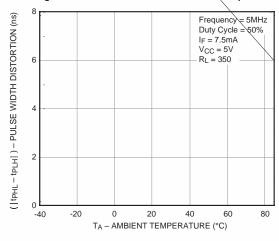
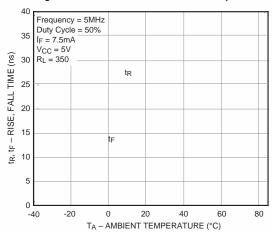


Fig. 10 Rise and Fall Time vs. Ambient Temperature



Schematics

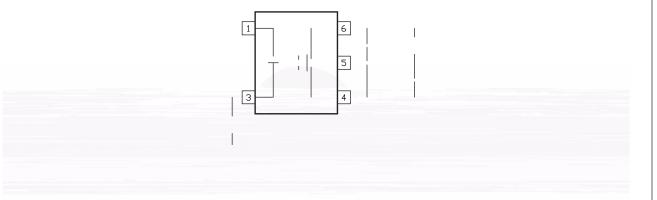


Figure 11. Test Circuit for Propagation Delay Time, Rise Time and Fall Time

Figure 12. Test Circuit for Instantaneous Common Mode Rejection Voltage

Package Dimensions

Notes:

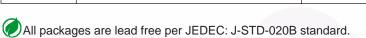
- 1. No standard applies
- 2. All dimensions are
- 3. Dimensions are grant and treatment of the same and the bar extrusion.
- 4. Drawings filesn on: MKT-MFP05A.

Package drawings are previous to customers considering Fairchild components. Drawings may change in any manner without notice. Please non-and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent specifically the warrance which covers Fairchild products.

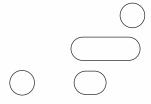
Always visit Faird conductor's online packaging area for the most recent package drawings:

Ordering Information

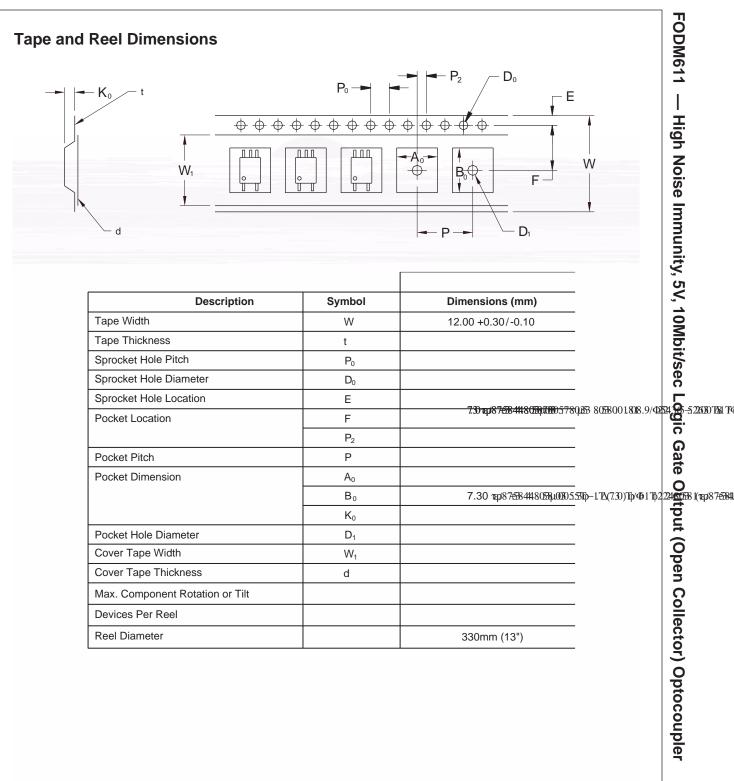
Option	Order Entry Identifier (Example)	Description
No Suffix	FODM611	Mini-Flat 5-pin, shipped in tubes (100 units per tube)
R2	FODM611R2	Mini-Flat 5-pin, tape and reel (2,500 units per reel)



Marking Information

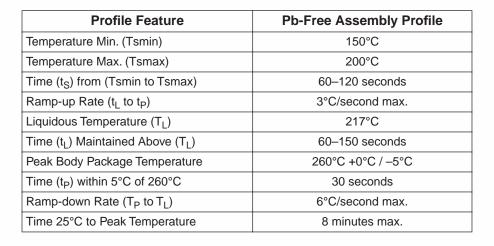


Tape and Reel Dimensions



Description	Symbol	Dimensions (mm)
Tape Width	W	12.00 +0.30/-0.10
Tape Thickness	t	
Sprocket Hole Pitch	P ₀	
Sprocket Hole Diameter	D ₀	
Sprocket Hole Location	E	
Pocket Location	F	7.30 кр/87538 444 8 0530 1000 5 7 8 0 û
	P ₂	
Pocket Pitch	Р	
Pocket Dimension	A ₀	
	B ₀	7.30 1ap/8745844480534u00005551
	K ₀	
Pocket Hole Diameter	D ₁	
Cover Tape Width	W ₁	
Cover Tape Thickness	d	
Max. Component Rotation or Tilt		
Devices Per Reel		
Reel Diameter		330mm (13")





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CTL ISOPF282A.**0**9l(ie)-8.6(sMsTj/T(®)Tj7.**6**6 **0**)96Td**0**e**6g**2**度**

Current Transfer Logic

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