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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

August 2016

FSA2275 / FSA2275A ð DPDT (0.5) HiFi Audio Switch w/ Negative Swing

Features

V_{DD} Operating Range: 2.5 to 5.5 V

External Capacitor Connection for Pop and Click Noise Suppression

Power-Off Protection on Common Ports

R_{ON} = 0.5 Ω (Typ.) at 2.5 V V_{DD}

THD+N = -105 dB; 2 V_{RMS}, 20 kΩ Load; f = 1 kHz

X_{TALK} = -134 dB at 1 $V_{RMS,}$ 50 Ω Load; f = 1 kHz

Off Isolation = -103 dB at 1 $V_{RMS,}$ 50 Ω Load; f = 1 kHz

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FSA2275A features ultra-low audio R_{ON} of 0.5 (typical) at 2.5 V V_{CC}. The FSA2275 / FSA2275A operates over a V_{CC} range of 2.5 V to 5.5 V, is fabricated with sub-micron CMOS technology to achieve fast switching speeds, and is designed for break-before-make operation. To minimize pop and

Pin Configuration

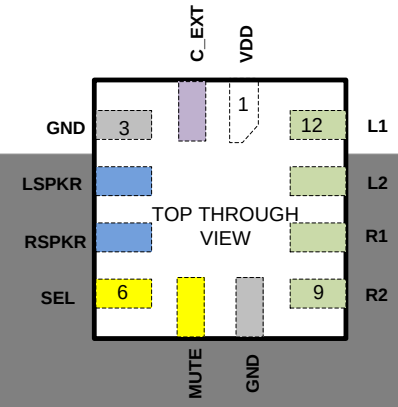


Figure 2. Pin Assignment (Top Through View)

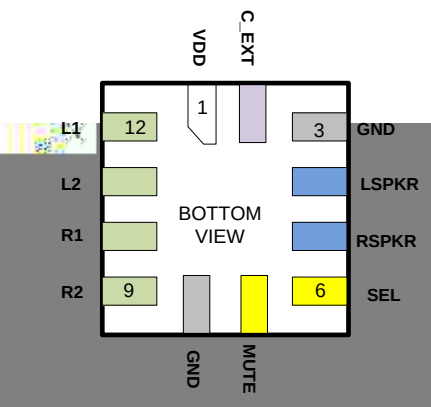
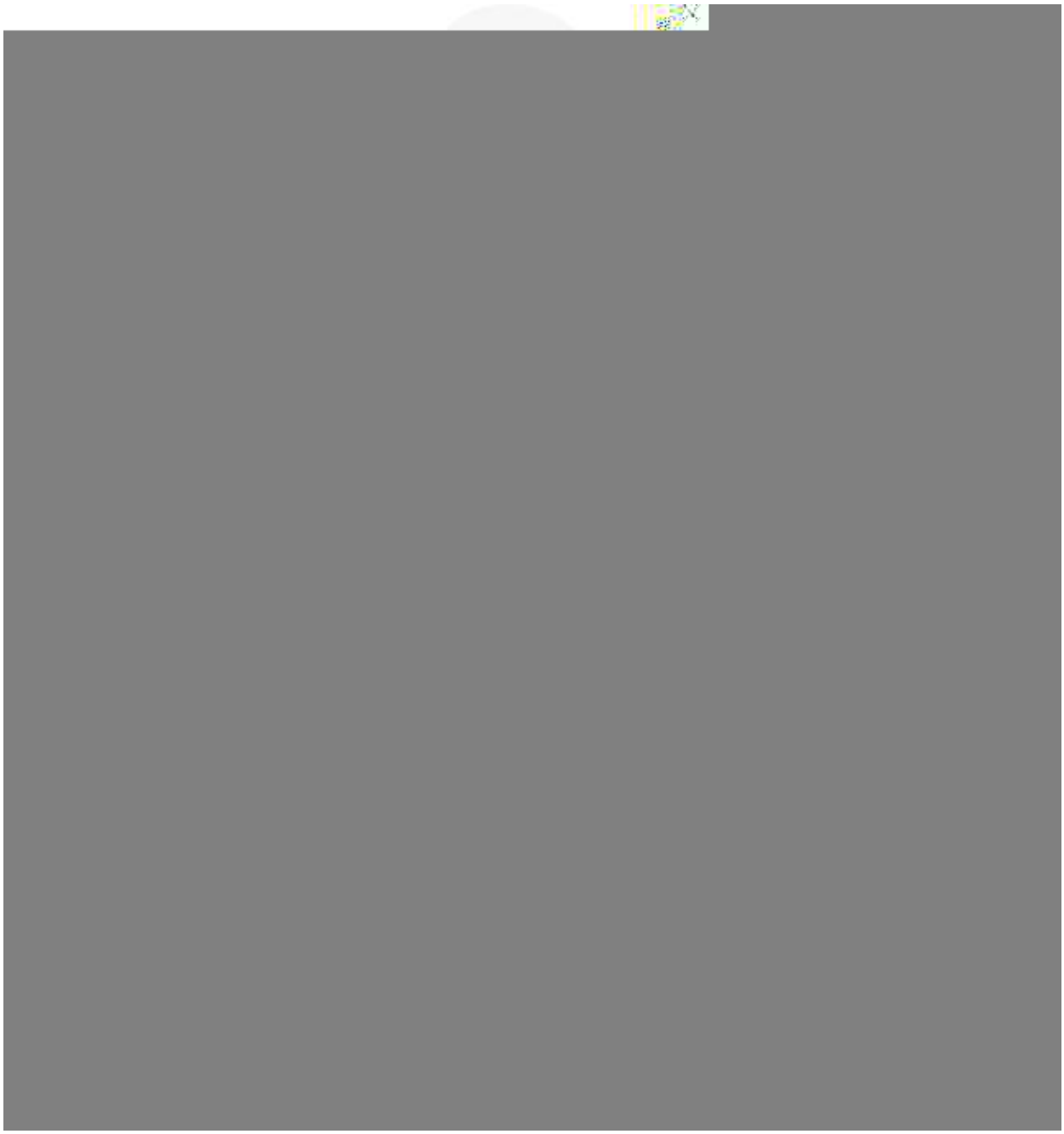


Figure 3. Pin Assignment (Bottom View)

Pin Descriptions

Pin	Name	Description
1	VDD	Power Supply (2.5 to 5.5 V)
2	C_EXT	Slow Turn On External Capacitor
3	GND	Ground
4	L_{SPKR}	Audio L_{SPPKR} Common I/O Port
5	R_{SPKR}	Audio R_{SPPKR} Common I/O Port
6	SEL	Select Pin
7	MUTE	Mute Enable - Active High
8	GND	Ground
9	R2	Audio – Right Channel Source2 I/O Port
10	R1	Audio – Right Channel Source1 I/O Port

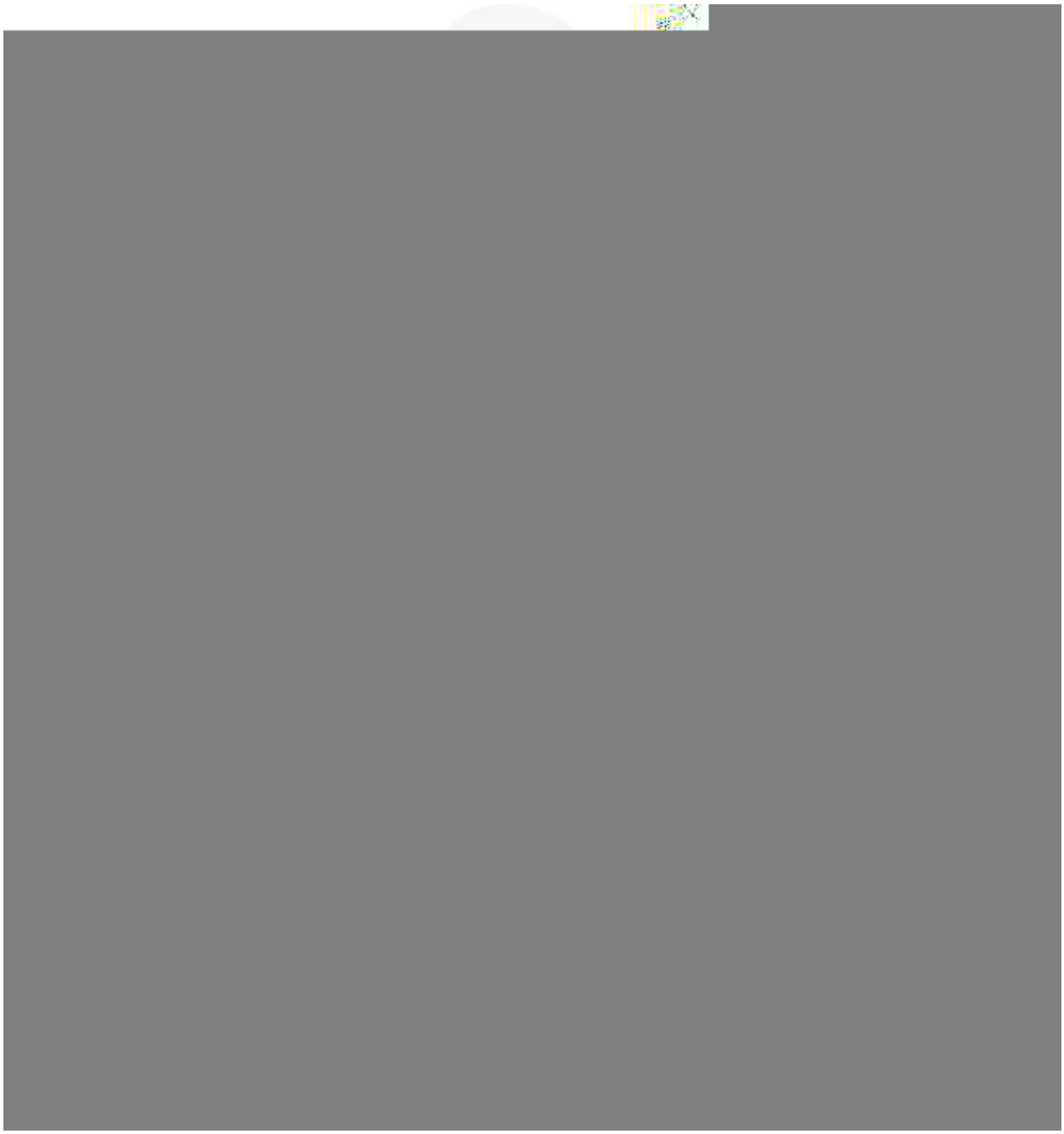
Absolute Maximum Ratings



AC Characteristics

V_{DD} = 2.5 V to 5.5 V, V_{DD} (Typ.) = 3.3 V. T_A = -40°C to 85°C. T_A (Typ.) = 25°C, unless otherwise specified

Symbol	Parameter	Condition	V_{DD} (V)	T_A=- 40°C to +85°C Min.	Unit
[redacted]					



Test Diagrams

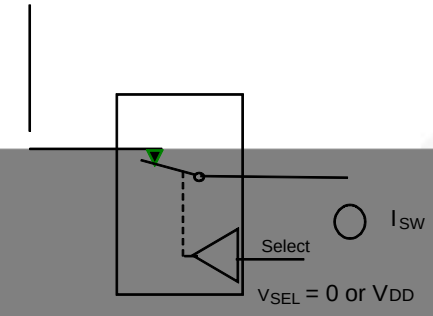


Figure 4. On Resistance

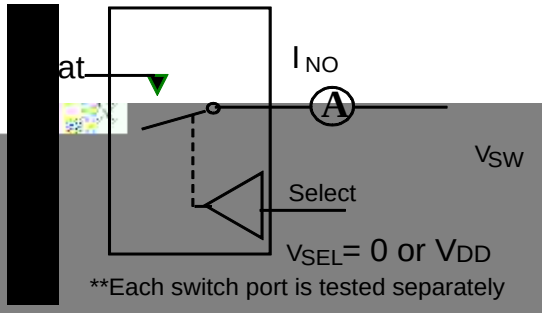


Figure 5. Off Leakage

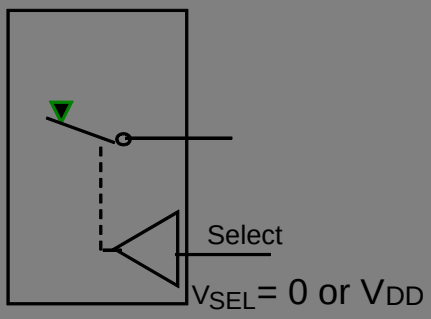


Figure 6. On Leakage

R_L

Figure 7. Test Circuit Load

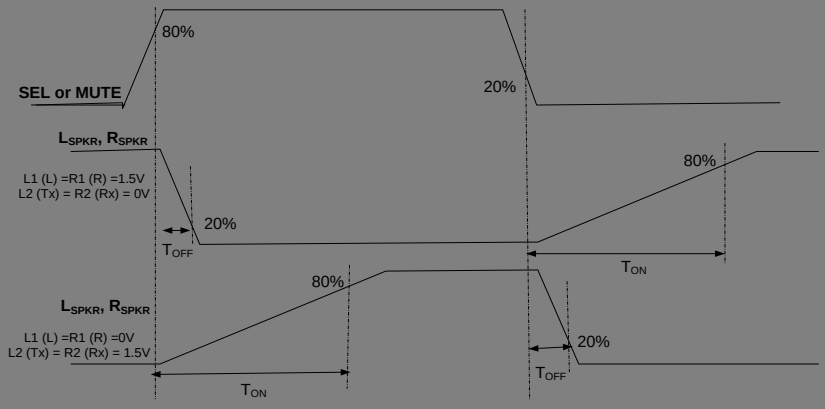


Figure 8. Turn On/Off Waveforms (SEL or MUTE to Output)

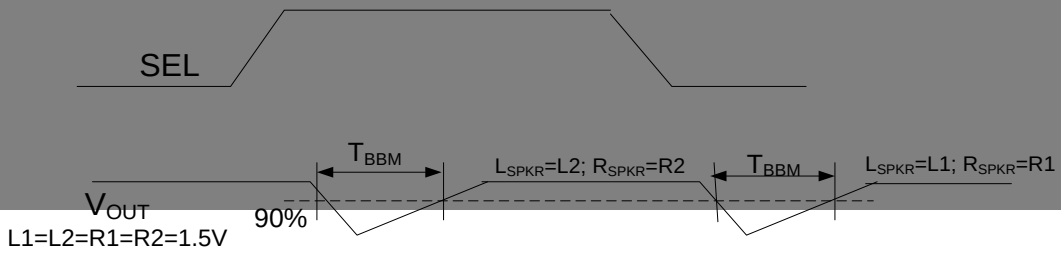
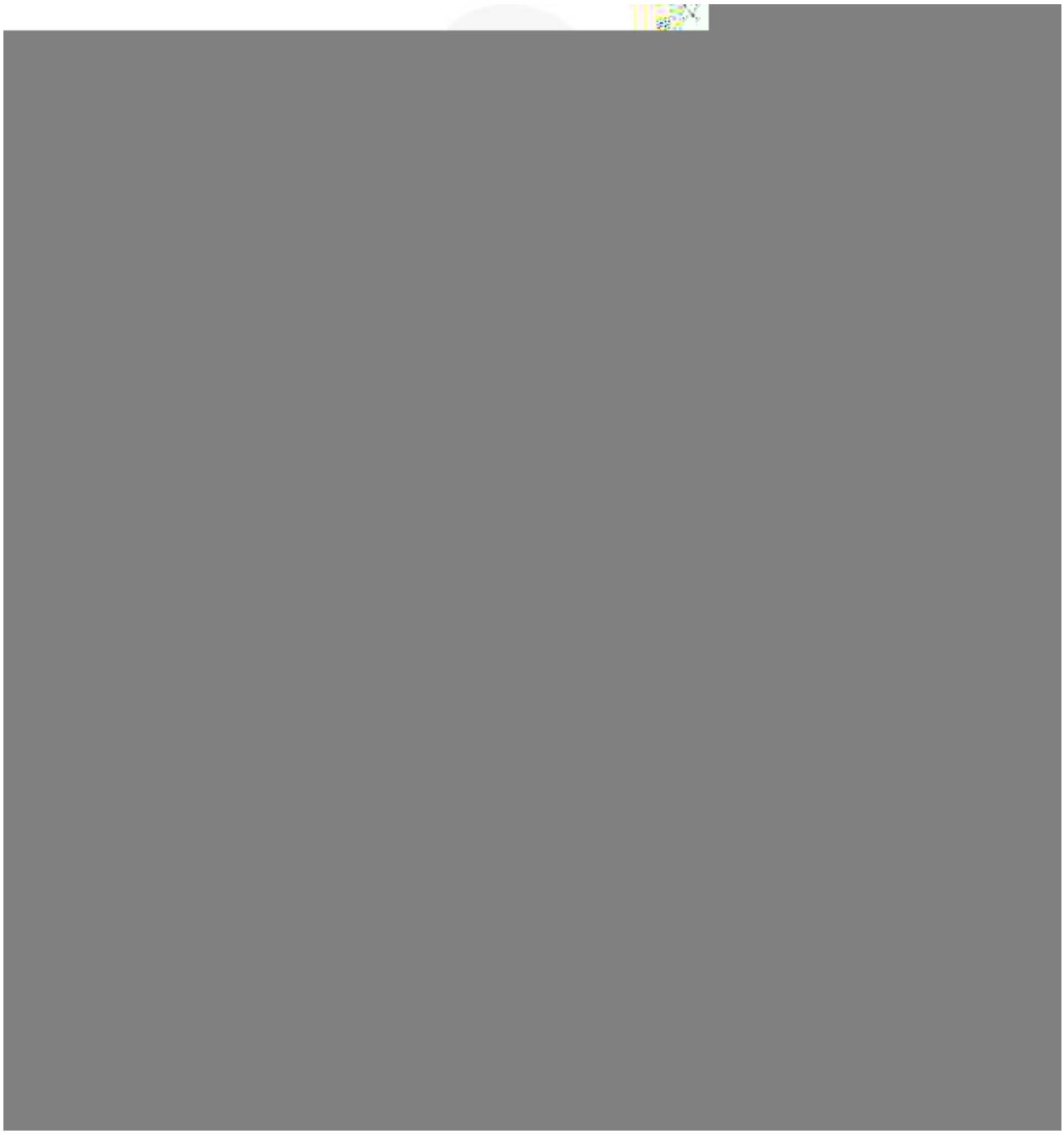
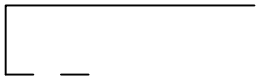


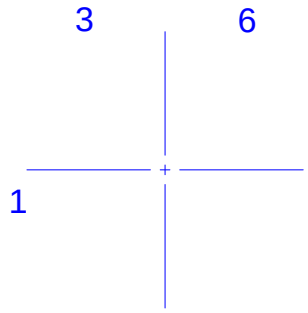
Figure 9. Break Before Make Interval Timing





RECOMMENDED LAND PATTERN

SIDE VIEW



DETAIL A
SCALE 2:1

BOTTOM VIEW

NOTES:

A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
D. DRAWING FILENAME: MKT-UMLP12ArevF

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