

# Low-Power, Dual SIM Card Analog Switch

## FSA2567

### Description

The FSA2567 is a bi-directional, low-power, dual double-pole, double-throw (4PDT) analog switch targeted at dual SIM card multiplexing. It is optimized for switching the WLAN-SIM data and control signals and dedicates one channel as a supply-source switch.

The FSA2567 is compatible with the requirements of SIM cards and features a low on capacitance ( $C_{ON}$ ) of 10 pF to ensure high-speed data transfer. The  $V_{SIM}$  switch path has a low  $R_{ON}$  characteristic to ensure minimal voltage drop in the dual SIM card supply paths.

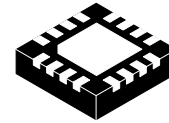
The FSA2567 contains special circuitry that minimizes current consumption when the control voltage applied to the SEL pin is lower than the supply voltage ( $V_{CC}$ ). This feature is especially valuable in ultra-portable applications, such as cell phones; allowing direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

### Features

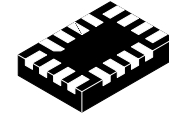
- Low On Capacitance for Data Path: 10 pF Typical
- Low On Resistance for Data Path: 6  $\Omega$  Typical
- Low On Resistance for Supply Path: 0.4  $\Omega$  Typical
- Wide  $V_{CC}$  Operating Range: 1.65 V to 4.3 V
- Low Power Consumption: 1  $\mu$ A Maximum
  - ◆ 15  $\mu$ A Maximum  $I_{CCT}$  Over Expanded Voltage Range ( $V_{IN} = 1.8$  V,  $V_{CC} = 4.3$  V)
- Wide -3 db Bandwidth: >160 MHz
- Packaged in:
  - ◆ Pb-free 16-Lead MLP & 16-Lead UMLP
- 3 kV ESD Rating, >12 kV Power/GND ESD Rating

### Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

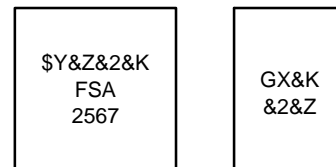


WQFN16 3x3, 0.5P  
CASE 510BS



UQFN16 1.8x2.6, 0.4P  
CASE 523BF

### MARKING DIAGRAM



GX, FSA2567 = Device Code  
 \$Y = onsemi Logo  
 &Z = Assembly Plant Code  
 &2 = 2-Digit Date Code  
 &K = 2-Digits Lot Run Traceability Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FSA2567

## ORDERING INFORMATION

Part Number	Top Mark	Operating Temperature Range	Package	Shipping†
FSA2567MPX	FSA2567	-40 to +85°C	16-Lead, Molded Leadless Package (MLP) Quad, JEDEC MO-220, 3 mm Square	3000 / Tape & Reel
FSA2567UMX	GX		16-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.8 x 2.6 mm	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# FSA2567

## TRUTH TABLE

Sel	Function
Logic LOW	1DAT = DAT, 1RST = RST, 1CLK = CLK, 1V <sub>SIM</sub> = V <sub>SIM</sub>
Logic HIGH	2DAT = DAT, 2RST = RST, 2CLK = CLK, 2V <sub>SIM</sub> = V <sub>SIM</sub>

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage			

# FSA2567

**DC ELECTRICAL CHARACTERISTICS** (All typical values are at 25°C, 3.3 V  $V_{CC}$  unless otherwise specified.)

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$			Unit
				Min	Typ	Max	
$V_{IK}$	Clamp Diode Voltage	$I_{IN} = -18 \text{ mA}$					

# FSA2567

## AC ELECTRICAL CHARACTERISTICS (All typical values are for $V_{CC} = 3.3\text{ V}$ at $25^\circ\text{C}$ unless otherwise specified.)

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$			Unit
				Min	Typ	Max	
$t_{OND}$	Turn-On Time Sel to Output (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW} = 1.5\ \text{V}$ Figure 11, Figure 12	1.8 (Note 5)	–	65	95	ns
			2.7 to 3.6	–	42	60	ns
$t_{OFFD}$	Turn-Off Time Sel to Output (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW} = 1.5\ \text{V}$ Figure 11, Figure 12	1.8 (Note 5)	–	30	50	ns
			2.7 to 3.6	–	20	40	ns
$t_{ONV}$	Turn-On Time Sel to Output ( $V_{SIM}$ )	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW} = 1.5\ \text{V}$ Figure 11, Figure 12	1.8 (Note 5)	–	55	80	ns
			2.7 to 3.6	–	35	55	ns
$t_{OFFV}$	Turn-Off Time Sel to Output ( $V_{SIM}$ )	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW} = 1.5\ \text{V}$ Figure 11, Figure 12	1.8 (Note 5)	–	35	50	
			2.7 to 3.6	–	22	40	ns
$t_{PD}$	Propagation Delay (Note 5) (DAT, CLK, RST)	$C_L = 35\ \text{pF}$ , $R_L = 50\ \Omega$ Figure 11, Figure 13	3.3	–	0.25	–	ns
$t_{BBMD}$	Break-Before-Make (Note 5) (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW1} = V_{SW2} = 1.5\ \text{V}$ Figure 15	2.7 to 3.6	3	18	–	ns
$t_{BBMV}$	Break-Before-Make (Note 5) ( $V_{SIM}$ )	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW1} = V_{SW2} = 1.5\ \text{V}$ Figure 15	2.7 to 3.6	3	12	–	ns
Q	Charge Injection (DAT, CLK, RST)	$C_L = 50\ \text{pF}$ , $R_{GEN} = 0\ \Omega$ , $V_{GEN} = 0\ \text{V}$	2.7 to 3.6	–	10	–	pC
$O_{IRR}$	Off Isolation (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $f = 10\ \text{MHz}$ Figure 17	2.7 to 3.6	–	–60	–	dB
Xtalk	Non-Adjacent Channel Crosstalk (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $f = 10\ \text{MHz}$ Figure 18	2.7 to 3.6	–	–60	–	dB
BW	–3 db Bandwidth (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ Figure 16	2.7 to 3.6	–	475	–	MHz

5. Guaranteed by characterization.

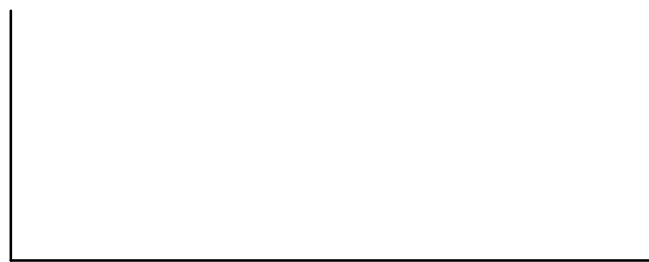
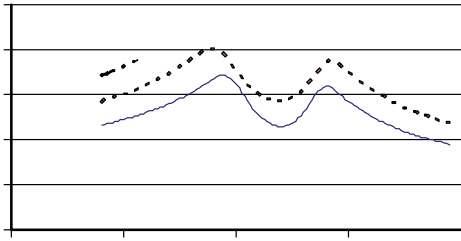
## CAPACITANCE

Symbol	Parameter	Conditions	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$			Unit
			Min	Typ	Max	
$C_{IN}$	Control Pin Input Capacitance	$V_{CC} = 0\ \text{V}$	–	1.5	–	pF
$C_{OND}$	RST, CLK, DAT On Capacitance (Note 6)	$V_{CC} = 3.3\ \text{V}$ , $f = 1\ \text{MHz}$ , Figure 20	–	10	12	
$C_{ONV}$	$V_{SIM}$ On Capacitance (Note 6)	$V_{CC} = 3.3\ \text{V}$ , $f = 1\ \text{MHz}$ , Figure 20	–	110	150	
$C_{OFFD}$	RST, CLK, DAT Off Capacitance	$V_{CC} = 3.3\ \text{V}$ , Figure 19	–	3	–	
$C_{OFFV}$	$V_{SIM}$ Off Capacitance	$V_{CC} = 3.3\ \text{V}$ , Figure 19	–	40	–	

6. Guaranteed by characterization.

# FSA2567

## TYPICAL PERFORMANCE CHARACTERISTICS



Frequency (MHz)  
 $C_L = 5 \text{ pF}$ ,  $V_{CC} = 2.7 \text{ V}$

# FSA2567

## TEST DIAGRAMS

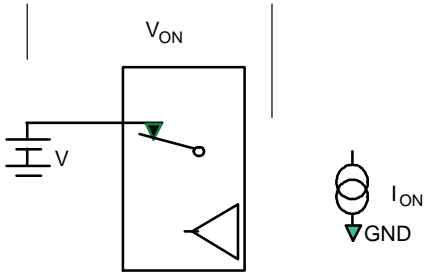


Figure 9. On Resistance

Figure 10. Off Leakage

**Figure 15. Break–Before–Make Interval Timing**

**Figure 16. Bandwidth**

**Figure 17. Channel Off Isolation**

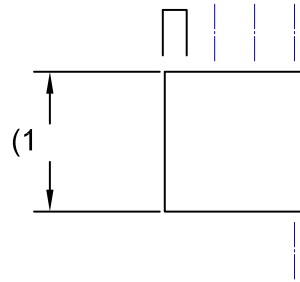
**Figure 18. Non–Adjacent Channel–to–Channel Crosstalk**



WQFN16 3x3, 0.5P  
CASE 510BS  
ISSUE O

DATE 31 AUG 2016

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**UQFN16 1.80x2.60x0.50, 0.40P**  
CASE 523BF  
ISSUE A

DATE 06 MAY 2024

L4      0.45      0.50       $\frac{\varnothing.45}{0.55}$

TOLERANCES FOR FEATURE C/D

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