

FSA3051 — High Performance SPDT Analog Switch with Over-Voltage Tolerance

Features

- Low On Capacitance: 7.7 pF Typical
- Low On Resistance: 6 Ω Typical
- Low Power Consumption: 1 μ A Maximum
 - 15 μ A Maximum I_{CC} over an Expanded Voltage Range ($V_{IN}=1.8$ V, $V_{CC}=5.5$ V)
- Wide -3 db Bandwidth: 1.0 GHz
- Packaged in Ultra Small 6-Lead TMLP
- Broad V_{CC} Operating Range: 1.6 V to 5.5 V
- Over-Voltage Tolerance (OVT) on all Data Ports up to 6 V without External Components

Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Description

The FSA3051 is a 6 pin, bi-directional, low-power, two-port, high-speed, Single Pole / Double Throw (SPDT) analog switch. It features an extremely low on capacitance (C_{ON}) of 7.7 pF and wide bandwidth of 1.0 GHz.

The FSA3051 contains special circuitry on the switch I/O pins for applications where the V_{CC} supply is powered-off ($V_{CC}=0$ V), which allows the device to withstand an over-voltage condition. This device is designed to minimize current consumption even when the control voltage applied to the select (S) pin is lower than the supply voltage (V_{CC}). This feature is especially

Analog Symbols

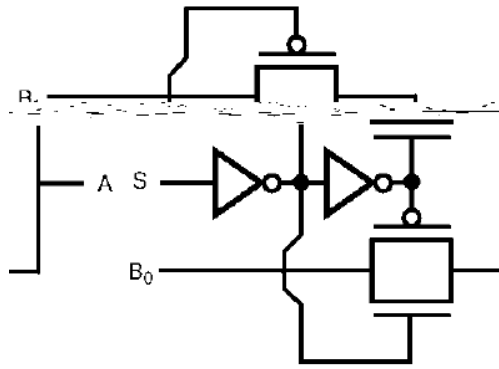


Figure 1. Logic Symbol

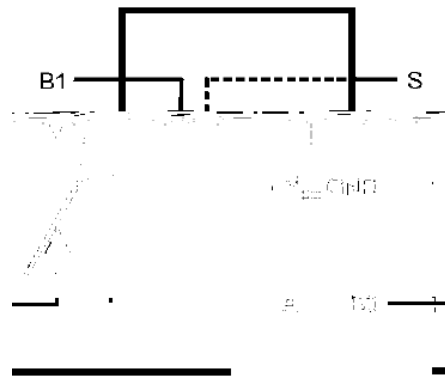


Figure 2. Analog Symbol

Pin Assignments

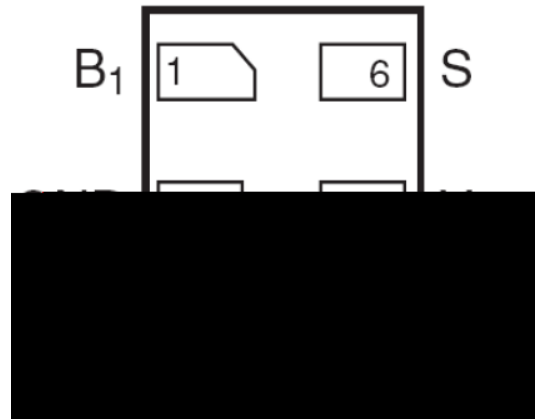


Figure 3. 6-Lead TMLP (Top-Through View)

Pin Definitions

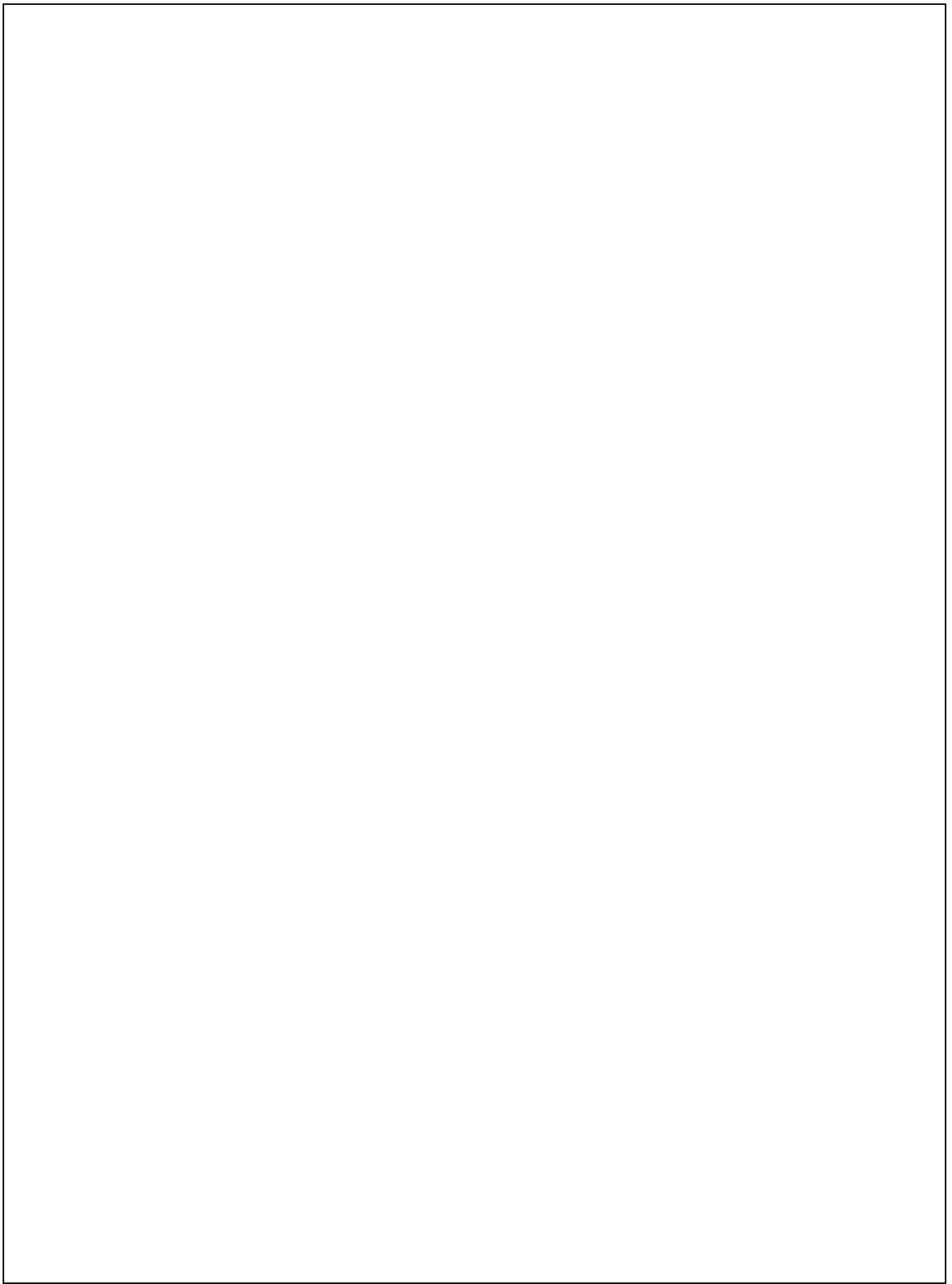
UMLP Pin#	Name	Description
1	B ₁	Data Port
2	GND	Ground
3	B ₀	Data Port
4	A	Data Port
5	V _{CC}	Supply Voltage
6	S	Switch Select

Truth Table

S	Function
LOW	B ₀ connected to A
HIGH	B ₁ connected to A

Notes:

1. LOW V_{IL}.
2. HIGH V_{IH}.



DC Electrical Characteristics

All typical value are at $T_A=25^\circ\text{C}$ unless otherw ise specified.

Symbol	Parameter	Condition	V_{CC} (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	$I_{IN}=-18$ mA	3.0			-1.2	V
V_{IH}	Input Voltage High		1.8 to 4.3	1.3			V
			4.3 to 5.5	1.7			
V_{IL}	Input Voltage Low		1.8 to 4.3			0.5	V
			4.3 to 5.5			0.7	
I_{IN}	Control Input Leakage	$V_{CNTRL}=0$ to V_{CC}	1.8	-1		1	μA
			5.5	-1		1	
I_{OZ}	Off State Leakage	$V_{SW}=0$ V to V_{CC}	1.8	-2		2	μA
		$V_{SW}=0$ V to 3.6 V	5.5	-2		2	
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	$V_{SW}=0$ V to 4.3 V, $V_{CC}=0$ V Figure 5	0	-2		2	μA
R_{ON}	Switch On Resistance ⁽⁵⁾	$V_{SW}=0.4$ V, $I_{ON}=-8$ mA Figure 4	3.0			4	Ω
		$V_{SW}=1.8$ V, $I_{ON}=-8$ mA Figure 4	3.0			6	
R_{ON}	Switch On Resistance ⁽⁵⁾	$V_{SW}=0.4$ V, $I_{ON}=-8$ mA Figure 4	1.8			6	Ω
		$V_{SW}=1.8$ V, $I_{ON}=-8$ mA Figure 4	1.8			14	
R_{ON}	On Resistance Match Between Channels ^(5,6)	$V_{SW}=0.4$ V, $I_{ON}=-8$ mA	3.0			35	m Ω
			1.8			40	
I_{CC}	Quiescent Supply Current	$V_{CNTRL}=0$ or V_{CC} , $I_{OUT}=0$	5.5			1	μA
I_{CCT}	Increase in I_{CC} Current per Control Voltage and V_{CC}	$V_{CNTRL}=1.8$ V	3.0			10	μA
		$V_{CNTRL}=2.6$ V	5.5			10	

.294.4 Tm [(=)0.2(1)-27.5(,)32.7/MCID

AC Electrical Characteristics⁽⁸⁾

All typical value are for $V_{CC}=3.3\text{ V}$ at $T_A=25^\circ\text{C}$ unless otherwise specified.

t_{ON}	Turn-On Time S to Output	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{SW}=0.8\ \text{V}$, Figure 6, Figure 7	3.0 to 3.6 1.8	34 110	ns
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Test Diagrams (Continued)

Figure 9. Break-Before-Make Interval Timing

Figure 10. Bandwidth

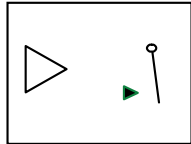


Figure 11. Channel Off Isolation

V_{OUT}

Figure 12. Channel-to-Channel Crosstalk

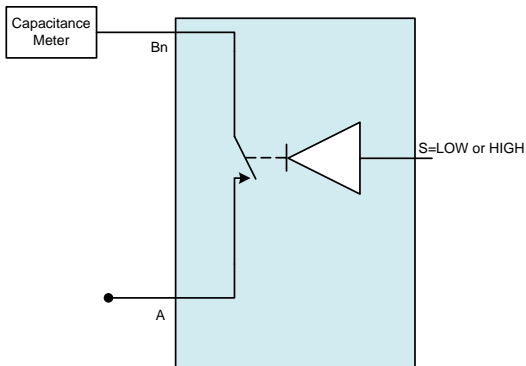


Figure 13. Channel Off Capacitance

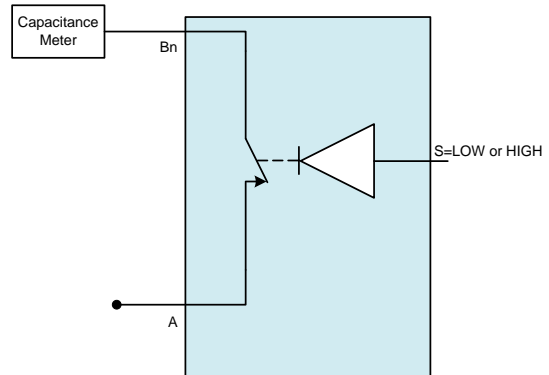


Figure 14. Channel On Capacitance

Carrier Tape Orientation

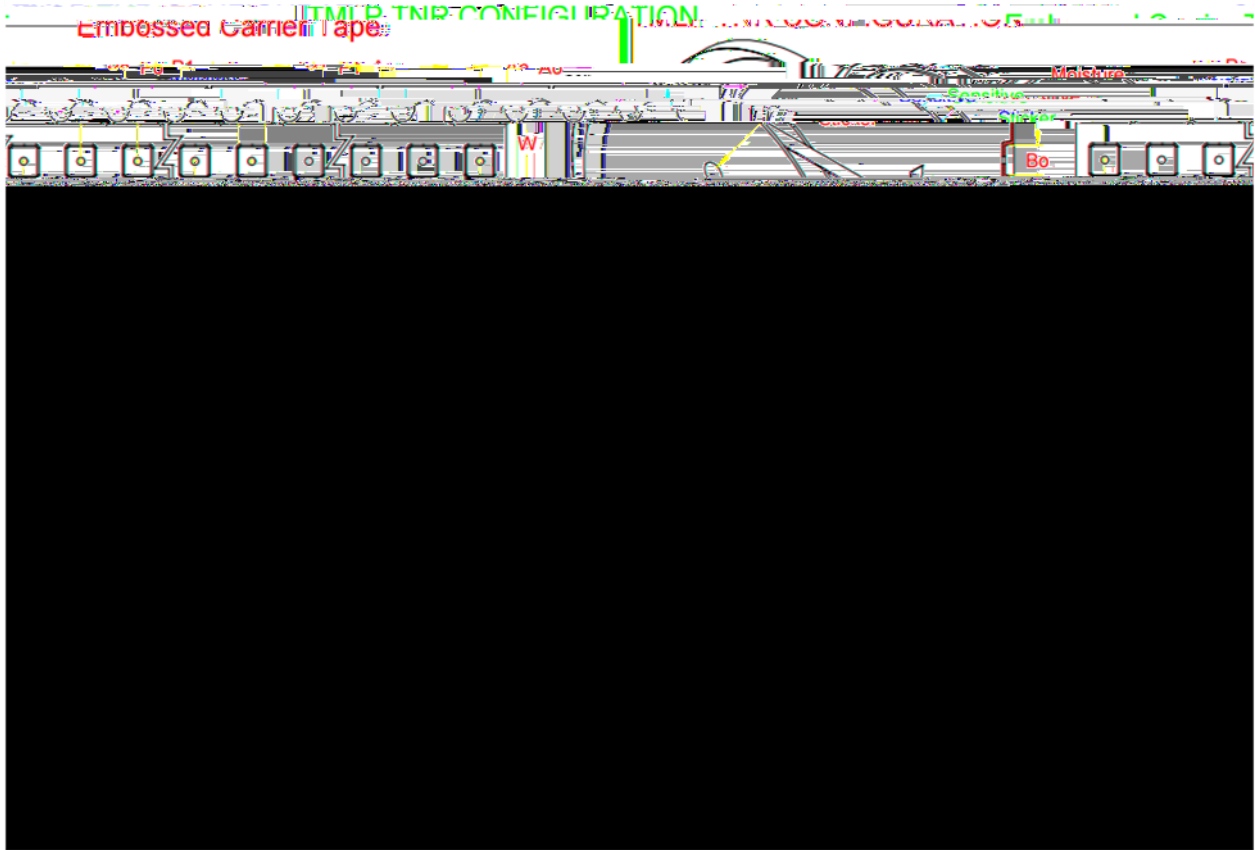
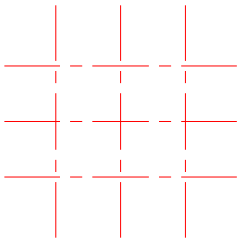
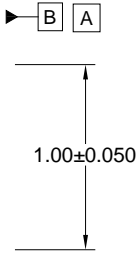
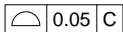


Figure 15. TMLP Carrier Tape Packing

Part Number	Unit Orientation
FSA3051TMX	Top Left
FSA3051TMX-F147	Bottom Left

Physical Dimensions



- NOTES:
- A. NO JEDEC STANDARD APPLIES
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

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