USB Type-C® Analog Audio Switch with Protection Function

FSA4480

Description

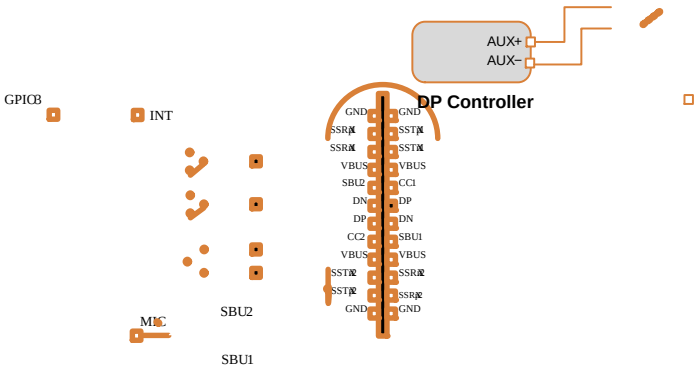
FSA4480 is a high performance USB Type−C port multimedia switch which supports analog audio headsets. FSA4480 allows the sharing of a common USB Type−C port to pass USB2.0 signal, analog audio, sideband use wires and analog microphone signal. FSA4480 also supports high voltage on SBU port and USB port on USB Type−C receptacle side.

Features

Power Supply: V_{CC}, 2.7 V to 5.5 V

USB High Speed (480 Mbps) Switch:

SDD_{21}



MAR

6D = Specific
&K = 2−digits
&2 = 2−digits
&Z = Assembly
J− = X− Coord
P = Y Coordi
UU = Two Digit
*For **onsemi** inter

ORDERI

Part Number
FSA4480UCX

Table 1. PIN DESCRIPTIONS

No.	Pin	Name	Description
1	A5	VCC	Power Supply (2.7 to 5.5 V)
2	B5	GND	Chip ground
3	D5	DP_R	USB/Audio Common Connector
4	D4	DN_L	USB/Audio Common Connector
5	E5	DP	USB Data (Differential +)
6	E4	DN	USB Data (Differential –)
7	C5	R	Audio – Right Channel
8	C4	L	Audio – Left Channel
9	A3	SBU1	Sideband use wire 1
10	A2	SBU2	Sideband use wire 2
11	C1	MIC	Microphone signal
12	B2	AGND	Audio signal ground
13	B94 522.709 -754 522.7o307 p 600.378 .90709 15n4, 0 8 126.2551 514[.84d 600.378 .9071 15.307 ref 6rm8 1O2[01192,23MIC		

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage from VCC	−0.5	6.5	V
V_{CC_IN}	V_{CC_IN}, to GND	−0.5	20	V
V_{SW_C}	V_{DP_R} to GND, V_{DN_L} to GND	−3.5	20	V
V_{SW_USB}	V_{DP} to GND, V_{DN} to GND	−0.5	6.5	V
V_{SW_Audio}	V_L to GND, V_R to GND	−3.6	6.5	V
$V_{V\_SBU/GSBU}$	V_{SBU1} to GND, V_{SBU2} to GND, V_{GSBU1} to GND, V_{GSBU1} to GND	−0.5	20	V
V_{VSBU_H}	V_{SBU1_H} to GND, V_{SBU2_H} to GND	−0.5	6.5	V
$V_{I/O}$	SENSE, MIC, DET, INT, to GND	−0.5	6.5	V
V_{CNTRL}	Control Input Voltage			

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
POWER					
V_{CC}	Supply Voltage	2.7	−	5.5	V
USB SWITCH					
V_{SW_USB}	V_{DP} to GND, V_{DN} to GND, V_{DP_R} to GND, V_{DN_L} to GND	0	−	3.6	V
AUDIO SWITCH					
V_{SW_Audio}	V_{DP_R} to GND, V_{DN_L} to GND, V_L to GND, V_R to GND	−3.6	−	3.6	V
MIC SWITCH					
V_{VSBU_MIC}	V_{SBU1} to GND, V_{SBU2} to GND, V_{MIC} to GND	0	−	3.6	V
SENSE SWITCH					
V_{VGSBU_SEN}	V_{GSBU1} to GND, V_{GSBU2} to GND, V_{SENSE} to GND	0	−	3.6	V
SBU TO SBUX_H SWITCH					
V_{VGSBU}					

Table 4. DC ELECTRICAL CHARACTERISTICS
(V_{CC}

Table 4. DC ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40 C to 85 C, and T_A (Typ.) = 25 C, unless otherwise specified.)

Symbol	Parameter	Condition	Power	Min.	Typ.	Max.	Unit
SENSE SWITCH							
V_{OV_TRIP}	Input OVP Lockout on GSBUx	Rising edge	V_{CC}: 2.7 V to 5.5 V	4.5	5	5.3	V
V_{OV_HYS}	Input OVP Hysteresis of GSBUx			–	0.3	–	V
SBUX PINS							
I_{OZ}	Off Leakage Current of SBUx	SBUx = 0 V to 3.6 V	V_{CC}: 2.7 V to 5.5 V	−3.0	–	3.0	μA
I_{OFF}	Power−Off Leakage Current Port SBUx	SBUx = 0 V to 3.6 V	Power off	−3.0	–	3.0	μA
V_{OV_TRIP}	Input OVP Lockout	Rising edge	V_{CC}: 2.7 V to 5.5 V	4.5	5	5.3	V
V_{OV_HYS}	Input OVP Hysteresis			–	0.3	–	V
MIC SWITCH							
I_{ON}	On Leakage Current of MIC Switch	SBUx = 0 V to 3.6 V, MIC is floating	V_{CC}: 2.7 V to 5.5 V	−3.0	–	3.0	μA
I_{OZ}	Off Leakage Current of MIC	MIC = 0 V to 3.6 V		−1.0	–	1.0	μA
I_{OFF}	Power Off Leakage Current of MIC	MIC = 0 V to 3.6 V	Power off	−1.0	–	1.0	μA
R_{ON_MIC}	MIC Switch On Resistance	Isw = 30 mA, V_{SW} = 3.6 V	V_{CC}: 2.7 V to 5.5 V	1.7	3.0	3.9	Ω
SBUX_H SWITCH							
I_{ON}	On Leakage Current of SBUx_H Switch	SBUx = 0 V to 3.6 V, SBUx_H is floating	V_{CC}: 2.7 V to 5.5 V	−3.0	–	3.0	μA
I_{OZ}	Off Leakage of SBUx_H	SBUx_H =0 V to 3.6 V		−1	–	1	μA
I_{OFF}	Power Off Leakage Current of SBUx_H	SBUx_H = 0 V to 3.6 V	Power off	−1.0	–	1.0	μA
R_{ON_SBU}	SBUx_H Switch On Resistance	Isw = 30 mA, V_{SW} = 0 V to 3.6 V	V_{CC}: 2.7 V to 5.5 V	1.5	3.0	3.5	Ω

Table 4. DC ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40 C to 85 C, and T_A (Typ.) = 25

Table 5. AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40 C to 85 C, and T_A (Typ.) = 25 C, unless otherwise specified.)

Symbol	Parameter	Condition	Power	Min.	Typ.	Max.	Unit
AUDIO SWITCH							
t_{delay}	Audio Switch Turn On Delay Time	DP_R = DN_L = 1 V, R_L = 32 Ω	V_{CC} = 3.3 V	−	65	−	μs
t_{rise}	Audio Switch Turn On Rising Time (Note 1)	DP_R = DN_L = 1 V, R_L = 32 Ω		−	240	−	μs
t_{OFF}	Audio Switch Turn Off Time	DP_R = DN_L = 1 V, R_L = 32 Ω		−	15	−	μs
X_{TALK}	Cross Talk (Adjacent)	f = 1 kHz, R_L = 50 Ω, V_{SW} = 1 V_{RMS}		−	−100	−	dB
BW							

Table 5. AC ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 2.7 V to 5.5 V, V_{CC}

Table 6. I²C SPECIFICATION

(V_{CC} = 2.7 V to 5.5, V_{CC} (Typ.) = 3.3 V ,T_A = −40 C to 85 C. T_A (Typ.) = 25 C, unless otherwise specified)

Symbol	Parameter	Fast Mode		
		Min.	Max.	Unit
f_{SCL}	I²C_SCL Clock Frequency		400	kHz
$t_{HD;\ STA}$	Hold Time (Repeated) START Condition	0.6		μs
t_{LOW}	Low Period of I²C_SCL Clock	1.3		μs
t_{HIGH}	High Period of I²C_SCL Clock	0.6		μs
$t_{SU;\ STA}$	Set−up Time for Repeated START Condition	0.6		μs
$t_{HD;\ DAT}$	Data Hold Time (Note 2)	0	0.9	μs
$t_{SU;\ DAT}$	Data Set−up Time (Note 3)	100		ns
t_r	Rise Time of I²C_SDA and I²C_SCL Signals (Note 3)	20 + 0.1C_b	300	ns
t_f	Fall Time of I²C_SDA and I²C_SCL Signals (Note 3)	20 + 0.1C_b	300	ns
$t_{SU;\ STO}$	Set−up Time for STOP Condition	0.6		μs
t_{BUF}	Bus−Free Time between STOP and START Conditions	1.3		μs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

2. Guaranteed by design, not production tested.
3. A fast−mode I²C−bus device can be used in a standard−mode I²C−bus system, but the requirement $t_{SU;DAT}$ 250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If such a device does stretch the LOW period of the I²C_SCL signal, it must output the next data bit to the I²C_SDA line t_{r_max} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard−mode I²C bus specification) before the I²C_SCL line is released.

Figure 3. Definition of Timing for Full−Speed Mode Devices on the I²C Bus

C to 85 C, and T_A (Typ.) = 25 C)

Condition	Power	T_A =− 40 C to +85 C			Unit
		Min.	Typ.	Max.	
f = MHz, 100 mV$_{PK-PK}$, 100 mV DC bias	VCC = 3.3 V		9		pF
f = 1 MHz, 100 mV$_{PK-PK}$, 100 mV DC bias			7.5		pF
f = 1 MHz, 100 mV$_{PK-PK}$, 100 mV DC bias			3		pF
f = 1 MHz, 100 mV$_{PK-PK}$, 100 mV DC bias			55		pF
f = 1 MHz, 100 mV$_{PK-PK}$, 100 mV DC bias			88		pF
f = 1 MHz, 100 mV$_{PK-PK}$, DC bias,					

DEVICE ID
Address: 00h
Reset Value: 8’b 0000_1001
Type: Read

Bits	Name	Size	Description
7:6	Vendor ID	2	Vendor ID

OVP STATUS

Address: 03h
Reset Value: 8'b 0000_0000
Type: Read

Bits	Name	Size	Description
[7:6]	Reserved	2	Do Not Use
5	OVP on DP_R PIN	1	0: OVP event has not occurred 1: OVP event has occurred
4	OVP on DN_L PIN	1	0: OVP event has not occurred 1: OVP event has occurred
3	OVP on SBU1 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
2	OVP on SBU2 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
1	OVP on GSBU1 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
0	OVP on GSBU2 PIN	1	0: OVP event has not occurred 1: OVP event has occurred

SWITCHING SETTING ENABLE

Address: 04h
Reset Value: 8'b 1001_1000
Type: Read/Write

Bits	Name	Size	Description
7	Device Enable	1	0: Device Disable; L, R pull down by 10 k and other switch nodes will be high−Z for positive input. 1: Device Enable. Device Enable = 1 Device enable = 0 ENN = 1 Device Disable Device Disable ENN = 0 Device Enable Device Disable
6	SBU1_H to SBUx switches	1	0: Switch Disable; SBU1_H will be high−Z for positive input 1: Switch Enable
5	SBU2_H to SBUx switches	1	0: Switch Disable; SBU2_H will be high−Z for positive input 1: Switch Enable
4	DN_L to DN or L switches	1	0: Switch Disable; DN_L,DN will be high−Z for positive input. L pull down by 10 kohm 1: Switch Enable
3	DP_R to DP or R switches	1	0: Switch Disable; DP_R,DP will be high−Z for positive input. R pull down by 10 kohm 1: Switch Enable
2	Sense to GSBUx switches	1	0: Switch Disable; Sense,GSBU1 and GSBU2 will be high−Z for positive input 1: Switch Enable
1	MIC to SBUx switches	1	0: Switch Disable: MIC will be high−Z for positive input. 1: Switch Enable
0	AGND to SBUx switches	1	0: Switch Disable: AGND will be high−Z for positive input. 1: Switch Enable

SWITCH SELECT
Address: 05h
Reset Value: 8'b 0001_1000
Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do Not Use
6	SBU1_H switches	1	0: SBU1_H to SBU1 switch ON 1: SBU1_H to SBU2 switch ON
5	SBU2_H switches	1	0: SBU2_H to SBU2 switch ON 1: SBU2_H to SBU1 switch ON
4	DN_L to DN or L switches	1	0: DN_L to L switch ON 1: DN_L to DN switch ON
3	DP_R to DP or R switches	1	0: DP_R to R switch ON 1: DP_R to DP switch ON
2	Sense to GSBUx switches	1	0: Sense to GSBU1 switch ON 1: Sense to GSBU2 switch ON
1	MIC to SBUx switches	1	0: MIC to SBU2 switch ON 1: MIC to SBU1 switch ON
0	AGND to SBUx switches	1	0: AGND to SBU1 switch ON 1: AGND to SBU2 switch ON

SWITCH STATUS0
Address: 06h
Reset Value: 8'b 0000_0000
Type: Read Only

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:2]	Sense Switch Status	2	00: Sense switch is Open/Not Connected 01: Sense connected to GSBU1 10: Sense connected to GSBU2 11: Not Valid
[3:2]	DP_RSwitch Status	2	00: DP_R Switch Open/Not Connected 01: DP_Rconnected to DP 10: DP_Rconnected to R 11: Not Valid
[1:0]	DN_L switch Status	2	00: DN_L Switch Open/Not Connected 01: DN_L connected to DN 10: DN_L connected to L 11: Not Valid

SENSE SWITCH SLOW TURN−ON
Address: 0Bh
Reset Value: 8’b 0000_0001
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25600 μS 00000001: 200 μS

TIMING DELAY BETWEEN SENSE SWITCH ENABLE AND L SWITCH ENABLE

Address: 0Fh
Reset Value: 8’b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting		

FUNCTION ENABLE

Address: 12h
Reset Value: 8'b 0000_1000
Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do not use
6	DET I/O Control	1	1: DET pin is in Open/Drain Configuration 0: DET pin is in Push/Pull Configuration
5	RES detection range setting	1	1: 10k to 2560 k 0: 1k to 256 k
4	GPIO control enable	1	1: enable 0: disable
3	Slow turn on control enable	1	1: enable 0: disable
2	MIC auto break out control enable	1	1: enable 0: disable
1	RES detection enable	1	1: enable; will be changed to '0' after low resistance detection 0: disable
0	Audio jack detection and configuration enable	1	1: enable; will be changed to '0' after audio jack detection and configuration 0: disable

When GPIO control mode (manual switch control) is enable. '**Switch control'** register is changed to read only. It will reflect switch status. I^2C slave address is

RES DETECTION PIN SETTING

Address: 13h
Reset Value: 8'b 0000_0000
Type: Read

Bits	Name	Size	Description
[7:3]	Reserved	5	Do not use
[2:0]	Pin selection	3	000: CC_IN 001: DP/R 010: DN_L 011: SBU1 100: SBU2 101: Do not use 111: Do not use

If RES detection pin is enable before setting PIN selection it will always do the CC_IN first. Recommend user to select the pin first before setting the RES detection pin enable.

RES VALUE

Address: 14h
Reset Value: 8'b 1111_1111
Type: Read

Bits	Name	Size	Description
[7:0]	Detected resistance value	8	0000_0000 : R < 1 k 1111_1111: R > 300 K

RES DETECTION THRESHOLD

Address: 15h
Reset Value: 8'b 0001_0110
Type: Read

Bits	Name	Size	Description
[7:0]	RES detection threshold	8	Selection by 1 KΩ per step if Reg 12h [5] = 0 Selection by 10 KΩ per step if Reg 12h [5] = 0 Default Value = 22 KΩ 0000_0000: 1 KΩ /10 KΩ 1111_1111: 256 KΩ / 2560 KΩ

RES DETECTION INTERVAL

Address: 16h
Reset Value: 8'b 0000_0000
Type: Read

Bits	Name	Size	Description
[7:2]	Reserved	6	Do not use
[1:0]	RES detection interval	2	00: Single 01: 100 mS 10: 1 S 11: 10 S

AUDIO JACK STATUS

Address: 17h
Reset Value: 8'b 0000_0001
Type: Read

Bits	Name	Size	Description
[7:3]	Reserved	4	Do not use
3	4pole	1	1: 4 Pole SBU2 to MIC, SBU1 to audio ground 0: others
2	4pole		

RES /AUDIO JACK DETECTION INTERRUPT MASK

Address: 19h
Reset Value: 8'b 0000_0000
Type: Read Clear

Bits	Name	Size	Description
[7:3]	Reserved	5	Do Not Use
2	Audio jack detection and configuration	1	1: Mask Audio jack detection and configuration has occurred interrupt
1	Low resistance occurred	1	1: Low resistance has occurred interrupt
0	Low resistance detection	1	1: Low resistance detection has occurred interrupt

AUDIO JACK DETECTION REG1 VALUE

Address: 1Ah
Reset Value: 8'b 1111_1111
Type: Read

Bits	Name	Size	Description
[7:0]	Audio jack detection value	8	Resistance between SBU1 to SBU2

AUDIO JACK DETECTION REG2 VALUE

Address: 1Bh
Reset Value: 8'b 1111_1111
Type: Read

Bits	Name	Size	Description
[7:0]	Audio jack detection value	8	Resistance between SBU2 to SBU1

MIC DETECTION THRESHOLD DATA0

Address: 1Ch
Reset Value: 8'b 0010_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA0	8	MIC detection threshold DATA0 0010_0000: 300 mV

MIC DETECTION THRESHOLD DATA1

Address: 1Dh
Reset Value: 8'b 1111_1111
Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA1	8	MIC detection threshold DATA1 1111_1111: 2.4 V

I2C RESET

Address: 1Eh
Reset Value: 8'b 0000_0000
Type: W/C

Bits	Name	Size	Description
[7:1]	Reserved	7	Reserved
0	I2C reset	1	0: default 1: I^2C reset

CURRENT SOURCE SETTING
Address: 1Fh
Reset Value: 8’b 0000_0111
Type: Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Reserved
[3:0]	Current Source Setting	4	1111: 1500 μA 0111: 700 μA 0001: 100 μA 0000: invalid

APPLICATION INFORMATION

Over−Voltage Protection

FSA4480 features over−voltage protection (OVP) on receptacle side pins that switches off the internal signal routing path if the input voltage exceeds the OVP threshold.

If OVP is occurred, interrupt signal can be send by INT signal and FLAG data will provide information that which pin had OVP event.

Headset Detection

FSA4480 integrates headset unplug detection function by detecting the CC_IN voltage. The function is always active when device is enabling. DET will be high when CC_IN is low (CC_IN < 1.2 V). When CC_IN = High (CC_IN > 1.5 V), DET will be released to low.

	Device Disable	Device Enable
CC_IN < V_{TH_L} = 1.2 V	DET = 0	DET = 1
CC_IN > V_{TH_H} = 1.5 V	DET = 0	DET = 0

MIC Switch Auto−off Function

The function is active during control bit 0x12h bit[2] = 1. When CC_IN is high (CC_IN > 1.5 V) and L,R, Audio ground switches are under on status, MIC switch will be off and receptacle side pin will be connected to ground for 50 μS first. Then it shows high−Z status under MIC switch is set on status.

Audio Ground Detection and Configuration

The function is active when control bit 0x12h bit[0] = 1 and R, L AGND switches are set to be on status. For type−C interface analog headset, the audio ground could be SBU1 pin or SBU2 pin. The function will provide autonomous detection and configuration to route MIC and audio ground signal accordingly.

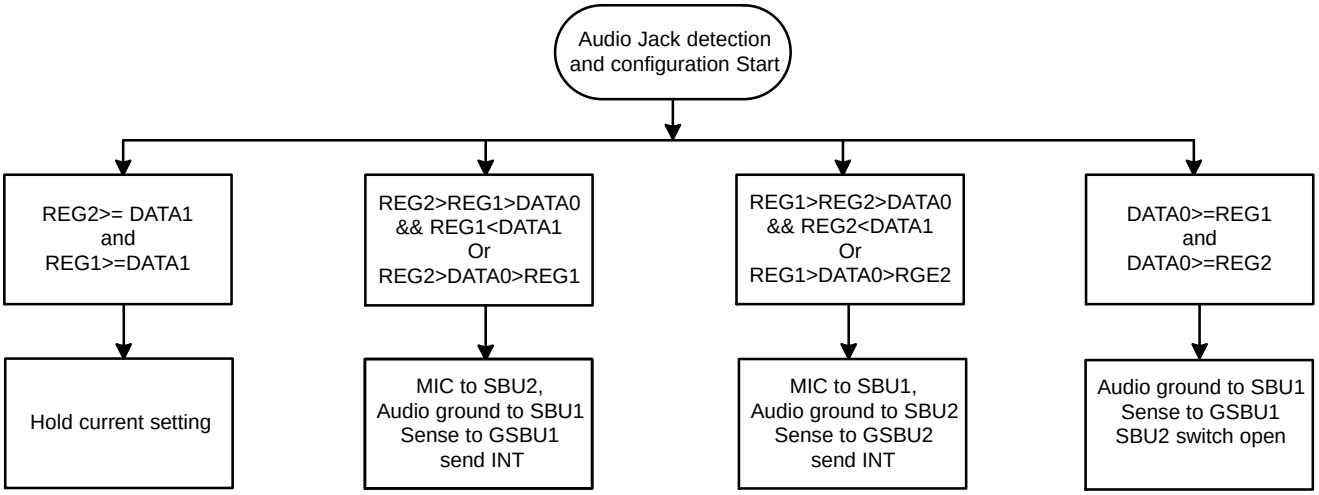


Figure 4.

During detection and configuration, the R, L, Sense, MIC and Audio ground switch will be off. After detection and configuration, R and L switches will turn on according to switch configuration and timing setting. MIC, Sense and Audio ground will turn on according to detection results and timing control setting.

Resistance Detection

The function is active during control bit 0x12h bit[1] = 1. It will monitor the resistance between receptacle side pins and ground. During resistance detection, the switch which is monitored will be off. The detection result will be saved in the resistance flag register. The measurement could be from 1 kΩ to 2.56 MΩ which is controlled by internal register. The detection interval can be set at 100 ms, 1 s or 10 s by register 0x16h.

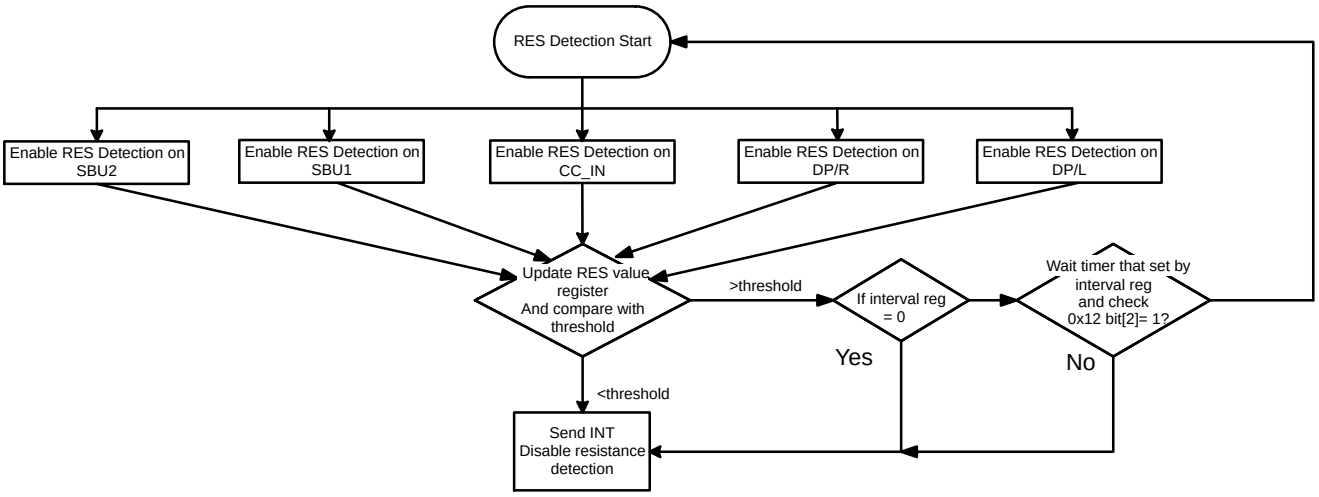


Figure 5.

Manual Switch Control

The function is active during control bit 0x12h bit[4] = 1 and 0x04h = FF. It will provide manual control for device. During this configuration, ADDR and INT pins will be set as logic control input.

MANUAL SWITCH CONTROL

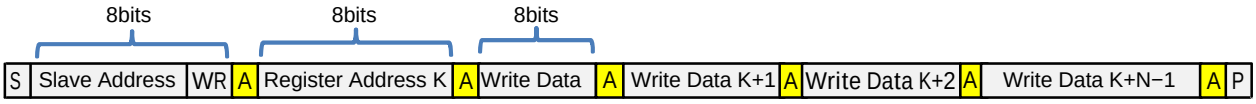
(The function is active during control bit 0x12h bit[4] = 1 and 0x04h = FF. It will provide manual control for device. During this configuration, ADDR and INT pins will be set as logic control input.)

Power	ENN	ADDR	INT	SENSE Switch	Headset Detection	USB Switch	Audio Switch	MIC/ Audio GND Switch	SBU by Pass Switch
OFF	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	H	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	L	0	0	OFF	OFF	ON: DP_R to DP DN_L to DN	OFF	OFF	ON: SBU1 to SBU1_H SBU2 to SBU2_H
ON	L	0	1	OFF	OFF	ON: DP_R to DP DN_L to DN	OFF	OFF	ON: SBU1 to SBU2_H SBU2 to SBU1_H

I²C INTERFACE

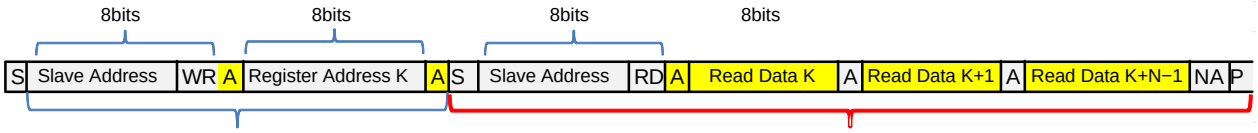
The FSA4480 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 2.1 requirements. This block is designed for fast mode, 400 kHz, signals.

Examples of an I²C write and read sequence are shown in below figures respectively.



NOTE: Single Byte read is initiated by Master with P immediately following first data byte.

Figure 6. I²C Write Example



NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed

Figure 7. I²C Read Example

TEST DIAGRAMS

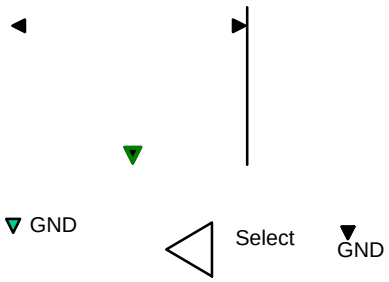
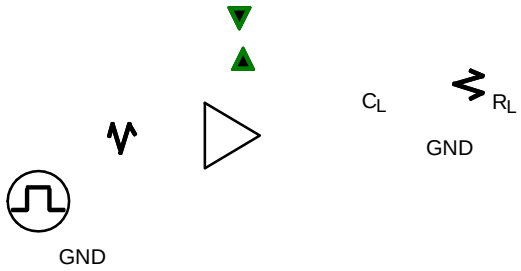
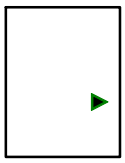


Figure 8. On Resistance





V_{OUT}

Figure 14. Bandwidth

Figure 15. Channel Off Isolation

Figure 16. Adjacent Channel Crosstalk

Figure 17. Channel Off Capacitance

Figure 18. Channel On Capacitance

Figure 19. Total Harmonic Distortion (THD + N)

WLCSP25 2.24x2.28x0.586
CASE 567UZ
ISSUE B

DATE 03 JAN 2018

PER

ASM