USB Type-C Analog Audio Switch with Protection Function

FSA4486

Description

FSA4486 is a high−performance USB Type−C port multimedia switch which supports analog audio headsets. FSA4486 allows the sharing of a common USB Type−C port to pass USB2.0 signal, analog

Figure 1. Application Block Diagram

PIN CONFIGURATION

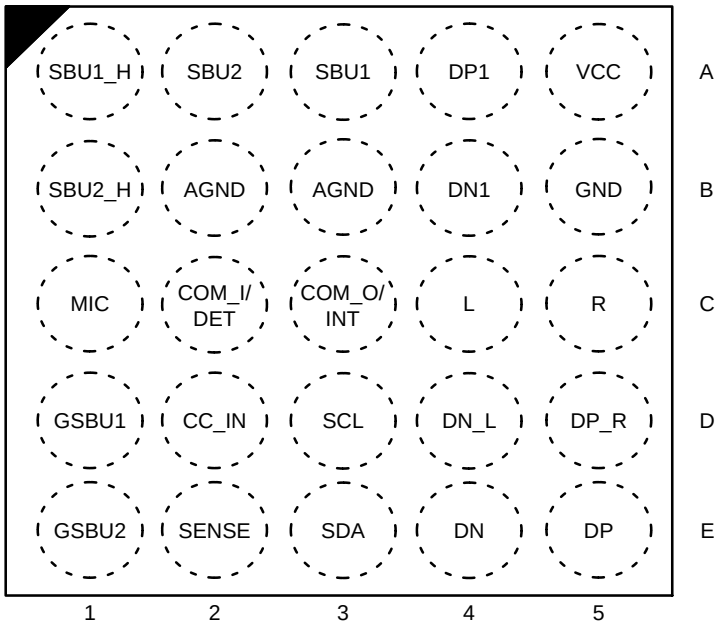

Figure 2. Pin Assignment (Top Through View)

Table 1. PIN DESCRIPTIONS

Name	Ball	Name	Description
1	A5	VCC	Power Supply (2.7 to 5.5 V) chip will be enabled after VCC is valid
2	B5	GND	Chip ground
3	D5	DP/R	USB/Audio Common Connector
4	D4	DN/L	USB/Audio Common Connector
5	E5	DP	

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage from VCC	−0.5	6.5	V
V_{CC_IN}	$V_{CC\_IN,}$ to GND	−0.5	20	V
V_{SW_USB}	USB Switch Voltage, (DP_R, DN_L) to GND	−3.6	20	V
V_{SW_SBU}	SBU Switch Voltage, (SBUx, GSBUx) to GND	−0.5	20	V
V_{SW_HOST}	Host Side Switch Voltage, (DP, DN, S1H, S2H, SENSE, MIC) to GND	−0.5	6.5	V
V_{SW_DP1DN1}	Host Side Switch Voltage, (DP1, DN1) to GND	−3.6	6.5	V
V_{SW_Audio}	Host Side Switch Voltage, (L, R) to GND	−3.6	6.5	V
V_{CNTRL}	Control Pin Input Voltage, (SDA, SCL, COMPI/DET, COMPO/INT) to GND	−0.5	6.5	V
I_{IK}	DC Input Diode Current	−50	−	mA
I_{SW_USB}				

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Max	Unit
POWER					
V_{CC}	Supply Voltage	2.7	−	5.5	V
USB SWITCH					
V_{SW_USB}	USB Switch Voltage, (DP_R, DN_L, DP, DN, DP1, DN1) to GND	0	−	3.6	V
AUDIO SWITCH					
V_{SW_Audio}	Audio Switch Voltage, (DP_R, DN_L, L, R) to GND	−3			

Table 4. DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
I_{CC}	Supply Current	USB switches on, SBUx to SBUx_H switches on	VCC: 2.7 V to 5.5 V	−	−	65	μA
I_{CC_AUDIO}	Audio Supply Current	Audio switches on, MIC switch on and Audio GND switch on		−	−	65	μA
ICCZ	Quiescent Current, Software Disabled	ENN = L, 04H'b7 = 0		−	−	5	μA
USB/AUDIO/MCU COMMON PINS: DP/R, DN_L							
IOZ	USB Connector Side Off Leakage Current	DP_R, DN_L = 0 V to 3.6 V	VCC: 2.7 V to 5.5 V	−3	−	3	μA
IOFF	USB Connector Side Power Off Leakage Current	DP_R, DN_L = 0 V to 3.6 V, VCC = 0 V	Power off	−3	−	3	μA
VOV_TRIP	Input OVP Lockout	Rising Edge of DP_R, DN_L	VCC: 2.7 V to 5.5 V	4.5	5	5.3	V
VOV_HYS	Input OVP Hysteresis			−	0.3	−	V
USB SWITCH							
ION_USB	USB Switch ON Leakage Current	DN_L, DP_R = 0 V to 3.6 V, DP, DN, R, L, DP1, DN1 = Float	VCC: 2.7 V to 5.5 V	−3	−	3	μA
IOZ_USB	USB Host Side Off Leakage Current	DN, DP = 0 V to 3.6 V		−3	−	3	μA
IOFF_USB	USB Host Side Power Off Leakage Current	DN, DP = 0 V to 3.6 V, VCC = 0 V	Power off	−3	−	3	μA
RON_USB	USB Switch On Resistance	ISW = 8 mA, VSW = 0.4 V	VCC: 2.7 V to 5.5 V	−	3	5.2	Ω
DP1 DN1 SWITCH							
ION_DN1DP1	DN1DP1 Switch ON Leakage Current	DN_L, DP_R = 0 V to 3.6 V, DP,					

Table 4. DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
SBU DATA SWITCH							

P Tk.0146 Tc(022 .9071 refiT)79 125.461C81 0 TD845 62.192 .9071 1.77j89.754 695.055 62.19427.074 709.455 26.02

Table 4. DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
COMP_I/DET PIN							
V_COMP/I_Trip	High Voltage Input		VCC: 2.7 V to 5.5 V	−	0.27	−	V
V_COMP/I_HYS	Input hysteresis voltage			−	30	−	mV
VOL_DET	Output Low Voltage	IOUT = 2 mA		−	−	0.275	V
IIN	Input Current			−3	−	3	μ

Table 5. AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
DP1DN1 SWITCH							
tON_DP1DN1	DP1DN1 Switch Turn−on Time	DP_R = DN_L = 1.5 V, RL = 50 Ω	VCC = 3.3 V	−	70	−	μs
tOFF_DP1DN1	DP1DN1 Switch Turn−off Time	DP_R = DN_L = 1.5 V, RL = 50 Ω		−	25	−	μs
BW_DP1DN1	−3 dB Differential Bandwidth	RL = 50 Ω		−	100	−	MHz
OIRR_DP1DN1	Off Isolation between DP1, DN1 and Common Node Pins	f = 1 kHz, RL = 50 Ω, CL = 0 pF, VSW = 1 VRMS, all of switches need to be opened		−	−100	−	dB
MIC/AUDIO GROUND SWITCH							
tON_MIC	MIC Switch Turn On Delay Time with Slow Turn On	SBUx = 1 V, RL = 50 Ω, MIC_SLOW = 00000000b	VCC = 3.3 V	−	250	−	μs
tOFF_MIC	MIC Switch Turn Off Time	SBUx = 2.5 V → GND, MIC = 50 Ω to GND		−	25	−	μs
tON_AGND	AGND Switch Turn On Time	SBUx pulled up to 0.5 V by 16 Ω, AGND connect to GND		−	250	−	μs
tOFF_AGND	AGND Switch Turn Off Time	SBUx = 0.5 V by 16 Ω		−	25	−	μs
BW	MIC Switch Bandwidth	RL = 50 Ω		−	50	−	MHz
PSRR_MIC	Power Supply Rejection Ratio to MIC	Supply Noise = 300 mVpp, f = 1 kHz, RL = 2000 Ω		−	−100	−	dB
SBU SWITCH							
tON_SBU	SBUx_H Switch Turn On Time	SBUx = 2.5 V, RL = 50 Ω	VCC = 3.3 V	−	100	−	μs
tOFF_SBU	SBUx_H Switch Turn Off Time	SBUx = 2.5 V, RL = 50 Ω		−	25	−	μs
BW_SBU	Bandwidth	RL = 50 Ω		−	50	−	MHz
tOVP_SBU	SBUx Pins OVP Response Time	Rload = 50 Ω, Vsw = 4 V to 6 V		−	0.5	1	μs
SENSE SWITCH							
tON_SENSE	Turn−On Time	GSBUx = 0 V to 1 V, SENSE = 50 Ω to GND	VCC = 3.3 V	−	400	−à"—^äis# }uîFœ ïå'¿1ø …5	
tOFF_SENSE	Sense Switch Turn Off Time						

Table 6. I²C SPECIFICATION (V_{CC} = 2.7 V to 5.5, V_{CC} (Typ.) = 3.3 V ,T_A = −40°C to 85°C. T_A (Typ.) = 25°C, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	I2C_SCL Clock Frequency	−	400	−	kHz
tHD; STA	Hold Time (Repeated) START Condition	0.6	−	−	μs
tLOW	Low Period of I2C_SCL Clock	1.3	−	−	μs
tHIGH	High Period of I2C_SCL Clock	0.6	−	−	μs
tSU; STA	Set−up Time for Repeated START Condition	0.6	−	−	μs
tHD; DAT	Data Hold Time (Note 2)	0	−	0.9	μs
tSU; DAT	Data Set−up Time	100	−	−	ns
tr	Rise Time of I2C_SDA and I2C_SCL Signals (Note 3)	20 + 0.1Cb	−	300	ns

Table 8. REGISTER MAPS

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	Device ID	R	0x08	0	0	0	0	1	0	0	1
01H	OVP Interrupt Mask	R/W	0x00	Mask OCP_AGND	Mask OVP interrupt	Mask OVP/ DP_R	Mask OVP/ DN_L	Mask OVP/ SBU1	Mask OVP/ SBU2	Mask OVP/ GSBU1	Mask OVP/ GSBU2
02H	OVP Interrupt Flag	R/C	0x00	OCP_AGND	OVP_ALL	DP_R	DN_L	SBU1	SBU2	GSBU1	GSBU2
03H	OVP Status	R	0x00	Reserved	OCP_STAT_ AGND	OVP/ DP_R	OVP/ DN_L				

OVP /OCP INTERRUPT MASK

Address: 01h
Reset Value: 8'b 0000_0000
Type: Read/Write

Bit	Name	Default	Description
7	M_OCP_AGND	0	0b: Do not mask OCP interrupt 1b: Mask OCP interrupt on SBUx to AGND
6	OVP Interrupt mask control	0	OVP Interrupt function Enable/Disable 0: Controlled by [5:0] bit 1: Mask all connector side pins OVP interrupt
5	DP_R OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt
4	DN_L OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt
3	SBU1 OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt
2	SBU2 OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt
1	GSBU1 OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt
0	GSBU2 OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt

OVP/OCP INTERRUPT FLAG

Address: 02h
Reset Value: 8'b 0000_0000
Type: Read Clear

Bit	Name	Default	Description
7	I_OCP_AGND	0	0: OCP has not occured 1: OCP event has occured on SBUx to AGND
6	I_OVP_ALL	0	0: OVP or OCP event has not occurred 1: OVP or OCP event has occurred
5	DP_R OVP	0	0: OVP event has not occurred 1: OVP event has occurred
4	DN_L OVP	0	0: OVP event has not occurred 1: OVP event has occurred
3	SBU1 OVP		

OVP/OCP STATUS

Address: 03h
Reset Value: 8'b 0000_0000
Type: Read

Bit	Name	Default	Description
7	Reserved	0	Do Not Use
6	OCP_STAT_AGND	0	0: OCP event has not occurred 1: OCP event has occurred on SBUx to AGND
5	OVP on DP_R PIN	0	0: OVP event has not occurred 1: OVP event has occurred
4	OVP on DN_L PIN	0	0: OVP event has not occurred 1: OVP event has occurred
3	OVP on SBU1 PIN	0	0: OVP event has not occurred 1: OVP event has occurred
2	OVP on SBU2 PIN	0	0: OVP event has not occurred 1: OVP event has occurred
1	OVP on GSBU1 PIN	0	0: OVP event has not occurred 1: OVP event has occurred
0	OVP on GSBU2 PIN	0	0: OVP event has not occurred 1: OVP event has occurred

SWITCHING SETTING ENABLE

Address: 04h
Reset Value: 8'b 1111_1000
Type: Read/Write

Bit	Name	Default	Description
7	Device Enable	1	0: Device Disable; All switch nodes will be high−Z. 1: Device Enable.
6	SBU1_H to SBUx switches	1	0: Switch Disable; SBU1_H will be high−Z. 1: Switch Enable Internal Notes: Priority: SBU > AGND > MIC
5	SBU2_H to SBUx switches	1	0: Switch Disable; SBU2_H will be high−Z. 1: Switch Enable Internal Notes: Priority: SBU > AGND > MIC
4	DN/L to DN/L/DN1 switches	1	0: Switch Disable; DN/L, DN/L/DN1 will be high−Z 1: Switch Enable
3	DP/R to DP/R/DP1 switches	1	0: Switch Disable; DP/R, DP/R/DP1 will be high−Z 1: Switch Enable
2	Sense to GSBUx switches	0	0: Switch Disable; Sense, GSBU1 and GSBU2 will be high−Z 1: Switch Enable
1	MIC to SBUx switches	0	0: Switch Disable: MIC will be high−Z. 1: Switch Enable Internal Notes: Priority: SBU > AGND > MIC
0	AGND to SBUx switches	0	0: Switch Disable: AGND will be high−Z. 1: Switch Enable Internal Notes: Priority: SBU > AGND > MIC

SWITCH SELECT
Address: 05h
Reset Value: 8’b 0000_1000
Type: Read/Write

Bit	Name	Default	Description
7	Reserve	0	

SWITCH STATUS2
Address: 07h
Reset Value: 8'b 0010_0011
Type: Read Only

Bit	Name	Default	Description
7:6	Reserved	00	Do Not Use
5:3	SBU2_STAT	100	000b: SBU2 switch is OPEN 001b: SBU2 switch is CLOSED to MIC 010b: SBU2 Switch is CLOSED to AGND 011b: SBU2 Switch is CLOSED to S1H 100b: SBU2 Switch is CLOSED to S2H 101b: SBU2 Switch is CLOSED to both S1H and S2H 110b: Not Valid 111b: Not Valid
2:0	SBU1	011	000b: SBU1 switch is OPEN 001b: SBU1 switch is CLOSED to MIC 010b: SBU1 Switch is CLOSED to AGND 011b: SBU1 Switch is CLOSED to S1H 100b: SBU1 Switch is CLOSED to S2H 101b: SBU1 Switch is CLOSED to both S1H and S2H 110b: Not Valid 111b: Not Valid

CURR_SOURCE_STATUS
Address: 08h
Reset Value: 8'b 0000_0010
Type: Read

Bit	Name	Default	Description
7:2	Reserved	000000	Do Not Use
1:0	CURR_SOURCE_STAT	10	00b: 20 μA 01b: 100 μA 10b: 700 μA (DEFAULT) 11b: 1500 μA

PROTECTION EN
Address: 09h
Reset Value: 8'b 0000_0001
Type: Read/Write

Bit	Name	Default	Description
7:3	Reserve	00000	Reset condition: 00000 Not Use
2	MODE_SEL	0	Reset condition: 0 0: COMP_I/DET will works as COMP_I; COMP_O/INT will work as COMP_O 1: COMP_I/DET will works as DET; COMP_O/INT will work as INT CC_IN will behaves as descripted in "Device attached and detach detection" accordingly
1	EN_OVP	1	0b: Over Voltage Protection is Disabled 1b: Over Voltage Protection is Enabled (DEFAULT)
0	EN_OCP	1	0b: Over Current Protection is Disabled 1b: Over Current Protection is Enabled (DEFAULT)

OVP OCP PROTECTION STATUS

Address: 0Bh

Reset Value: 8’b 0010_1100

Type: Read/Write

Bit	Name	Default

SENSE2L_EN_DELAY

Address: 0Fh
Reset Value: 8'b 0000_0000
Type: Read/Write

Bit	Name	Default	Description
7:0	SENSE2L_EN_DELAY	0000000	00000000b: = 0 μs (DEFAULT) 00000001b: = 100 μs ..... 11111111b: = 25500 μs Increment size is 100 μs per bit

AGND2L_EN_DELAY

Address: 10h
Reset Value: 8'b 0000_0000
Type: Read/Write

Bit	Name	Default	Description
7:0	AGND2L_EN_DELAY	0000000	00000000b: = 0 μs (DEFAULT) 00000001b: = 100 μs ..... 11111111b: = 25500 μs Increment size is 100 μs per bit

AUDIO ACCESSORY STATUS

Address: 11h
Reset Value: 8'b 0000_0001
Type: Read

Bit	Name	Default	Description
7:2	Reserved	000000	Reserved
1	CC_IN_STAT	0	0b: CC_IN = Low 1b: CC_IN = High
0	DET_STAT	1	0b: DET output is LOW 1b: DET output is High−Z

FUNCTION ENABLE

RES DETECTION THRESHOLD

Address: 15h
Reset Value: 8'b 0001_0110
Type: Read

Bit	Name	Default	Description
7:0	RES_DET_THRESH	00010110	Selection by 1 kΩ per step if Reg 12h [5] = 0 Selection by 10 kΩ per step if Reg 12h [5] = 1 Default Value = 22 kΩ 0000_0000: 1 kΩ / 10 kΩ ..... 1111_1111: 256 kΩ / 2560 kΩ

AUTO REST & DET_INTV

Address: 16h
Reset Value: 8'b 0000_1100
Type: Read/ Write

Bit	Name	Default	Description
7:5	Reserved	000	Do Not Use
4	TIMER_RESET	0	1: Reset the Timer for auto reset function, and it will be changed back to "0" automatically once timer was rested 0: Not reset the timer for auto reset function

RES DETECTION /AUDIO JACK DETECTION INTERRUPT FLAG

Address: 18h
Reset Value: 8'b 0000_0000
Type: Read Clear

Bit	Name	Default	Description
7:5	Reserved	000	Do Not Use
4	I_CC/IN_CHG	0	0b: CC_IN change has not been detected 1b: CC_IN change has been detected
3	I_DET_FUNCT	0	Audio Accessory Detach has occurred 0b: DET_FUNCT = 00b, 01b, 11b, or DET_FUNCT = 10b and DET_STAT = 1b 1b: DET_FUNCT = 10b and DET_STAT = 0b Clearing I DET FUNCT will return the DET output to High−Z
2	I_AUDIO_JACK_DET	0	0b: Audio Jack Detection and Configuration has not occurred 1b: Audio Jack Detection and Configuration has occurred
1	I_LOW_RES	0	0b: A Resistance < RES_DET_THRESH has not been detected 1b: A Resistance < RES_DET_THRESH has been detected
0	I_RES_DET_COMP	0	0b: Resistance Detection has not been completed 1b: Resistance Detection has been completed

AUDIO JACK DETECTION REG2 VALUE

Address: 1Bh
Reset Value: 8’b 1111_1111
Type: Read

Bit	NameName

Auto Reset Function

The function will be active during control bit 0x12h bit[3] = 1.When the bit[4] of register DET_INTV not being written before timer (can be set through bit[2][3]) out, FSA4486 will be reset automatically, and all of channel restore to default state including USB switch will be switched to DP/DN for logging purpose during debugging scenarios, even AP hang up happens when FSA4486 stays audio or other mode.

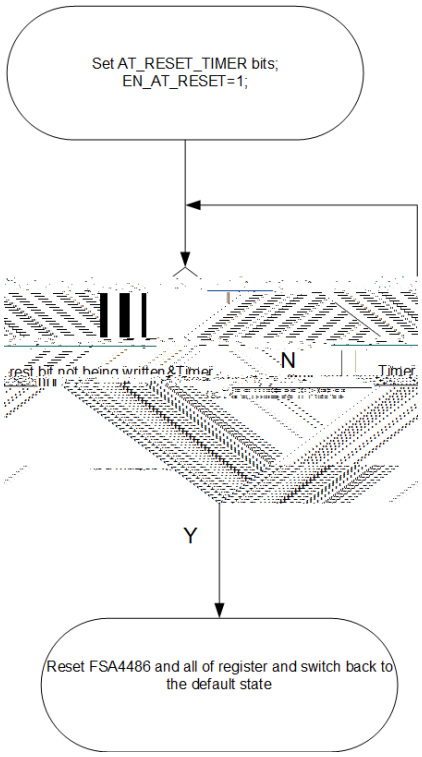

Figure 4. Auto Reset

I²C INTERFACE

The FSA4486 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 2.1 requirements. This block is designed for fast mode, 400 kHz, signals.

Examples of an I²C write and read sequence are shown in below figures respectively.

Figure 5. I²C Write Example

Figure 6. I²C Read Example

Test Diagrams

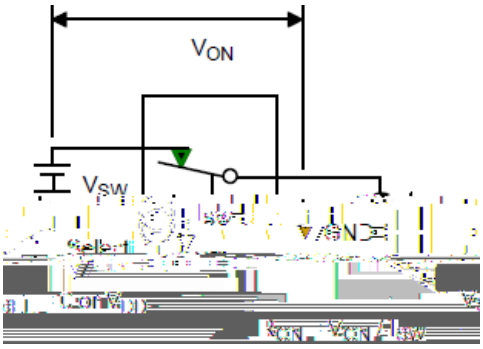

Figure 7. On Resistance

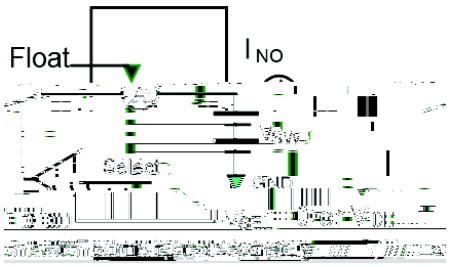

Figure 8. Off Leakage (Ioz)

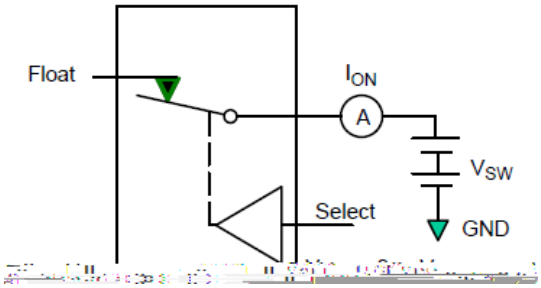

Figure 9. On Leakage

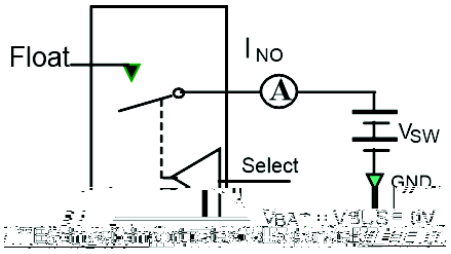

Figure 10. Power Off Leakage (Ioff)

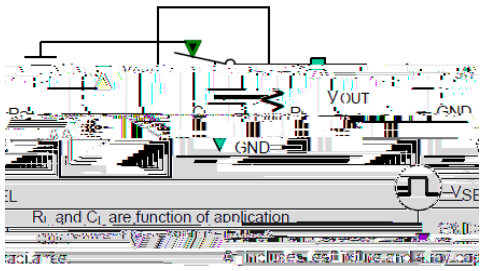

Figure 11. Test Circuit Load

Figure 12. Turn On/Off Waveforms under Manual Mode

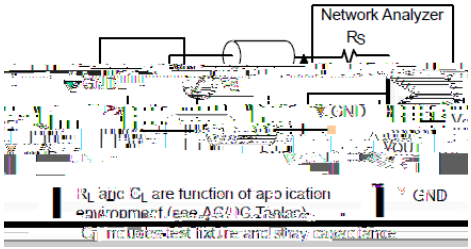

Figure 13. Bandwidth

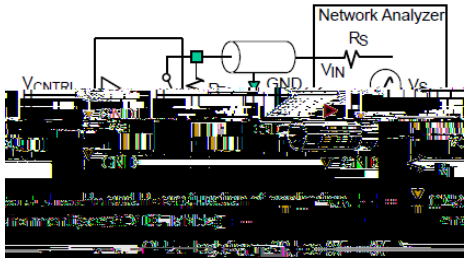

Figure 14. Channel Off Isolation

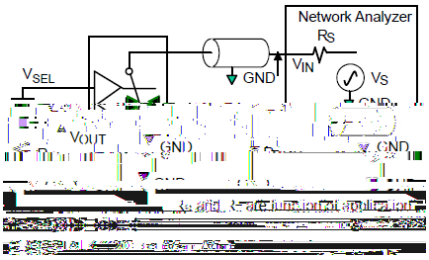

Figure 15. Adjacent Channel Crosstalk

Figure 16. Channel Off Capacitance

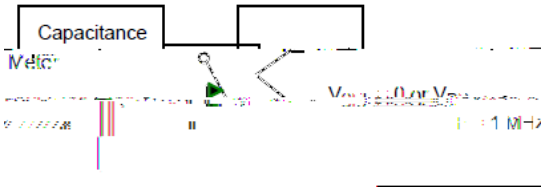

Figure 17. Channel On Capacitance

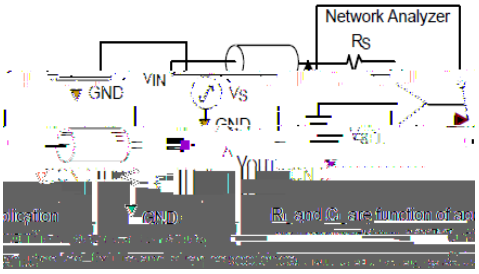

Figure 18. Total Harmonic Distortion (THD+N)

ORDERING INFORMATION

Part Number	Marking	Operating Temperature	Package Type	Shipping†
FSA4486UCX	6E	−40 to +85°C	25−Ball WLCSP, Non−JEDEC 2.24 x 2.28 mm, 0.4 mm Pitch (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WLCSP25 2.24x2.28x0.586
CASE 567UZ
ISSUE B

DATE 03 JAN 2018

PER

ASM