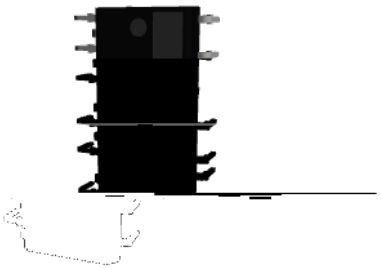
Motion SPM® 5 Series

FSB50550BB



FSB50550BB	FSB50550BB	SPM5T−021 (Pb−Free)	Rail	15

	(Each MOSFET Unless Otherwise Specified)			
V_{DSS}	Drain−Source Voltage of Each MOSFET		500	V
*$I_{D\ 25}$	Each MOSFET Drain Current, Continuous	T_C = 25°C	3.0	A
*$I_{D\ 80}$	Each MOSFET Drain Current, Continuous	T_C = 80°C	1.9	A
*I_{DP}	Each MOSFET Drain Current, Peak	T_C = 25°C, PW < 100 μs	7.0	A
*I_{DRMS}	Each FRFET Drain Current, Rms	T_C = 80°C, F_{PWM} < 20 kHz	1.3	A_{rms}
	(Each HVIC Unless Otherwise Specified)			
V_{DD}	Control Supply Voltage	Applied Between V_{DD} and COM	20	V
V_{BS}	High−side Bias Voltage	Applied Between V_B and V_S	20	V
V_{IN}	Input Signal Voltage	Applied Between IN and COM	−0.3~V_{DD} + 0.3	V
	(Each Bootstrap Diode Unless Otherwise Specified.)			
V_{RRMB}	Maximum Repetitive Reverse Voltage		500	V
* I_{FB}	Forward Current	T_C = 25°C	0.5	A
* I_{FPB}	Forward Current (Peak)	T_C = 25°C, Under 1 ms Pulse Width	2.0	A

$R_{th(j−c)Q}$	Junction to Case Thermal Resistance (Note 1)	Each FET under inverter operating condition (Note 1)	8.9	°C/W

T_J	Operating Junction Temperature		−40~150	°C
T_{STG}	Storage Temperature		−40~125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1 minute, Connect Pins to Heat Sink Plate		

1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U−Phase High−Side MOSFET Driving
3	$V_{DD(U)}$	Bias Voltage for U−Phase IC and Low−Side MOSFET Driving
4	$IN_{(UH)}$	Signal Input for U−Phase High−Side
5	$IN_{(UL)}$	Signal Input for U−Phase Low−Side
6	N.C	No Connection
7	$V_{B(V)}$	Bias Voltage for V−Phase High Side MOSFET Driving
8	$V_{DD(V)}$	Bias Voltage for V−Phase IC and Low Side MOSFET Driving
9	$IN_{(VH)}$	Signal Input for V−Phase High−Side
10	$IN_{(VL)}$	Signal Input for V−Phase Low−Side
11	N.C	No Connection
12	$V_{B(W)}$	Bias Voltage for W−Phase High−Side MOSFET Driving
13	$V_{DD(W)}$	Bias Voltage for W−Phase IC and Low−Side MOSFET Driving
14	$IN_{(WH)}$	Signal Input for W−Phase High−Side
15	$IN_{(WL)}$	Signal Input for W−Phase Low−Side
16	V_{TS}	Output for HVIC Temperature Sensing
17	P	Positive DC−Link Input
18	U, $V_{S(U)}$	Output for U−Phase & Bias Voltage Ground for High−Side MOSFET Driving
19	N_U	Negative DC−Link Input for U−Phase
20	N_V	Negative DC−Link Input for V−Phase
21	V, $V_{S(V)}$	Output for V−Phase & Bias Voltage Ground for High−Side MOSFET Driving
22	N_W	Negative DC−Link Input for W−Phase
23	W, $V_{S(W)}$	Output for W Phase & Bias Voltage Ground for High−Side MOSFET Driving

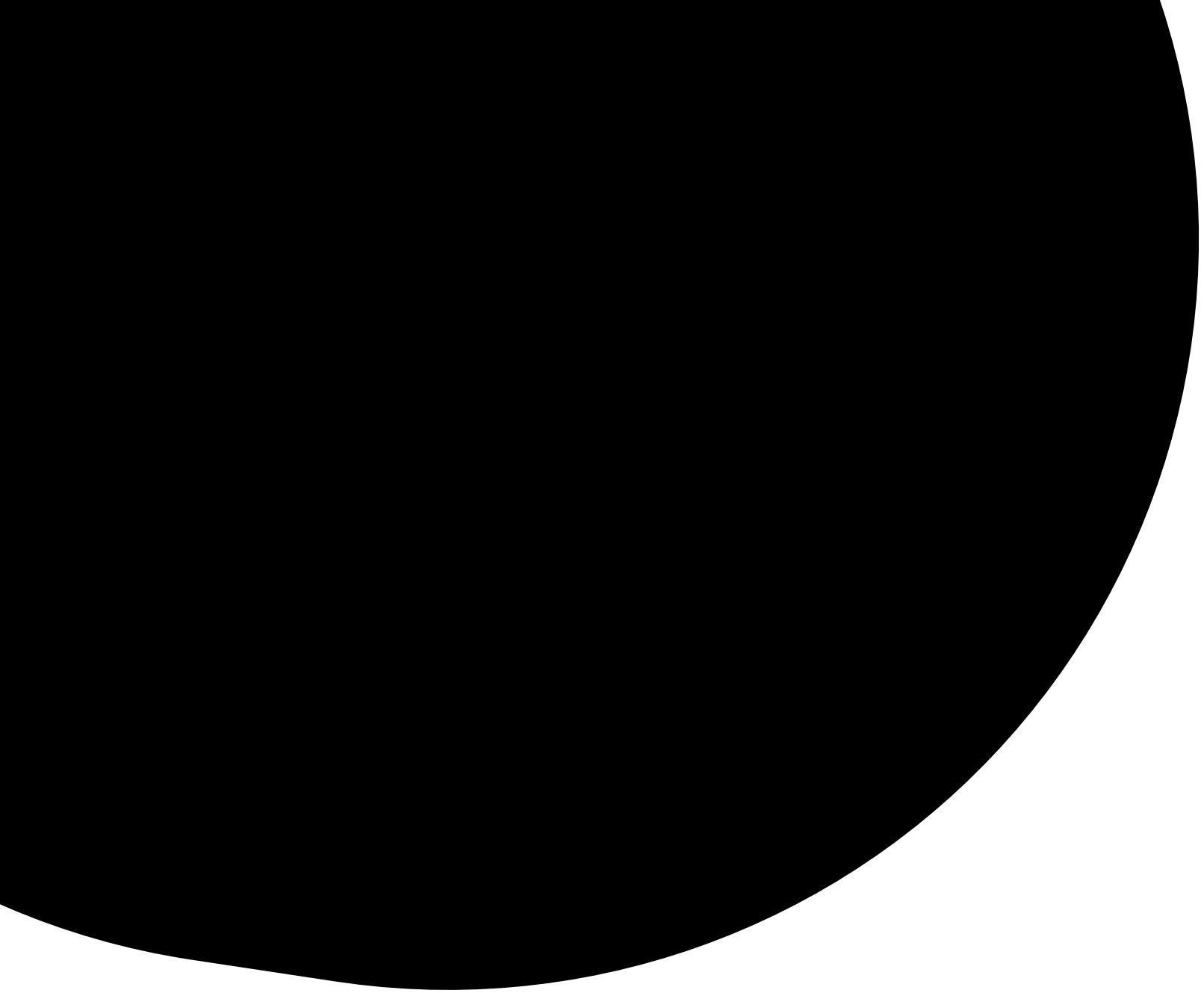
NOTE:
3. Source terminal of each low−

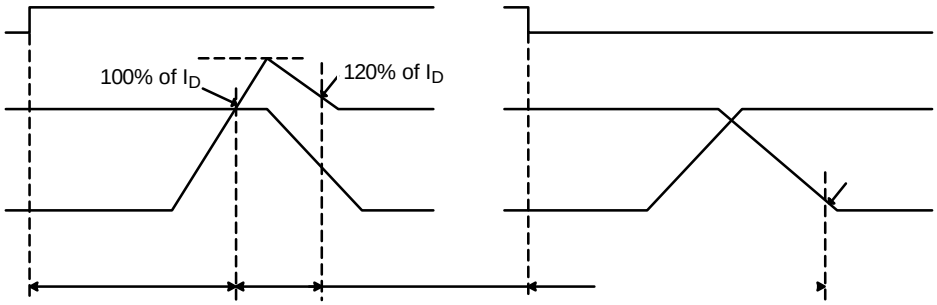
(T_J = 25°C, V_{DD} = V_{BS} = 15 V Unless Otherwise Specified.)

	(Each MOSFET Unless Otherwise Specified)					
BV_{DSS}	Drain − Source Breakdown Voltage	V_{IN} = 0 V, I_D = 1 mA (Note 4)	500	−	−	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{IN} = 0 V, V_{DS} = 500 V	−	−	1	mA
$R_{DS(on)}$	Static Drain − Source Turn−On Resistance	V_{DD} = V_{BS} = 15 V, V_{IN} = 5 V, I_D = 1.2 A	−	2.3	3.0	Ω
V_{SD}	Drain − Source Diode Forward Voltage	V_{DD} = V_{BS} = 15 V, V_{IN} = 0 V, I_D = −1.2 A	−	−	1.3	V
t_{ON}	Switching Times	V_{PN} = 300 V, V_{DD} = V_{BS} = 15 V, I_D = 1.2 A V_{IN} = 0 V ↔ 5 V, Inductive Load L = 3 mH High− and Low−Side MOSFET Switching (Note 5)	460	780	1100	ns
t_{OFF}			1001	1660	2300	ns
t_{rr}			−	230	−	ns

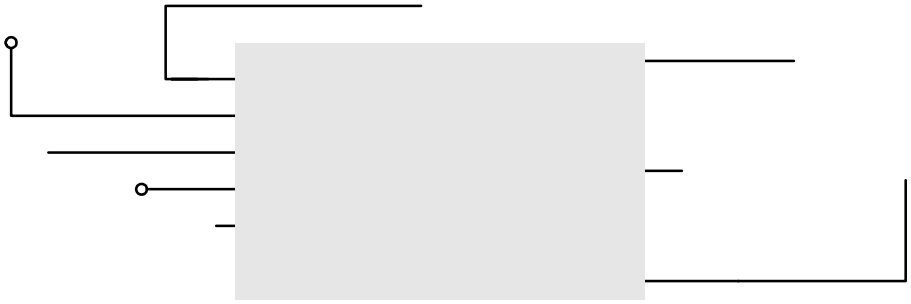
V_{PN}	Supply Voltage	Applied between P and N	−	300	400	V
V_{DD}	Control Supply Voltage	Applied between V_{DD} and COM	13.5	15.0	18.5	V
V_{BS}	High−Side Bias Voltage	Applied between V_B and V_S	13.5	15.0	18.5	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied between V_{IN} and COM	3.0	−	V_{DD}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	−	0.6	V
t_{dead}	Blanking Time for Preventing Arm−Short	V_{DD} = V_{BS} = 13.5~16.5 V, $T_J \leq 150°C$	2	−	−	μs
		V_{DD} = V_{BS} = 12.3~14.4 V, $T_J \leq 150°C$	1	−	−	μs
f_{PWM}	PWM Switching Frequency	$T_J \leq 150°C$	−	15	−	kHz

Functional





(a) Turn−on (b) Turn−off



SPM5T−021 / 21LD, PDD STD, FULL PACK, DOUBLE DIP TYPE
CASE MODET
ISSUE O

DATE 31 JAN 2017

NOTES: UNLESS OTHERWISE SPECIFIED
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