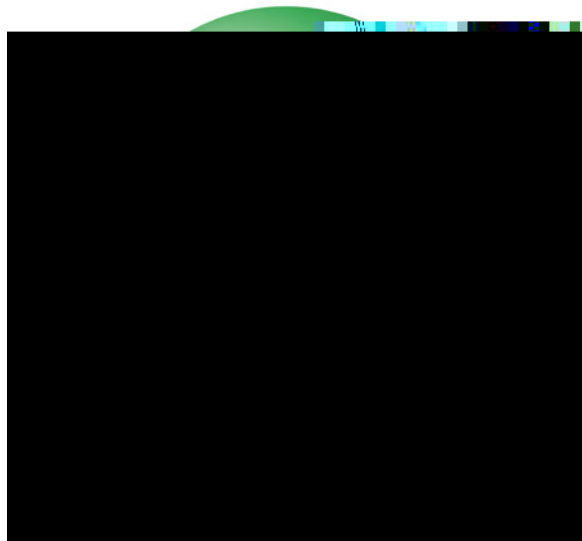




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# FSD176MRT

## Green-Mode Fairchild Power Switch (FPS™)

### Features

- Advanced Soft Burst-Mode Operation for Low Standby Power and Low Audible Noise
- Random Frequency Fluctuation for Low EMI
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis, Output-Short Protection (OSP), and Under-Voltage Lockout (UVLO) with Hysteresis
- Low Operating Current (0.4 mA) in Burst Mode
- Internal Startup Circuit
- Internal High-Voltage SenseFET: 650 V
- Built-in Soft-Start: 15 ms
- Auto-Restart Mode

### Applications

Power Supply for LCD Monitor, STB, and DVD Combination

### Description

The FSD176MRT is an integrated Pulse Width Modulation (PWM) controller and SenseFET specifically designed for offline Switch-Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed-frequency

### Application Circuit

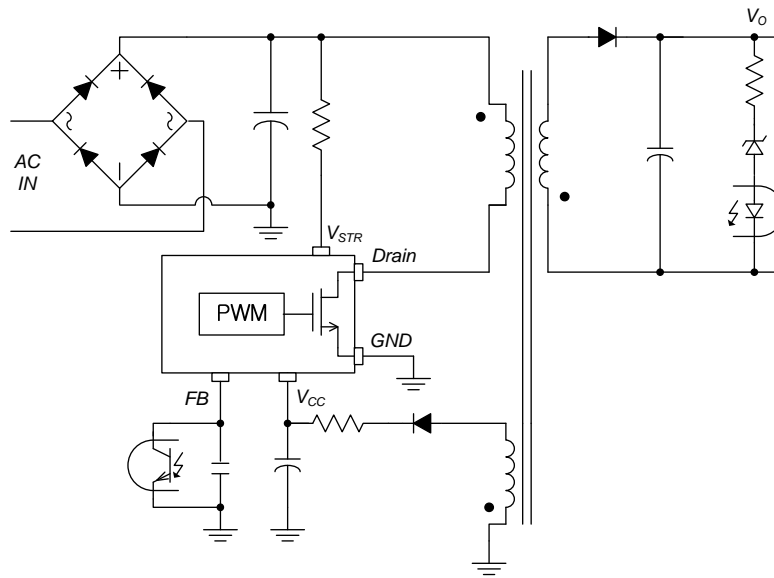
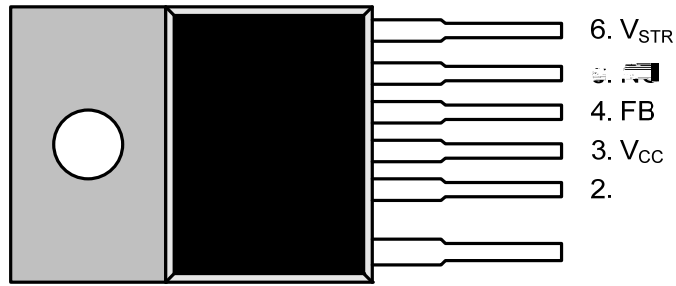


Figure 1. Typical Application Circuit

### Pin Configuration



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{STR}$	$V_{STR}$ Pin Voltage		650	V
$V_{DS}$	Drain Pin Voltage		650	V
$V_{CC}$	$V_{CC}$ Pin Voltage		26	V
$V_{FB}$	Feedback Pin Voltage	- 0.3	12.0	V
$I_{DM}$	Drain Current Pulsed		12.8	A
$I_{DS}$	Continuous Switching Drain Current <sup>(6)</sup>	$T_C=25^\circ\text{C}$	6.4	A
		$T_C=100^\circ\text{C}$	4.0	A

## Electrical Characteristics

T<sub>J</sub> = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
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**Electrical Characteristics** (Continued)





## Typical Performance Characteristics

Characteristic graphs are normalized at  $T_A=25^\circ\text{C}$ .

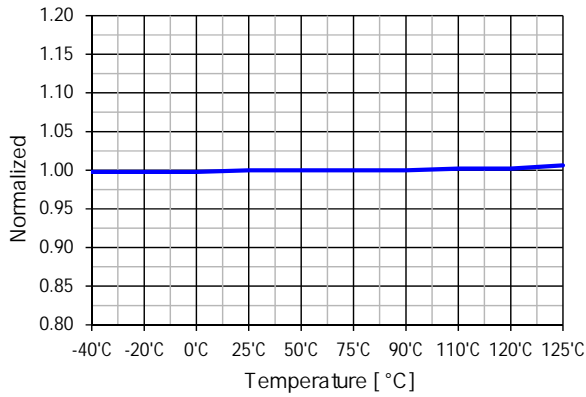


Figure 11. UVLO Threshold Voltage ( $V_{\text{START}}$ ) vs.  $T_A$

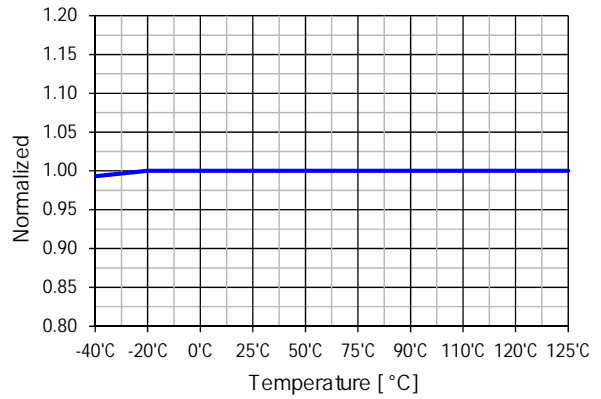


Figure 12. UVLO Threshold Voltage ( $V_{\text{STOP}}$ ) vs.  $T_A$

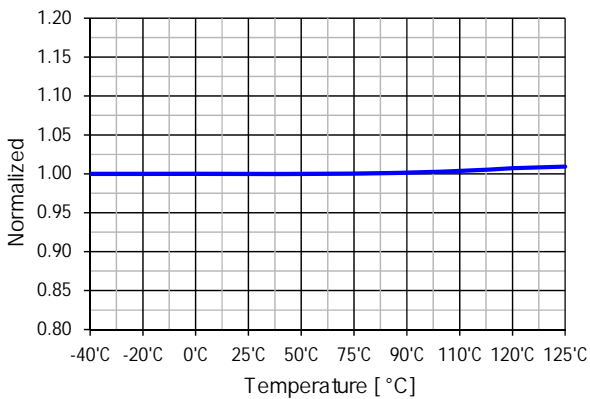


Figure 13. Shutdown Feedback Voltage ( $V_{\text{SD}}$ ) vs.  $T_A$

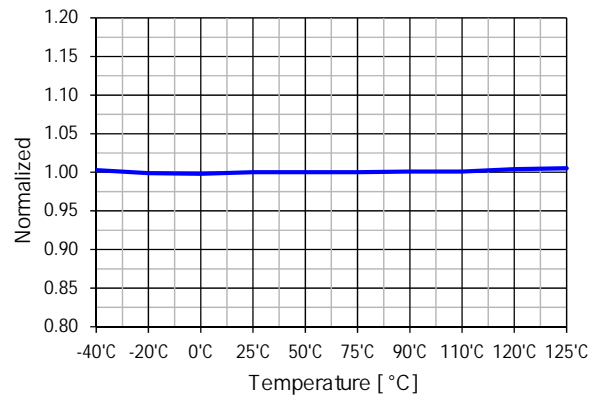


Figure 14. Over-Voltage Protection ( $V_{\text{OVP}}$ ) vs.  $T_A$

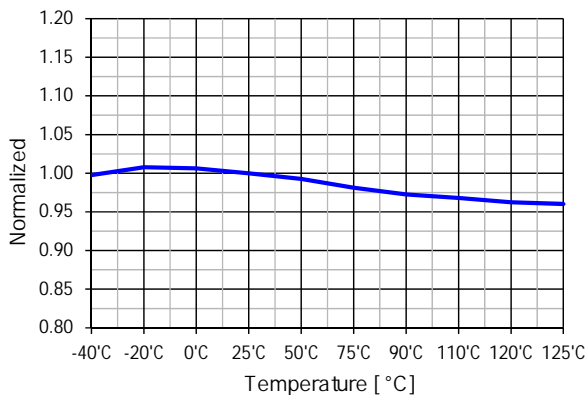


Figure 15. Switching Frequency ( $f_s$ ) vs.  $T_A$

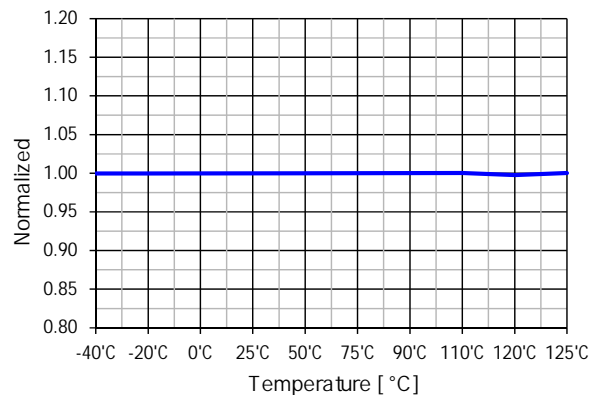
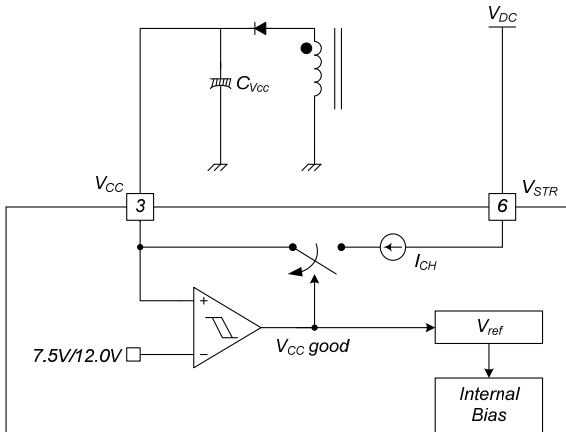


Figure 16. Maximum Duty Ratio ( $D_{\text{MAX}}$ ) vs.  $T_A$

## Functional Description

**1. Startup:** At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor ( $C_{VCC}$ ) connected to the  $V_{CC}$  pin, as illustrated in Figure 17. When  $V_{CC}$  reaches 12 V, the FSD176MRT begins switching and the internal high-voltage current source is disabled. The FSD176MRT continues normal switching operation and the power is supplied from the auxiliary transformer winding unless  $V_{CC}$  goes below the stop voltage of 7.5 V.



**Figure 17. Startup Block**

**2. Soft-Start:** The internal soft-start circuit increases the PWM comparator inverting input voltage, together with the SenseFET current, slowly after startup. The typical soft-start time is 15ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. This helps prevent transformer saturation and reduces stress on the secondary diode during startup.

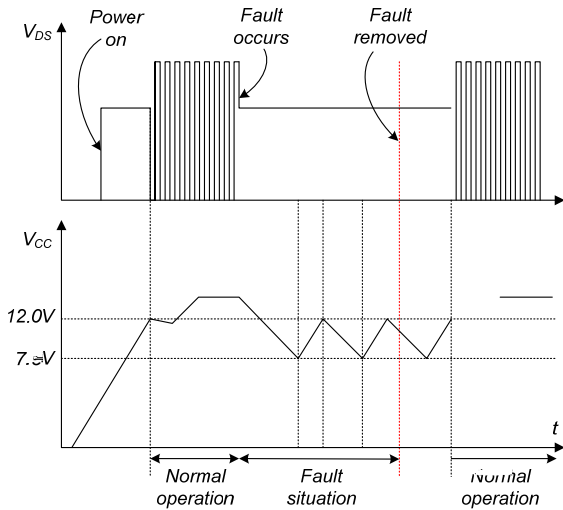
**3. Feedback Control:** This device employs current-mode control, as shown in Figure 18. An opto-coupler (such as the FOD817) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the  $R_{SENSE}$  resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5 V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing drain current. This typically occurs when the input voltage is increased or the output load is decreased.

**3.1 Pulse-by-Pulse Current Limit:** Because current-mode control is employed, the peak current through the SenseFET is limited by the inverting input of the PWM comparator ( $V_{FB}^*$ ), as shown in Figure 18. Assuming that the  $90 \mu A$  current source flows only through the internal resistor ( $3R + R = 27 k \Omega$ ), the cathode voltage of diode D2 is about 2.5 V. Since D1 is blocked when the feedback voltage ( $V_{FB}$ ) exceeds 2.5 V, the maximum voltage of the cathode of D2 is clamped at this voltage. Therefore, the peak value of the current through the SenseFET is limited.

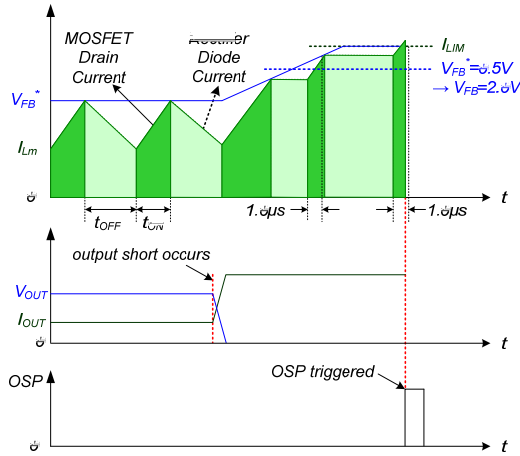
**3.2 Leading-Edge Blanking (LEB):** At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the  $R_{SENSE}$  resistor leads to incorrect feedback operation in the current-mode PWM control. To counter this effect, the leading-edge blanking (LEB) circuit inhibits the PWM comparator for  $t_{LEB}$  (300 ns) after the SenseFET is turned on.



**4. Protection Circuits:** The FSD176MRT has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Output-Short Protection (OSP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart. Once a fault condition is detected, switching is terminated and the SenseFET remains off. This causes  $V_{CC}$  to fall. When  $V_{CC}$  falls to the Under-Voltage Lockout (UVLO) stop voltage of 7.5 V, the protection is reset and the startup circuit charges the  $V_{CC}$  capacitor. When  $V_{CC}$  reaches the start voltage of 12.0 V, the FSD176MRT resumes normal operation. If the fault condition is not removed, the SenseFET remains off and  $V_{CC}$  drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.



**4.3. Output-Short Protection (OSP):** If the output is shorted, steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Such a steep current brings high-voltage stress on the drain of the SenseFET when turned off. To protect the device from this abnormal condition, OSP is included. It is comprised of detecting  $V_{FB}$  and SenseFET turn-on time. When the  $V_{FB}$  is higher than 2.0 V and the SenseFET turn-on time is lower than 1.0  $\mu$ s, the FSD176MRT recognizes this condition as an abnormal error and shuts down PWM switching until  $V_{CC}$  reaches  $V_{START}$  again. An abnormal condition output short is shown in Figure 22.



**Figure 22. Output-Short Protection**

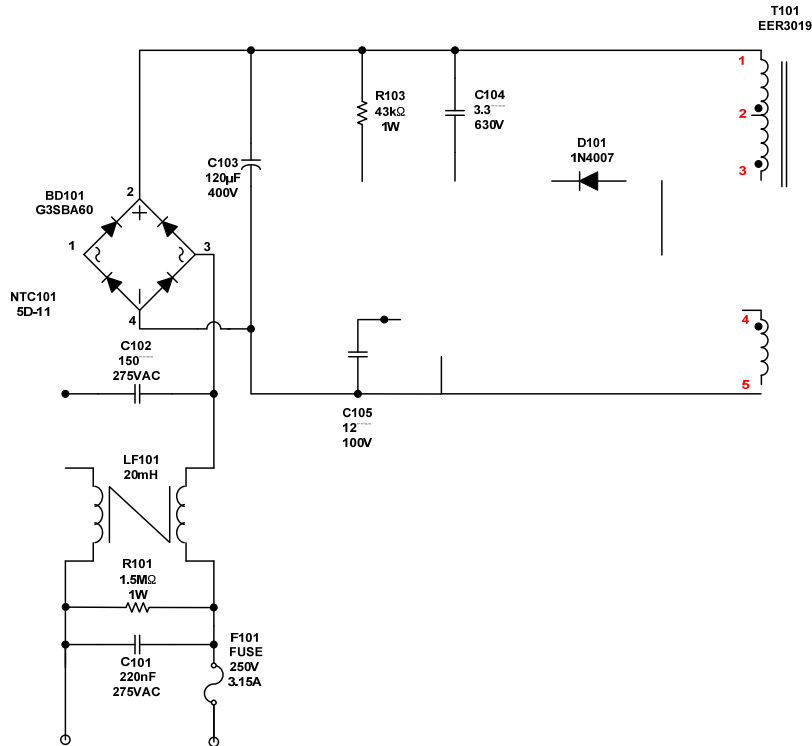
**4.4 Over-Voltage Protection (OVP):** If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then  $V_{FB}$  climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In

### Typical Application Circuit

Application	Input Voltage	Rated Output	Rated Power
LCD Monitor	85 ~ 265 V <sub>AC</sub>	5.0 V (3 A)	64 W
Power Supply		14.0 V (3.5 A)	

#### Key Design Notes:

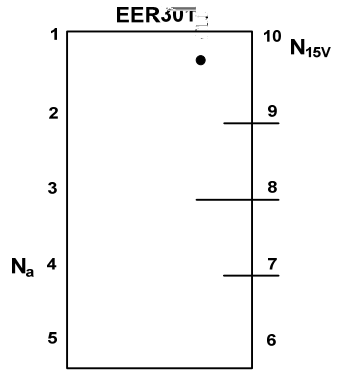
1. The delay for overload protection is designed to be about 30 ms with C105 (8.2 nF). OLP time between 39 ms (12 nF) and 46 ms (15 nF) is recommended.
2. The SMD-type capacitor (C106) must be placed as close as possible to the V<sub>CC</sub> pin to avoid malfunction by abrupt pulsating noises and to improve ESD and surge immunity. Capacitance between 100 nF and 220 nF is recommended.



### Transformer Specification

Core: EER3019 ( $A_e=134 \text{ mm}^2$ )

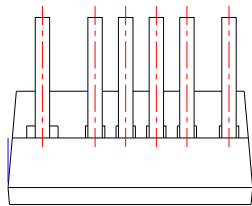
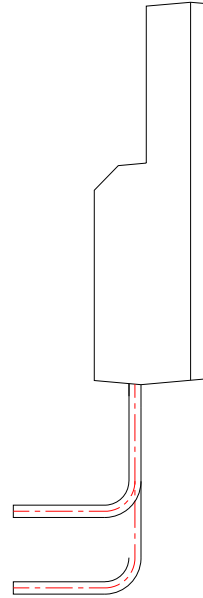
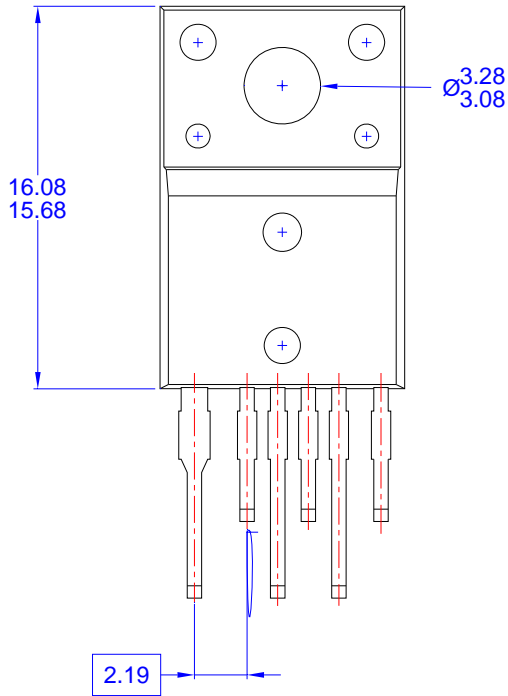
Bobbin: EER3019



**Table 3. Bill of Materials**

Part #	Value	Note	Part #	Value	Note
<b>Fuse</b>			<b>Capacitor</b>		
F101	250 V 3.15 A		C101	220 nF / 275 V	Box (Pilkor)
<b>NTC</b>			C102	150 nF / 275 V	Box (Pilkor)
NTC101	5D-11	DSC	C103	120 μF / 400 V	Electrolytic (SamYoung)
<b>Resistor</b>			C104	3.3 nF / 630 V	Film (Sehwa)
R101	1.5 M , J	1 W	C105	12 nF / 100 V	Film (Sehwa)
R103	43 k , J	1 W	C106	220 nF	SMD (2012)
R201	1 k , F	1/4 W, 1%	C107	47 μF / 50 V	Electrolytic (SamYoung)
R202	1.2 k , F	1/4 W, 1%	C201	1000 μF / 25 V	Electrolytic (SamYoung)

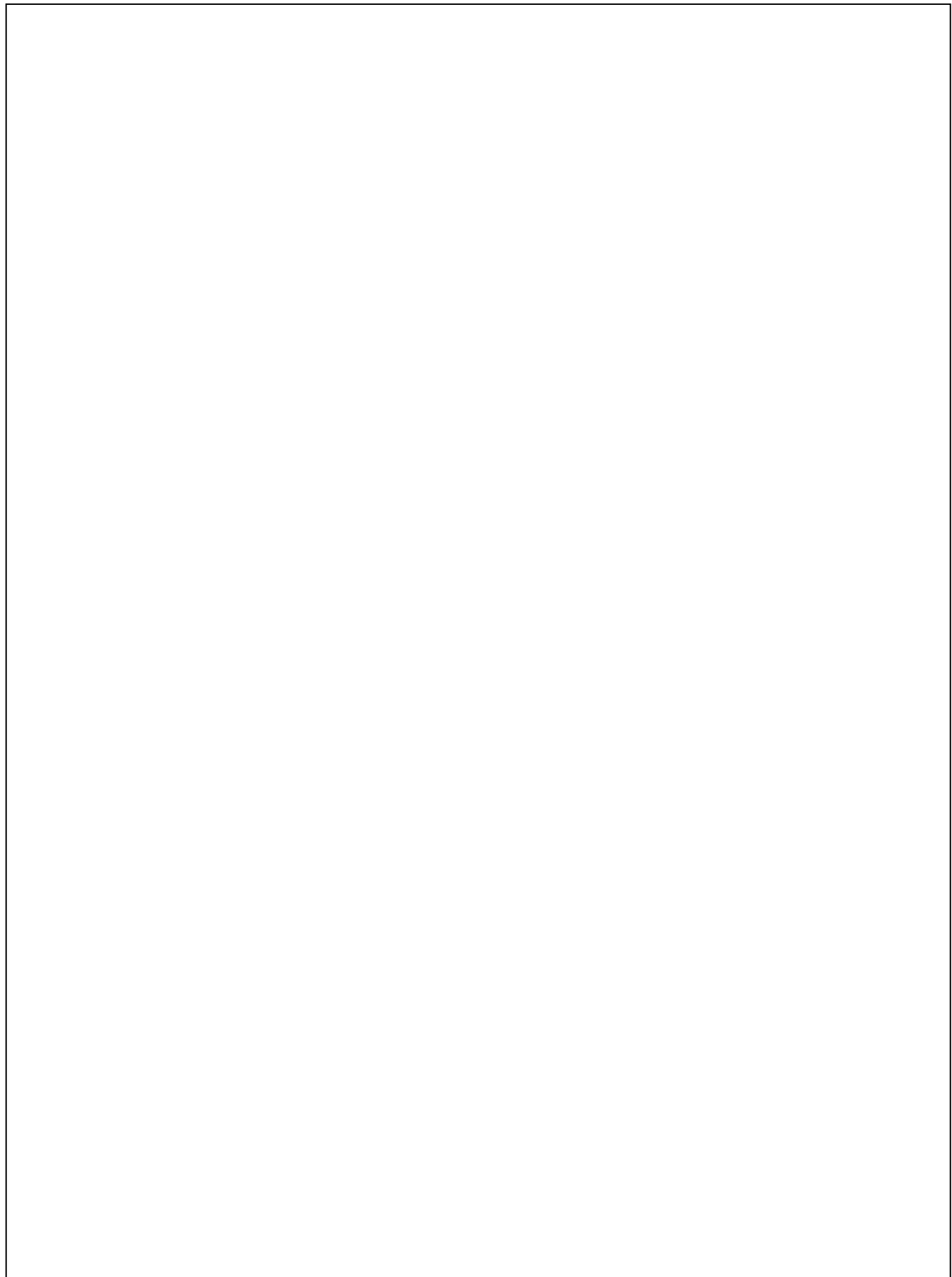
### Physical Dimensions



**NOTES:**

- A) NO PACKAGE STANDARD APPLIES.
- B) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C) DIMENSIONS ARE IN MILLIMETERS.
- D) DRAWING FILENAME : MKT-TO220E06REV2





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