ures

- rnal Avalanche Rugged SenseFET
- vanced Burst-Mode Operation Consumes Under One at 240VAC & 0.5W Load
- ecision Fixed Operating Frequency (66kHz)
- ternal Start-up Circuit
- nproved Pulse by Pulse Current Limiting
- ver Voltage Protection (OVP) : Auto-Restart
- Over Load Protection (OLP): Auto-Restart
- nternal Thermal Shutdown (TSD) : Auto-Restart
- Under Voltage Lock Out (UVLO) with Hysteresis
- Low Operating Current (2.5mA)
- Built-in Soft Start

Application

- SMPS for LCD monitor and STB
- Adapter

Related Application Notes

- **AN4137** - Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS)
- **AN4140** - Transformer Design Consideration for Off-line Flyback Converters Using Fairchild Power Switch
- **AN4141** - Troubleshooting and Design Tips for Fairchild Power Switch Flyback Applications
- **AN4148** - Audible Noise Reduction Techniques for FPS Applications

Description

The FSDM0465RB is an integrated Pulse Width Modulator (PWM) and SenseFET specifically designed for high performance offline Switch Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high voltage power switching regulator which combines a rugged avalanche, SenseFET with a current mode PWM control block. The PWM controller includes integrated fixed frequency oscillator, under voltage lockout, leading edge blanking (LEB), optimized gate driver, internal soft start, temperature compensated precise current sources for a loop compensation and self protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the PWM/ FSDMRB can reduce total cost, component count, size and weigh, while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform well suited for cost-effective designs of flyback converters.

OUTPUT POWER TABLE (4)

	230VAC ±15%(3)	85-265VAC
PRODUCT	Adapter(1)	

Table 1. Maximum Output Power

Notes:

1. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient.
2. Maximum practical continuous power in an open frame design at 50°C ambient.
3. 230 VAC or 100/115 VAC with doubler.
4. The junction temperature can limit the maximum output power.

Typical Circuit

Figure 1. Typical Flyback Application

Internal Block Diagram

Figure 2. Functional Block Diagram of FSDM0465RB

Pin Description

Pin Number	Pin Name	Pin Function Description
1	Drain	This pin is the high voltage power SenseFET drain. It is designed to drive the transformer directly.
2	GND	This pin is the control ground and the SenseFET source.
3	Vcc	This pin is the positive supply voltage input. During start up, the power is supplied by an internal high voltage current source that is connected to the Vstr pin. When Vcc reaches 12V, the internal high voltage current source is disabled and the power is supplied from the auxiliary transformer winding.
4	Vfb	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6.0V, the over load protection is activated resulting in shutdown of the FPS^{TM}.
5	N.C	-
6	Vstr	This pin is connected directly to the high voltage DC link. At startup, the internal high voltage current source supplies internal bias and charges the external ca-

Pin Assignments

Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	650	V
Vstr Max Voltage	V_{STR}	650	V
Pulsed Drain Current (Tc=25°C)(1)	I_{DM}	9.6	A
Continuous Drain Current (Tc=25°C) (2)	I_D	2.2	A (rms)
Continuous Drain Current (Tc=100°C) (2)		1.4	A (rms)
Continuous Drain Current* (T_{DL}=25°C)(3)	I_D*	4	A (rms)
Single Pulsed Avalanche Energy (4)	E_{AS}	-	mJ
Supply Voltage	V_{CC}	20	V
Input Voltage Range	V_{FB}	-0.3 to V_{CC}	V
Total Power Dissipation (Tc=25°C) (2)	P_D	33	W
Operating Junction Temperature	T_j	Internally limited	°C
Operating Ambient Temperature	T_A	-25 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
ESD Capability, HBM Model (All pins except Vstr and Vfb)	-	2.0 (GND-Vstr/Vfb=1.5kV)	kV
ESD Capability, Machine Model (All pins except Vstr and Vfb)	-	300 (GND-Vstr/Vfb=225V)	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Tc: Case Back Surface Temperature (With infinite heat sink)
3. T_{DL}: Drain Lead Temperature (With infinite heat sink)
4. L=14mH, starting Tj=25°C2. L=14mH, starting Tj=25°C

Thermal Impedance

Parameter	Symbol	Value	Unit
Junction-to-Ambient Thermal	θ_{JA}	-	°C/W
Junction-to-Case Thermal	θ_{JC}(1)	3.78	°C/W

Notes:

1. Infinite cooling condition - refer to the SEMI G30-88.

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SenseFET SECTION						
Drain Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	650	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V	-	-	250	μA
		V_{DS}= 520V V_{GS} = 0V, T= 520V= 520V				

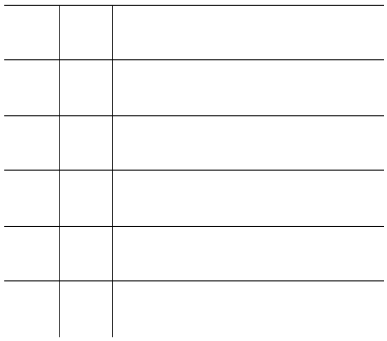
Electrical Characteristics (Continued)

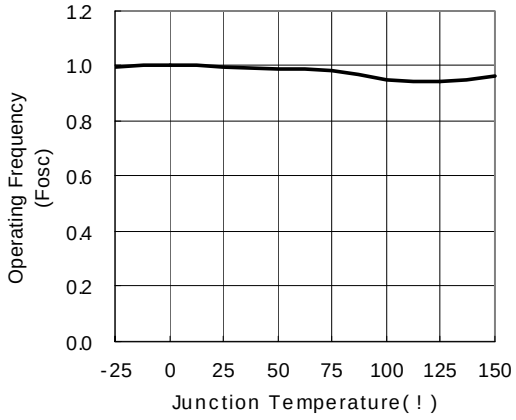
(Ta = 25°C unless otherwise specified)

Notes:
1. Pulse test: Pulse width ≤ 300μS, duty ≤ 2%
2. These parameters, although guaranteed at the design, are not tested in mass production.
3. These parameters indicate the inductor current.
4. This parameter is the current flowing into the control IC.

Typical Performance Characteristics

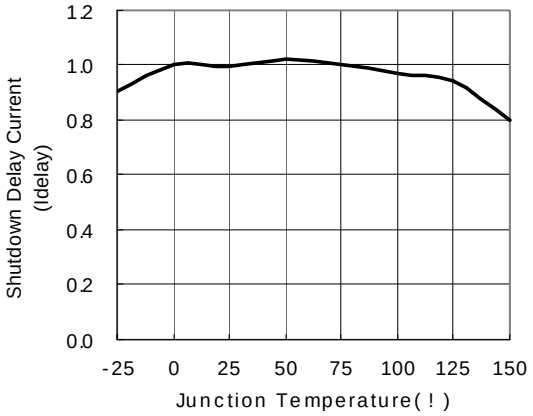
(These Characteristic Graphs are Normalized at Ta= 25°C)

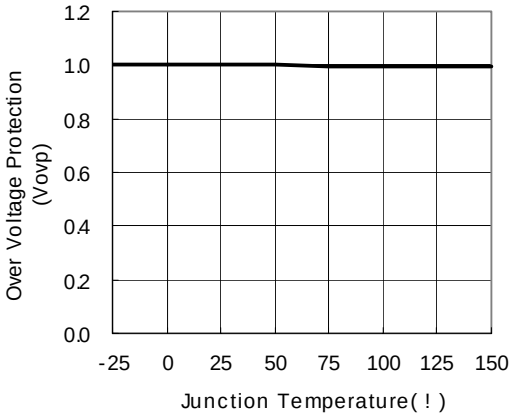


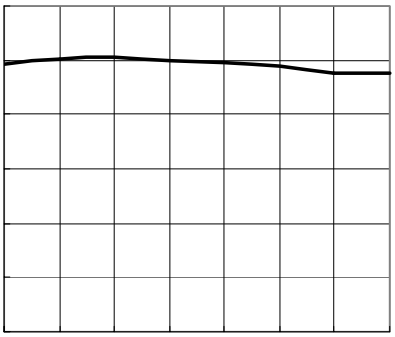


Typical Performance Characteristics (Continued)

(These Characteristic Graphs are Normalized at Ta= 25°C)







Functional Description

1. Startup: In previous generations of Fairchild Power Switches (FPS™) the Vcc pin had an external start-up resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high voltage current source. At startup, an internal high voltage current source supplies the internal bias and charges the external capacitor (C_a

Figure 6. Auto Restart Operation

3.1 Over Load Protection (OLP): Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS.
However, even when the SMPS is operation normally, the over load protection circuit can be activated during the load transition. To avoid this undesired operation, the over load protection circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation.
Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (Vfb).
If Vfb exceeds 2.5V, D1 is blocked and the 3.5uA current source starts to charge C_B slowly up to Vcc.
In this condition, Vfb continues increasing until it reaches 6V, when the switching operation is terminated as shown in Figure 7. The delay time for shutdown is the time required to charge C_B from 2.5V to 6.0V with 3.5uA.
In general, a 10 ~ 50 ms delay time is typical for most applications.

Figure 7. Over Load Protection

3.2 Over Voltage Protection (OVP): If the secondary side

5. Burst Operation: To minimize power dissipation in standby mode, the FSDM0465RB enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 8, the device automatically enters burst mode when the feedback voltage drops below V_{BURL}(500mV). At this point switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}(700mV), switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power SenseFET thereby reducing switching loss in Standby mode.

Figure 8. Waveforms of Burst Operation

Typical application circuit

Features

- High efficiency (>81% at 85Vac input)
- Low zero load power consumption (<300mW at 240Vac input)
- Low standby mode power consumption (<800mW at 240Vac input and 0.3W load)
- Low component count

2. Transformer Schematic Diagram

3.Winding Specification

4.Electrical Characteristics

5. Core & Bobbin

Core: EER 3016

6.Demo Circuit Part List

Part	Value	Note	Part	Value	Note
	Fuse		C301	4.7nF	Polyester Film Cap.
F101	2A/250V				
	NTC			**Inductor**	
RT101	5D-9		L201	5uH	Wire 1.2mm
	Resistor		L202	5uH	Wire 1.2mm
R101	560K	1W			
R102	30K	1/4W			
R103	56K	2W			
R104	5	1/4W		**Diode**	
R105	40K	1/4W	D101	UF4007	
R201	1K	1/4W	D102	TVR10G	

Ordering Information

Product Number	Package	Marking Code	BVdss	Rds(on) Max.
FSDM0465RBWDTU	TO-220F-6L(Forming)	DM0465R	650V	2.6 Ω

WDTU: Forming Type