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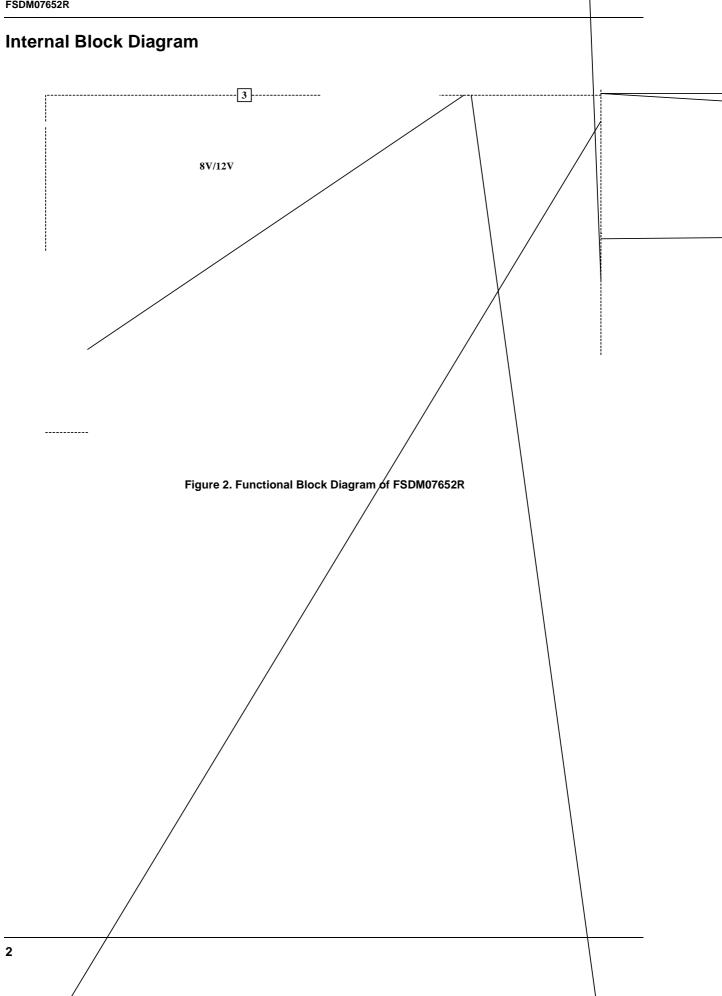
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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild questions@onsemi.com.

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Pin Definitions

Pin Number Pin Name

Pin Function Description

Pin Configuration

Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-source voltage	VDSS	650	V
Vstr Max Voltage	VSTR	650	V
Pulsed Drain current (Tc=25°C) ⁽¹⁾	IDM	15	ADC
Continuous Drain Current(Tc=25°C)	la	3.8	А
Continuous Drain Current(Tc=100°C)	ID	2.4	А
Single pulsed avalanche energy ⁽²⁾	Eas	370	mJ
Single pulsed avalanche current ⁽³⁾	IAS	-	А
Supply voltage	Vcc	20	V
Input voltage range	VFB	-0.3 to VCC	V
Total power dissipation(Tc=25°C)	P _D (Watt H/S)	45	W
Operating junction temperature	Тј	Internally limited	°C
Operating ambient temperature	TA	-25 to +85	°C
Storage temperature range	TSTG	-55 to +150	°C
ESD Capability, HBM Model (All pins excepts for Vstr and Vfb)	-	2.0 (GND-Vstr/Vfb=1.5kV)	kV
ESD Capability, Machine Model (All pins excepts for Vstr and Vfb)	-	300 (GND-Vstr/Vfb=225V)	V

Notes:

1. Repetitive rating: Pulse width limited by maximum junction temperature

2. L=14mH, starting Tj=25°C

3. L=13uH, starting Tj=25°C

Thermal Impedance

Parameter	Symbol	Value	Unit
Junction-to-Ambient Thermal	$ heta_{JA^{(1)}}$	49.90	°C/W
Junction-to-Case Thermal	$\theta_{JC}^{(2)}$	2.78	°C/W

Notes:

1. Free standing with no heat-sink under natural convection.

2. Infinite cooling condition - Refer to the SEMI G30-88.

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Sense FET SECTION						
Drain source breakdown voltage	BVDSS	$VGS = 0V, ID = 250\mu A$	650	-	-	V
		VDS = 650V, VGS = 0V	-	-	50	μA
Zero gate voltage drain current	IDSS	V _{DS} = 520V				

FSDM07652R

Shutdown delay current	IDELAY	V _{FB} =5V	2.8	3.5	4.2	μΑ
TOTAL DEVICE SECTION						
	IOP	VFB=GND, VCC=14V				
Operating supply current ⁽⁵⁾	IOP(MIN)	VFB=GND, VCC=10V	-	2.5	5	mA
	IOP(MAX)	VFB=GND, V _{CC} =18V				

Notes:

- 1. Pulse test : Pulse width $\leq 300 \mu S,\,duty \leq 2\%$
- 2. These parameters, although guaranteed at the design, are not tested in mass production.
- 3. These parameters, although guaranteed, are tested in EDS(wafer test) process.
- 4. These parameters indicate the inductor current.
- 5. This parameter is the current flowing into the control IC.

Comparison Between FS6M07652RTC and FSDM07652R

Function	FS6M07652RTC	FSDM07652R	FSDM07652R Advantages
Soft-Start	Adjustable soft-start time using an external capacitor	Internal soft-start with typically 10ms (fixed)	 Gradually increasing current limit during soft-start further reduces peak current and voltage component stresses Eliminates external components used for soft-start in most applications Reduces or eliminates output overshoot
Burst Mode Operation	 Built into controller Output voltage drops to around half 	Built into controllerOutput voltage fixed	Improve light load efficiencyReduces no-load consumption

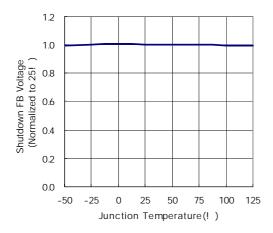
Typical Performance Characteristics

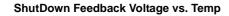
(These Characteristic Graphs are Normalized at Ta= 25°C)

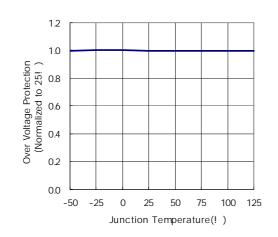
Operating Current vs. Temp

Typical Performance Characteristics (Continued)

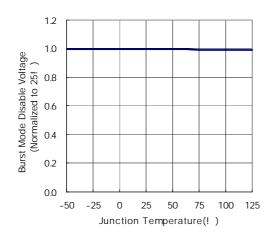
(These Characteristic Graphs are Normalized at Ta= 25°C)



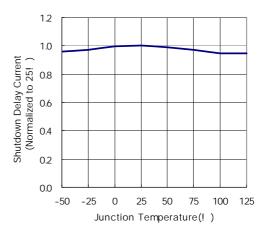




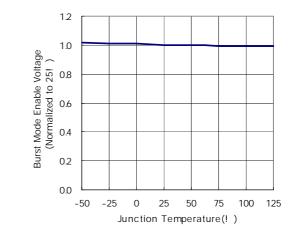
Over Voltage Protection vs. Temp



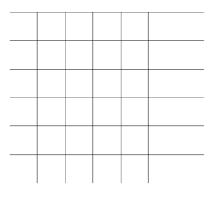
Burst Mode Disable Voltage vs. Temp



ShutDown Delay Current vs. Temp



Burst Mode Enable Voltage vs. Temp



Current Limit vs. Temp

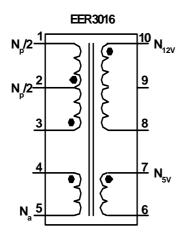
Typical Performance Characteristics (Continued)

(These Characteristic Graphs are Normalized at Ta= 25°C)

Soft Start Time vs. Temp

output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, Vcc is proportional to the output voltage and the FPSTM uses Vcc instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, an OVP circuit is activated resulting in the termination of the FSDM07652R

2. Transformer Schematic Diagram



3.Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
Na	$4 \rightarrow 5$	$0.2^{\phi} imes 1$	8	Center Winding
Insulation:	Polyester Tape t = 0.05	i0mm, 2Layers		
Np/2	$2 \rightarrow 1$	$0.4^{ m \phi} imes$ 1	18	Solenoid Winding
Insulation:	Polyester Tape t = 0.05	i0mm, 2Layers		
N12v	$10 \rightarrow 8$	$0.3^{\phi} imes 3$	7	Center Winding
Insulation:	Polyester Tape t = 0.05	i0mm, 2Layers		
N5v	$7 \rightarrow 6$	$0.3^{\phi} imes 3$	3	Center Winding
Insulation:	Polyester Tape t = 0.05	i0mm, 2Layers		•
Np/2	$3 \rightarrow 2$	$0.4^{ m \phi} imes$ 1	18	Solenoid Winding
Outer Insu	lation: Polyester Tape t	= 0.050mm, 2Layers	•	•

4.Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	520uH ± 10%	100kHz, 1V
Leakage Inductance	1 - 3	10uH Max	2 nd all short

5. Core & Bobbin

Core : EER 3016 Bobbin : EER3016 Ae(mm2) : 96

6.Demo Circuit Part List

7. Layout

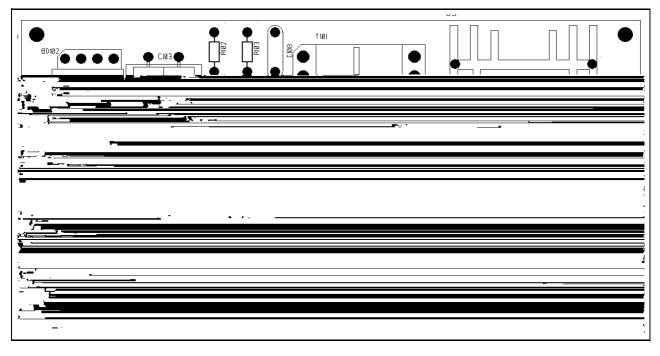


Figure 10. Layout Considerations for FSDM07652R

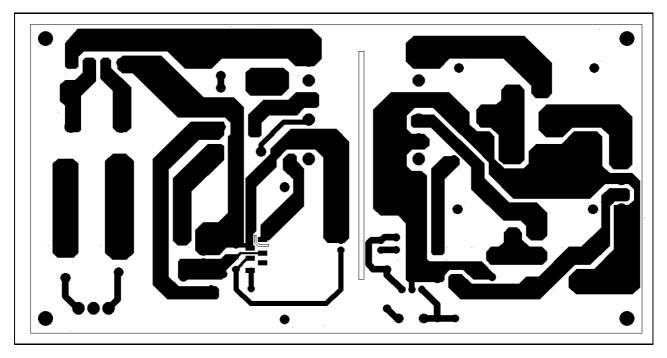


Figure 11. Layout Considerations for FSDM07652R

Ordering Information

Product Number	Package	Marking Code	BVdss	Rds(on)Max.
FSDM07652RWDTU	TO-220F-6L(Forming)	DM07652R	650V	1.6 Ω

WDTU : Forming Type

FSDM07652R

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