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Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	Drain	This pin is the high voltage power Sense FET drain. It is designed to drive the transformer directly.
2	GND	This pin is the control ground and the Sense FET source.
3	Vcc	This pin is the positive supply voltage input. During start up, the power is supplied by an internal high voltage current source that is connected to the Vstr pin. When Vcc reaches 12V, the internal high voltage current source is disabled and the power is supplied from the auxiliary transformer winding.
4	Vfb	

Pin Configuration

Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Notes:

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit

TOTAL DEVICE SECTION						
Operating supply current (5)	I_{OP}	V_{FB}=GND, V_{CC}=14V	-	2.5	5	mA
	$I_{OP(MIN)}$	V_{FB}=GND, V_{CC}=10V				
	$I_{OP(MAX)}$	V_{FB}=GND, V_{CC}=18V				

Notes:

1. Pulse test : Pulse width ≤ 300μS, duty ≤ 2%
2. These parameters, although guaranteed at the design, are not tested in mass production.
3. These parameters, although guaranteed, are tested only in EDS(wafer test) process.
4. These parameters indicate the inductor current.
5. This parameter is the current flowing into the control IC.

Comparison Between FS6M07652RTC and FSDM07652RB

Function	FS6M07652RTC	FSDM07652RB	FSDM07652RB Advantages
Soft-Start	Adjustable soft-start time using an external capacitor	Internal soft-start with typically 10ms (fixed)	• Gradually increasing current limit during soft-start further reduces peak current and voltage component stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
Burst Mode Operation	• Built into controller • Output voltage drops to around half	• Built into controller • Output voltage fixed	• Improve light load efficiency • Reduces no-load consumption

Typical Performance Characteristics

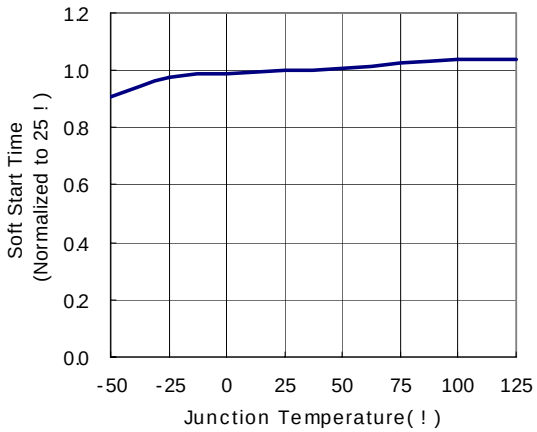
(These Characteristic Graphs are Normalized at Ta= 25°C)

Operating Current vs. Temp

Start Threshold Voltage vs. Temp

Typical Performance Characteristics (Continued)

(These Characteristic Graphs are Normalized at Ta= 25°C)



Soft Start Time vs. Temp

Functional Description

1. Startup : In previous generations of Fairchild Power Switches (FPS™

Figure 6. Auto restart operation

3.1 Over Load Protection (OLP) : Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is in the normal operation, the over load protection circuit can be activated during the load transition. In order to avoid this undesired operation, the over load protection circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the Sense FET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the

5. Burst operation : In order to minimize power dissipation in standby mode, the FSDM07652RB enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 8, the device automatically enters burst mode when the feedback voltage drops below V_{BURL}(500mV). At this point switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}(700mV) switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power Sense FET thereby reducing switching loss in Standby mode.

Figure 8. Waveforms of burst operation

Typical application circuit

Application	Output power	Input voltage	Output voltage (Max current)
LCD Monitor	40W	Universal input (85-265Vac)	5V (2.0A) 12V (2.5A)

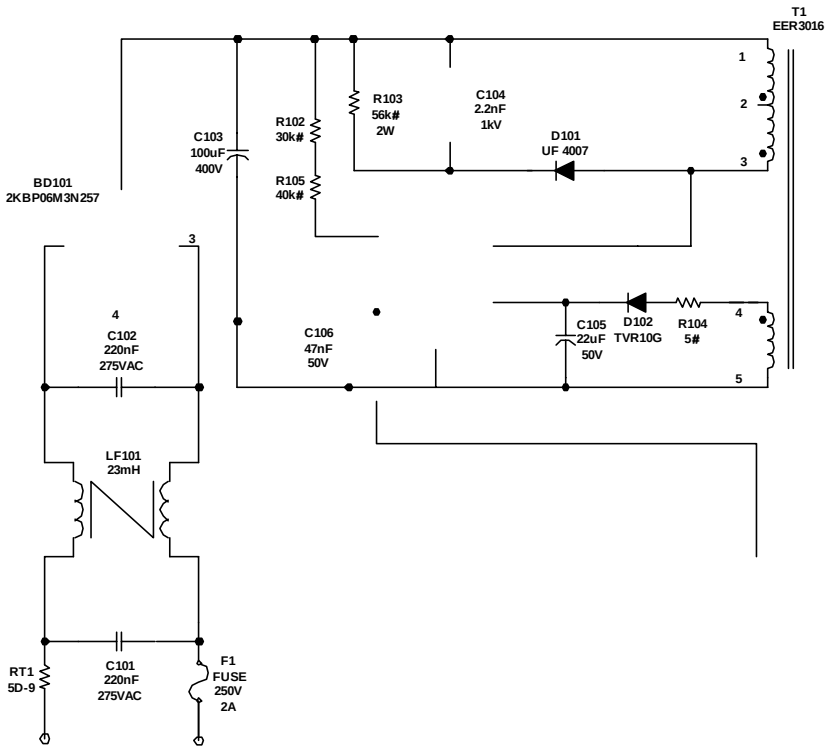
Features

- High efficiency (>81% at 85Vac input)
- Low zero load power consumption (<300mW at 240Vac input)
- Low standby mode power consumption (<800mW at 240Vac input and 0.3W load)
- Low component count
- Enhanced system reliability through various protection functions
- Internal soft-start (10ms)

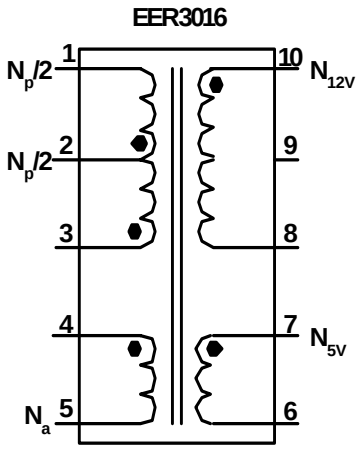
Key Design Notes

- Resistors R102 and R105 are employed to prevent start-up at low input voltage. After startup, there is no power loss in these resistors since the startup pin is internally disconnected after startup.
- The delay time for over load protection is designed to be about 50ms with C106 of 47nF. If a faster triggering of OLP is required, C106 can be reduced to 10nF.
- Zener diode ZD102 is used for a safety test such as UL. When the drain pin and feedback pin are shorted, the zener diode fails and remains short, which causes the fuse (F1) blown and prevents explosion of the opto-coupler (IC301). This zener diode also increases the immunity against line surge.

1. Schematic



2. Transformer Schematic Diagram



3.Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
Na	4 → 5	$0.2^{\phi} \times 1$	8	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	2 → 1	$0.4^{\phi} \times 1$	18	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N_{12V}	10 → 8	$0.3^{\phi} \times 3$	7	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N5V	7 → 6	$0.3^{\phi} \times 3$	3	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	3 → 2	$0.4^{\phi} \times 1$	18	Solenoid Winding
Outer Insulation: Polyester Tape t = 0.050mm, 2Layers				

4.Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	520uH ± 10%	100kHz, 1V
Leakage Inductance	1 - 3	10uH Max	2^{nd} all short

5. Core & Bobbin

Core : EER 3016
Bobbin : EER3016
Ae(mm2) : 96

7. Layout

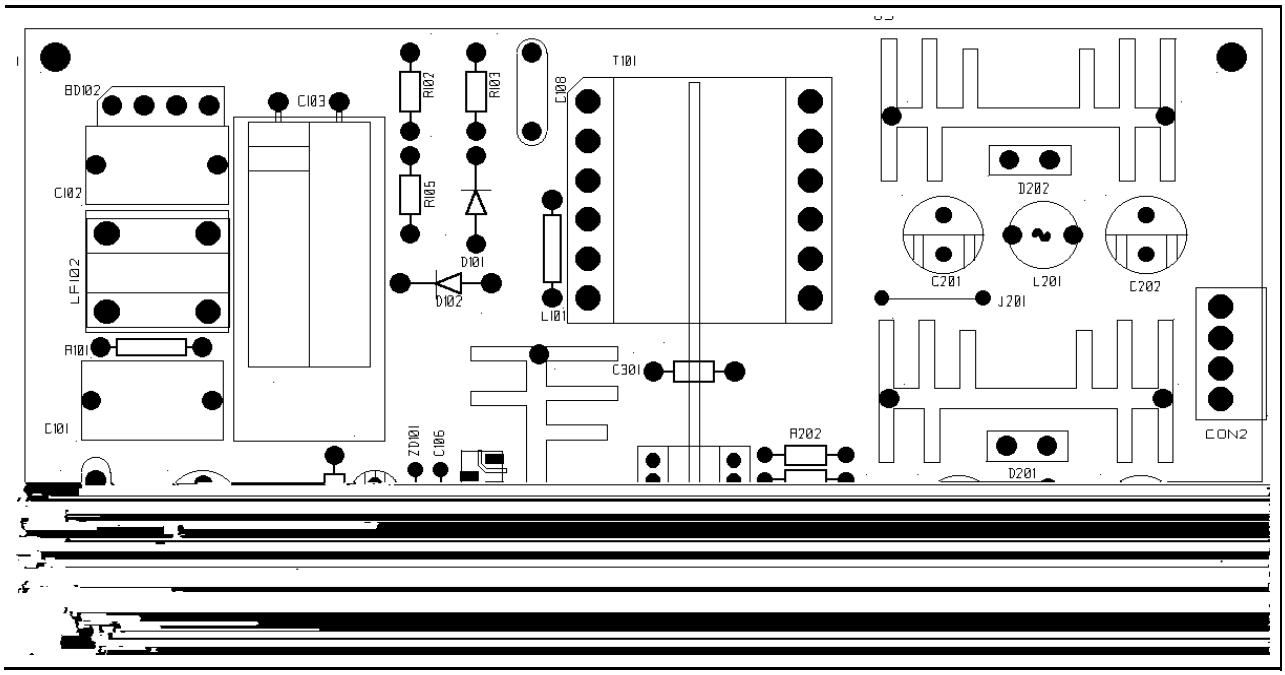


Figure 9. Layout Considerations for FSDM07652RB

Figure 10. Layout Considerations for FSDM07652RB

Package Dimensions

Ordering Information

Product Number	Package	Marking Code	BVdss	Rds(on)Max.
FSDM07652RBWDTU	TO-220F-6L(Forming)	DM07652R	650V	1.6 Ω

WDTU : Forming Type

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