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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at

January 2013

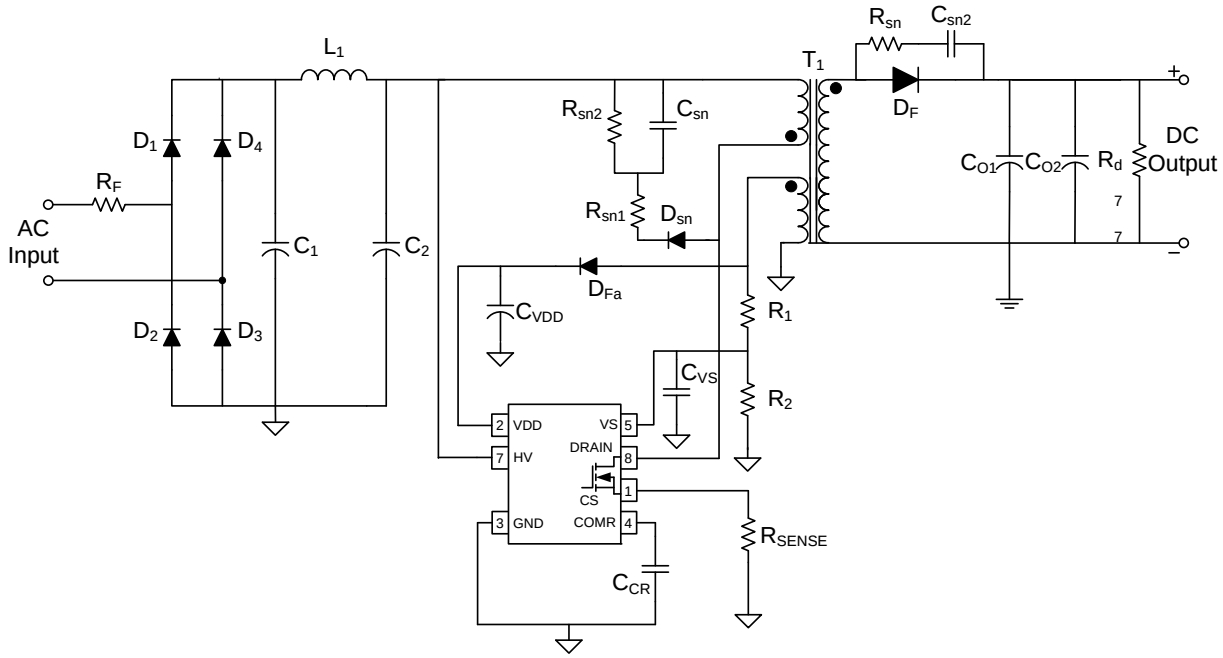
®

FSEZ1317WA
Primary-Side-Regulation PWM with POWER MOSFET Integrated

Features

- Low Standby Power Under 30 mW
- High-Voltage Startup
- Fewest External Component Counts
- Constant-Voltage (CV) and Constant-Current (CC) Control without Secondary-Feedback Circuitry
- Green-Mode: Linearly Decreasing PWM Frequency
- Fixed PWM Frequency at 50 kHz with Frequency

Application Diagram



Marking Information

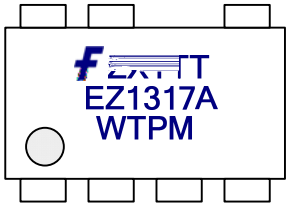


Figure 4. Top Mark

Pin Configuration

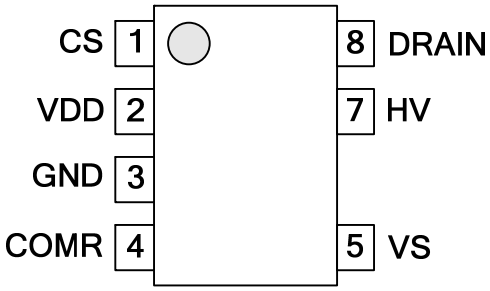


Figure 5. Pin Configuration

Pin Definitions

Pin #	Name	Description

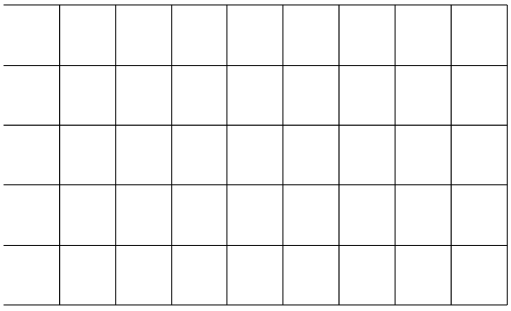
Electrical Characteristics

Unless otherwise specified, V_{DD}=15 V and T_A=25°C.

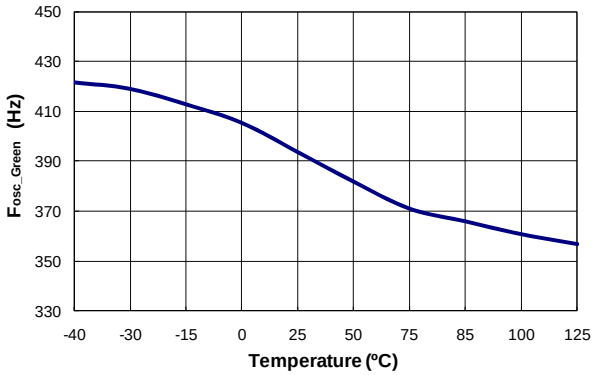
Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
V_{DD} Section							
V_{OP}	Continuously Operating Voltage					23	V
V_{DD-ON}	Turn-On Threshold Voltage			15	16	17	V
V_{DD-OFF}	Turn-Off Threshold Voltage			4.5	5.0	5.5	V
I_{DD-OP}	Operating Current				2.5	5.0	mA
$I_{DD-GREEN}$	Green-Mode Operating Supply Current				0.95	1.45	mA
V_{DD-OVP}	V_{DD} Over-Voltage-Protection Level (OVP)				24		V
$V_{DD-OVP-HYS}$	Hysteresis Voltage for V_{DD} OVP			1.5	2.0	2.5	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage-Protection Debounce Time			50	200	300	µs
HV Startup Current Source Section							
V_{HV-MIN}	Minimum Startup Voltage on HV Pin					50	V
I_{HV}	Supply Current Drawn from HV Pin		V_{AC}=90 V (V_{DC}=100 V); V_{DD}=0 V		1.5	5.0	mA
I_{HV-LC}	Leakage Current after Startup		HV=500 V, V_{DD}=V_{DD-OFF}+1 V		0.96	3.00	µA
Oscillator Section							
f_{OSC}	Frequency	Center Frequency		47	50	53	kHz
		Frequency Hopping Range			±3.5		
$f_{OSC-N-MIN}$	Minimum Frequency at No-Load				370		Hz

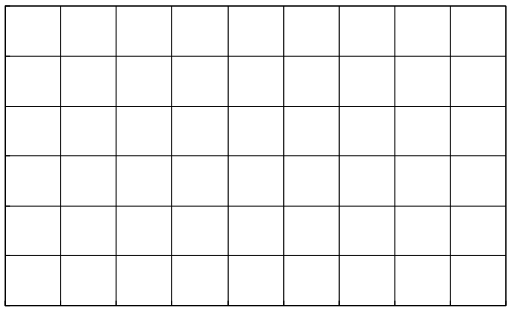
R4 TmHc42.3 .42

Typical Performance Characteristics



Typical Performance Characteristics (Continued)





Functional Description

Figure 24 shows the basic circuit diagram of primary-side regulated flyback converter, with typical waveforms shown in Figure 25. Generally, discontinuous conduction mode (DCM) operation is preferred for primary-side regulation because it allows better output regulation. The operation principles of DCM flyback converter are as follows:

During the MOSFET on time (t_{ON}), input voltage (V_{DL}) is applied across the primary-side inductor (L_m). Then MOSFET current (I_{ds}) increases linearly from zero to the peak value (I

Cable Voltage Drop Compensation

In cellular phone charger applications, the battery is located at the end of cable, which typically causes

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16 V and 5 V, respectively. During startup, the hold-up capacitor must be charged to 16V through the startup resistor to enable the FSEZ1317WA. The hold-up capacitor continues to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} is not allowed to drop below 5 V during this startup process. This UVLO hysteresis window ensures that hold-up capacitor properly supplies V_{DD} during startup.

Protections

The FSEZ1317WA has several self-protection functions, such as Over-Voltage Protection (OVP), Over-Temperature Protection (OTP), and pulse-by-pulse current limit. All the protections are implemented as auto-restart mode. Once the abnormal condition occurs, the switching is terminated and the MOSFET remains off, causing V_{DD} to drop. When V_{DD} drops to the V_{DD} turn-off voltage of 5 V, internal startup circuit is enabled again and the supply current drawn from the HV pin charges the hold-up capacitor. When V_{DD} reaches the turn-on voltage of 16 V, normal operation resumes. In this manner, the auto-restart alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated *(see Figure 29).*

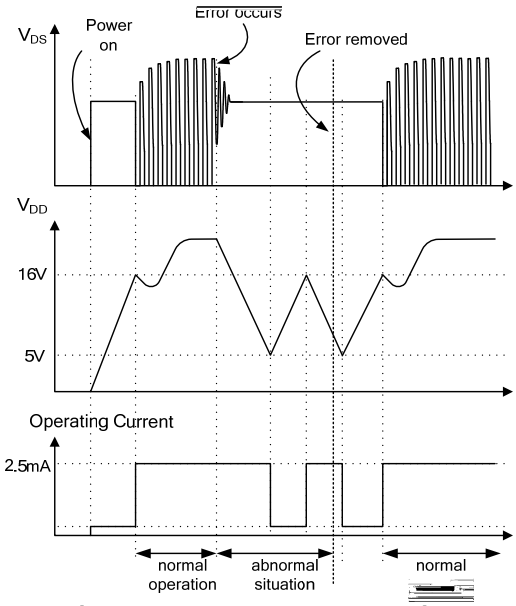


Figure 29. Auto-Restart Operation

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents damage from over-voltage conditions. If the V_{DD} voltage exceeds 24V at open-loop feedback condition, OVP is triggered and the PWM switching is disabled. The OVP has a debounce time (typically 200 µs) to prevent false triggering due to switching noises.

Over-Temperature Protection (OTP)

The built-in temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 140°C.

Pulse-by-pulse Current Limit

When the sensing voltage across the current-sense resistor exceeds the internal threshold of 0.8 V, the MOSFET is turned off for the remainder of switching cycle. In normal operation, the pulse-by-pulse current limit is not triggered since the peak current is limited by the control loop.

Leading-Edge Blanking (LEB)

Each time the power MOSFET switches on, a turn-on spike occurs at the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver. As a result conventional RC filtering can be omitted.

Gate Output

The FSEZ1317WA output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 15 V Zener diode to protect the power MOSFET transistors against undesired over-voltage gate signals.

Built-In Slope Compensation

The sensed voltage across the current-sense resistor is used for current mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillations due to peak-current mode control. The FSEZ1317WA has a synchronized, positive-slope ramp built-in at each switching cycle.

Noise Immunity

Noise from the current sense or the control signal can cause significant pulsewidth jitter, particularly in continuous-conduction mode. While slope compensation helps alleviate thei6 from tTc44 -13.405 .3 -14.28 cen

Typical Application Circuit (Primary-Side Regulated Flyback Charger)

Application	Fairchild Devices	Input Voltage Range	Output	Output DC cable
Cell Phone Charger	FSEZ1317WA	90~265 V_{AC}	5V/0.7 A (3.5 W)	AWG26, 1.8 Meter

Features

- High efficiency (>65.5% at full load) meeting EPS 2.0 regulation with enough margin.
- Low standby (Pin<30 mW at no-load condition).

$230V_{AC}$ 60Hz(

(%)

Typical Application Circuit (Continued)

Transformer Specification

- Core: EE16
- Bobbin: EE16

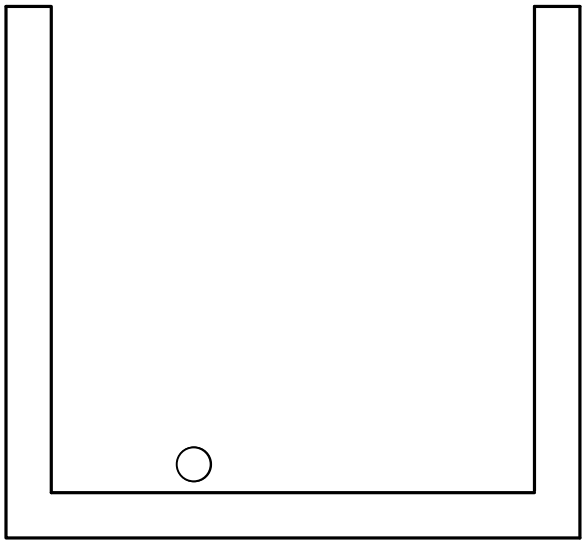
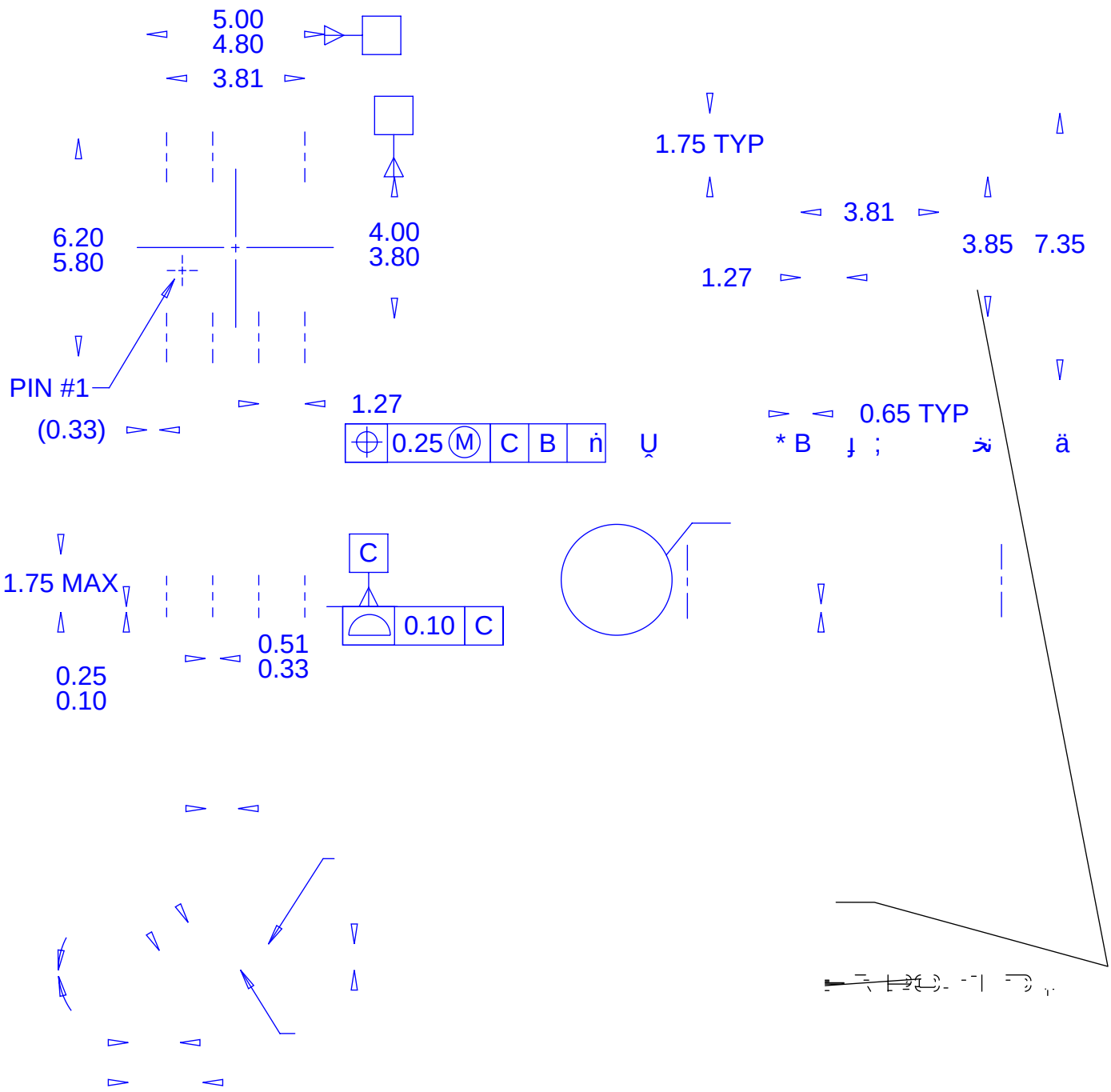


Figure 33. Transformer Specification

Notes:
7. When W4R's winding is reversed winding, it must wind one layer.
8. When W2 is winding, it must wind three layers and put one layer of tape after winding the first layer.

No.	Terminal		Wire	t_s	Insulation	Barrier Tape	
	S	F			t_s	Primary	Seconds
W1	4	5	2UEW 0.23*2	15	2		
W2	3	1	2UEW 0.17*1	41	1		
				39	0		
				37	2		
W3	1	-	COPPER SHIELD	1.2	3		
W4	7	9	TEX-E 0.55*1	9	3		
			CORE ROUNDING TAPE		3		

	Pin	Specification	Remark
Primary-Side Inductance	1ف3	2.25 mH ± 7%	100 kHz, 1 V
Primary-Side Effective Leakage	1ف3	80 µH ± 5%	Short One of the Secondary Windings


5.00
4.80
3.81
6.20
5.80
4.00
3.80
PIN #1
(0.33)
1.27
0.25 M C B
1.75 TYP
3.81
3.85
7.35
1.27
0.65 TYP
* B
1.75 MAX
C
0.10 C
0.51
0.33
0.25
0.10