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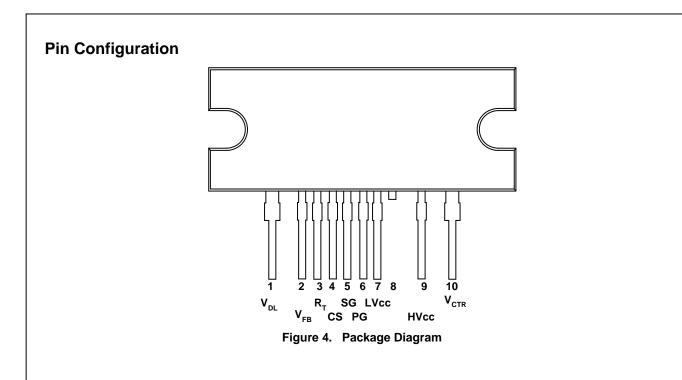
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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild questions@onsemi.com.

February 2013

Application Circuit Diagram





Pin Definitions

Pin #	Name	Description
1	V _{DL}	This is the drain of the high-side MOSFET, typically connected to the input DC link voltage.
2	V _{FB}	This pin is connected to the inverting input of the PWM comparator internally and to the opto- coupler externally. The duty cycle is determined by the voltage on this pin.
3	R _T	

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}C$ unless otherwise specified.

Symbol	Parameter		Min.	Max.	Unit
V _{DS}	Maximum Drain-to-Source Voltage (V _{DL} -	V _{CTR} and V _{CTR-PG})	600		V
LV _{CC}	Low-Side Supply Voltage		-0.3	25.0	V
HV _{CC} to V _{CTR}	High-Side V _{CC} Pin to Low-Side Drain Vo	Itage	-0.3	25.0	V
HV _{cc}	High-Side Floating Supply Voltage	-0.3	625.0	V	
V_{FB}	Feedback Pin Input Voltage	-0.3	LV _{CC}	V	
V _{CS}	Current Sense (CS) Pin Input Voltage	-5.0	1.0	V	
V_{RT}	R_T Pin Input Voltage	-0.3	5.0	V	
dV _{CTR} /dt	Allowable Low-Side MOSFET Drain Voltage Slew Rate			50	V/ns
PD	Total Power Dissipation ⁽³⁾			12.0	W
TJ	Maximum Junction Temperature ⁽⁴⁾			+150	
	Recommended Operating Junction Tem	-40	+130	°C	
T _{STG}	Storage Temperature Range		-55	+150	°C
IOSFET Sec	ction		·		-
V_{DGR}	Drain Gate Voltage (R _{GS} =1MΩ)		600		V
V_{GS}	Gate Source (GND) Voltage			±30	V
I _{DM}	Drain Current Pulsed			33	А
Ι _D	Orationana Daria Oranat	T _C =25°C		11	٨
	Continuous Drain Current	T _C =100°C		7	A
Package Sec	tion	•	·	•	•
Torque	Recommended Screw Torque		5	~7	kgf∙cm

Notes:

3. Per MOSFET when both MOSFETs are conducting.

4. The maximum value of the recommended operating junction temperature is limited by thermal shutdown.

Thermal Impedance

 $T_A{=}25^\circ C$ unless otherwise specified.

Symbol	Parameter	Value	Unit
JC	Junction-to-Case Center Thermal Impedance (Both MOSFETs Conducting)	10.44	°C/W
JA	Junction-to-Ambient Thermal Impedance	80	°C/W

₄=25°C and	LV_{CC} =17 V unless otherwise specified.					
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
IOSFET Se	ection	•	·			
BV_{DSS}	Drain-to-Source Breakdown Voltage	I _D =200 μA, T _A =25°C	600			v
		I _D =200 μA, T _A =125°C		650		
R _{DS(ON)}	On-State Resistance	V _{GS} =10 V, I _D =5.5 A		0.32	0.38	Ω
t _{rr}	Body Diode Reverse Recovery Time ⁽⁵⁾	V _{GS} =0 V, I _{Diode} =11.0 A, dI _{Diode} /dt=100 A/µs		120		ns
C _{ISS}	Input Capacitance ⁽⁵⁾	V _{DS} =25 V, V _{GS} =0 V, f=1.0 MHz	•	1148		pF

Electrical Characteristics (Continued)

 $T_A{=}25^\circ C$ and $LV_{CC}{=}17$ V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Protectio	n Section			•	•	
I _{OLP}	OLP Delay Current	V _{FB} =5 V	3.8	5.0	6.2	μA
V _{OLP}	OLP Protection Voltage	V _{FB} > 6 V	6.3	7.0	7.7	V
V _{OVP}	LV _{cc} Over-Voltage Protection	LV _{CC} > 21 V	21	23	25	V
V _{AOCP}	AOCP Threshold Voltage	ΔV/Δt=-1 V/µs	-1.0	-0.9	-0.8	V
t _{BAO}	AOCP Blanking Time ⁽⁵⁾	$V_{CS} < V_{AOCP};$ $\Delta V/\Delta t$ =-1 V/µs		50		ns
t _{DA}	Delay Time (Low-Side) from V_{AOCP} to Switch Off ⁽⁵⁾	∆V/∆t=-1 V/µs		250	400	ns
V_{LIM}	Pulse-by-Pulse Current Limit Threshold Voltage	ΔV/Δt=-0.1 V/μs	-0.64	-0.58	-0.52	V
t _{BL}	Pulse-by-Pulse Current Limit Blanking Time	$V_{CS} < V_{LIM};$ $\Delta V/\Delta t$ =-0.1 V/µs		150		ns
t _{DL}	Delay Time (Low-Side) from V_{LIM} to Switch Off ⁽⁵⁾	ΔV/Δt=-0.1 V/μs		450		ns
T _{SD}	Thermal Shutdown Temperature ⁽⁵⁾		110	130	150	°C
I _{SU}	Protection Latch Sustain LV _{CC} Supply Current	LV _{CC} =7.5 V		100	150	μA
V _{PRSET}	Protection Latch Reset LV _{CC} Supply Voltage		5			V
Dead-Tim	e Control Section	· · ·		•	•	
D _T	Dead Time ⁽⁶⁾			200		ns

Notes:

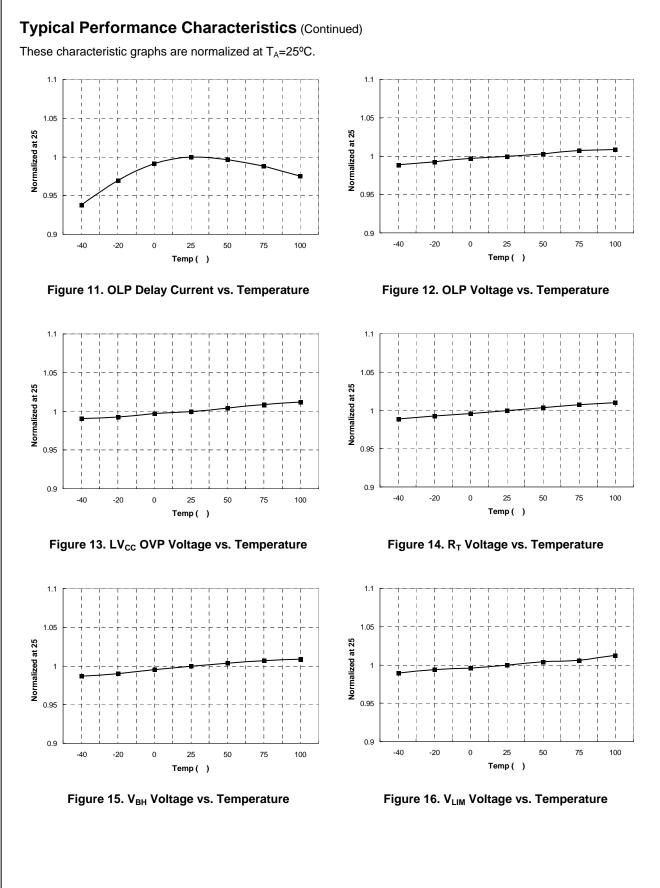
5. This parameter, although guaranteed, is not tested in production.

6. These parameters, although guaranteed, are tested only in EDS (wafer test) process.

Typical Performance Characteristics

These characteristic graphs are normalized at $T_A=25^{\circ}C$.

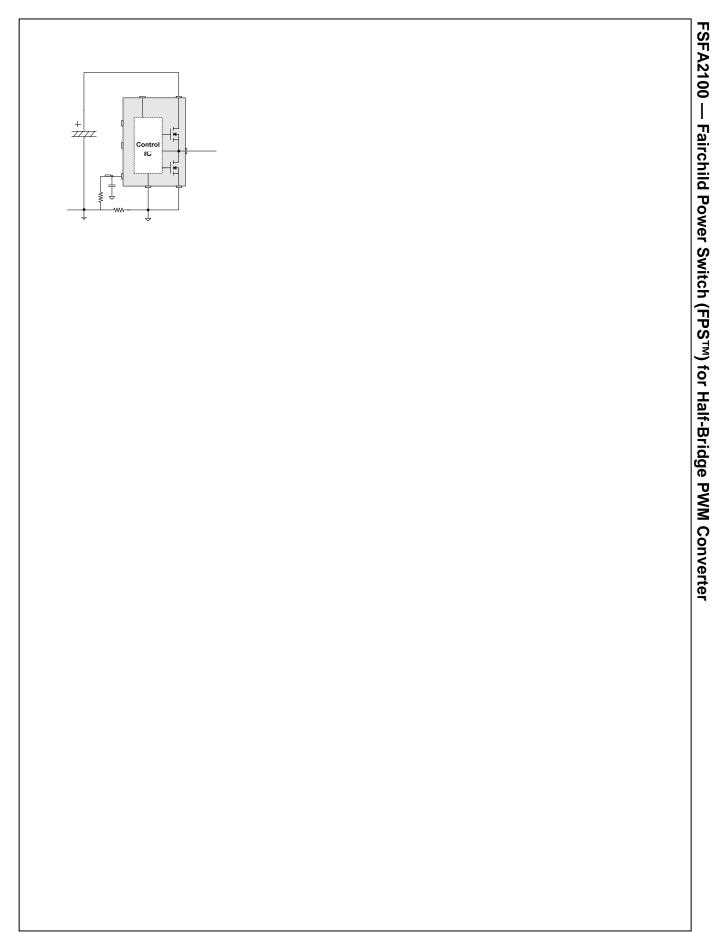
© 2008 Fairchild Semiconductor Corporation FSFA2100 • Rev. 1.0.1



FSFA2100 — Fairchild Power Switch (FPS[™]) for Half-Bridge PWM Converter

Functional Description

1. Internal Oscillator: FSFA2100 employs a current-



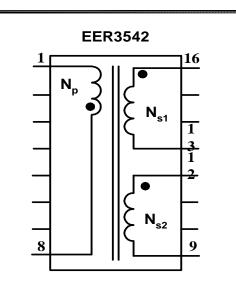
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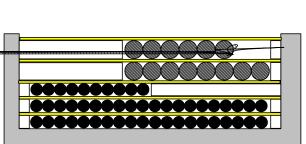
Typical Application Circuit (Asymmetric PWM Half-Bridge Converter)							
Application	FPS™ Device	Input Voltage Range	Rated Output Power	Output Voltage (Rated Current)			
LCD TV	FSFA2100	400 V	200 W	25 V-8 A			

Features

Typical Application Circuit (Continued)

Core: EER3542 (Ae=107 mm²) Bobbin: EER3542 (Horizontal)





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