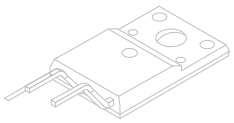
FSGM0465R

Green-Mode Power Switch

Description

The FSGM0465R is an integrated Pulse Width Modulation (PWM) controller and SENSEFET® specifically designed for offline Switch−Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed−frequency oscillator, Under−Voltage Lockout (UVLO), Leading−Edge Blanking (LEB), optimized gate driver, internal soft−start, temperature−compensated precise current sources for loop compensation, and self−protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSGM series can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform suited for cost−effective design of a flyback converter.



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GM0465R

Features

- Soft Burst−Mode Operation for Low Standby Power Consumption and Low Noise
- Precision Fixed Operating Frequency: 66 kHz
- Pulse−by−Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over−Voltage Protection (OVP), Abnormal Over−Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis, Output−Short Protection (OSP), and Under−Voltage Lockout (UVLO) with Hysteresis
- Auto−Restart Mode
- Internal Startup Circuit
- Internal High−Voltage SENSEFET: 650 V
- Built−in Soft−Start: 15 ms
- These are Pb−Free Devices

Applications

- Power Supply for LCD TV and Monitor, STB and DVD Combination

Related Resources

- *Power Supply WebDesigner — Flyback Design &ources*

ORDERING INFORMATION

Part Number	Package	Operating Junction Temperature	Current Limit	$R_{DS(ON)}$ (Max.)	Output Power Table (Note 2)				Replaces Device	Shipping
					230V_{AC} ± 15% (Note 3)		85 − 265 V_{AC}			
					Adapter (Note 4)	Open Frame (Note 5)	Adapter (Note 4)	Open Frame (Note 5)		
FSGM0465RWDTU	TO−220F 6−Lead (Note 1) W−Forming	−								

Internal Block Diagram

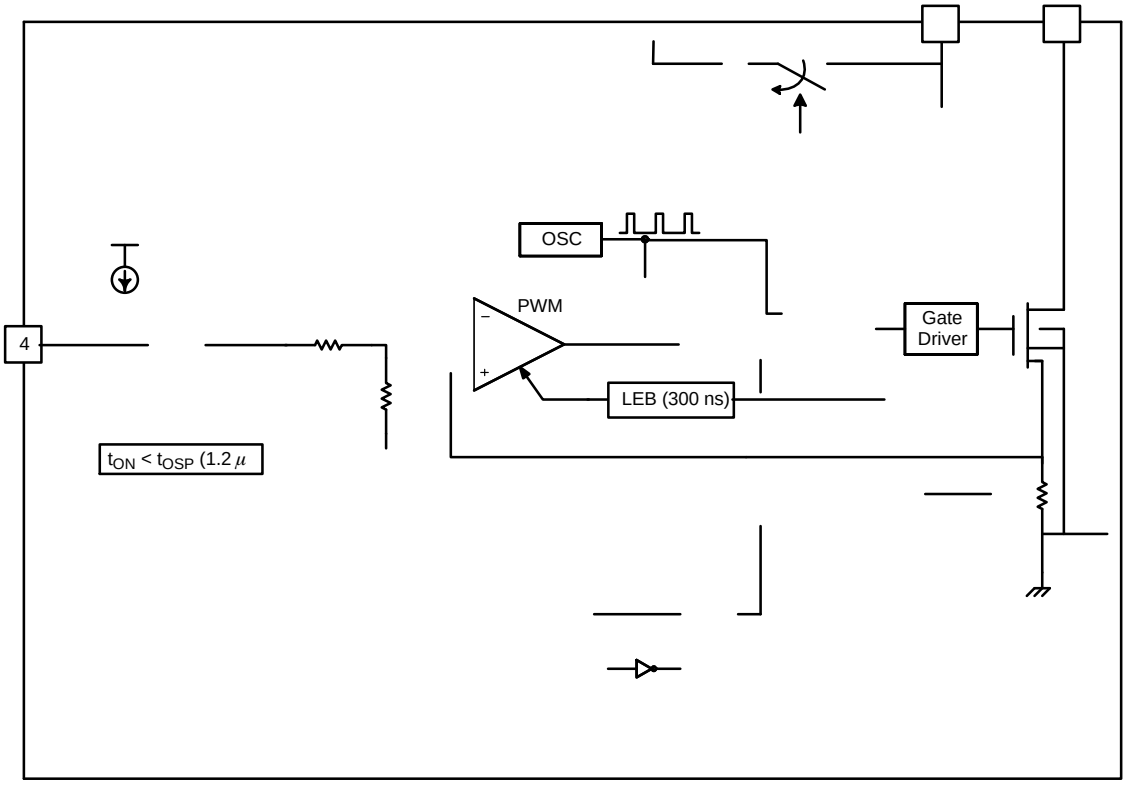

Figure 2. Internal Block Diagram

PIN DEFINITIONS

Pin No.	Name	Description
1	Drain	. High−voltage power SENSEFET drain connection.
2	GND	. This pin is the control ground and the SENSEFET source.
3	V_{CC}	. This pin is the positive supply input, which provides the internal operating current for both startup and steady−state operation.
4	FB	. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto−coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6 V, the overload protection triggers, which shuts down the power switch.
5	N.C.	No connection.
6	V_{STR}	. This pin is connected directly, or through a resistor, to the high−voltage DC link. At startup, the internal high−voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 12 V, the internal current source (I_{CH}) is disabled.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{STR}	V_{STR} Pin Voltage	−	650	

THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Unit
θ_{JA}	Junction−to−Ambient Thermal Impedance (Note 11)	62.5	°C/W
θ_{JC}	Junction−to−Case Thermal Impedance (Note 12)	3	°C/W

11. Infinite cooling condition − .
12. Free standing with no heat−sink under natural convection.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SENSEFET SECTION						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{CC} = 0 V, I_D = 250 μA	650	−	−	V
I_{DSS}	Zero−Gate−Voltage Drain Current	V_{DS} = 520 V, T_A = 125°C	−	−	250	μA
$R_{DS(ON)}$	Drain−Source On−State Resistance	V_{GS} = 10 V, I_D = 1 A	−	2.1	2.6	Ω
C_{ISS}	Input Capacitance (Note 13)	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz	−	436	−	pF
C_{OSS}	Output Capacitance (Note 13)	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz	−	65	−	pF
t_r	Rise Time	V_{DS} = 325 V, I_D = 4 A, R				

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
PROTECTION SECTION							
t_{OSP}	Output Short Protection (Note 13)	Threshold Time	OSP Triggered when $t_{ON} < t_{OSP}$ & $V_{FB} > V_{OSP}$ (Lasts Longer than t_{OSP_FB})	1.0	1.2	1.4	μs
V_{OSP}		Threshold V_{FB}		1.8	2.0	2.2	V
t_{OSP_FB}		V_{FB} Blanking Time		2.0	2.5	3.0	μs
T_{SD}	Thermal Shutdown Temperature (Note 13)		Shutdown Temperature	130	140	150	°C

TYPICAL CHARACTERISTICS (T_A = 25°

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FUNCTIONAL DESCRIPTION

Startup

At startup, an internal high−voltage current source supplies the internal bias and charges the external capacitor

Protection Circuits

The FSGM0465R has several self−protective functions, such as Overload Protection (OLP), Abnormal Over−Current Protection (AOCP), Output−Short Protection (OSP), Over−Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto−restart. Once the fault condition is detected, switching is terminated and the SENSEFET remains off. This causes V_{CC} to fall. When V_{CC} falls to the Under−Voltage Lockout (UVLO) stop voltage of 7.5 V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 12.0 V, the FSGM0465R resumes normal operation. If the fault condition is not removed, the SENSEFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto−restart can alternately enable and disable the switching of the power SENSEFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.

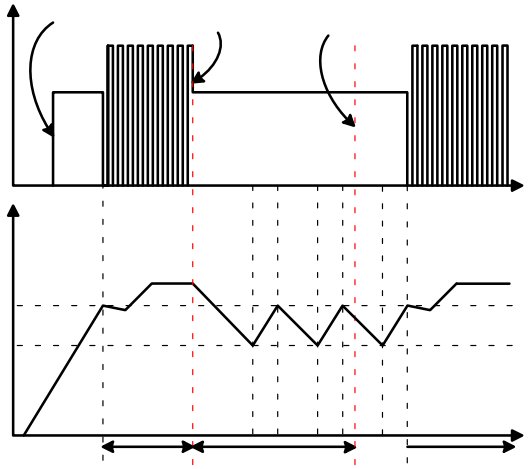


Figure 19. Auto−Restart Protection Waveforms

Overload Protection (OLP)

Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse−by−pulse current limit capability, the maximum peak current through the SENSEFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_{OUT}) decreases below the set voltage. This reduces the current through the opto−coupler LED, which also reduces the opto−coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.4 V, D1 is blocked and the 3.3 μA current source starts to charge C_{FB} slowly up. In this condition, V_{FB} continues increasing until it reaches 6.0 V, when the switching operation is terminated, as shown in Figure 20. The delay time for shutdown is the time required to charge C_{FB} from 2.4 V to 6.0 V with 3.3 μA. A 25 ~ 50 ms delay is typical for most applications. This protection is implemented in auto−restart mode.

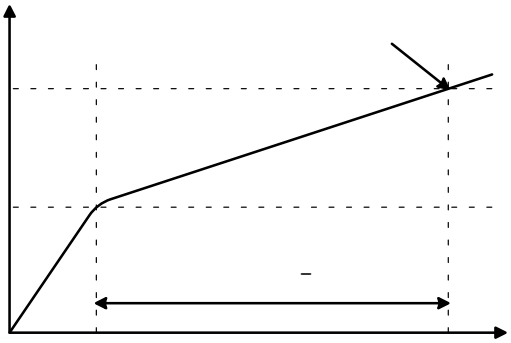


Figure 20. Overload Protection

Abnormal Over−Current Protection (AOCP)

When the secondary rectifier diodes or the transformer pins are short1ml2.891 1.417 2.041 2.4.2 4893.823. This protectioarCext

Output−Short Protection (OSP)

If the output is shorted, steep current with extremely high di/dt can flow through the SENSEFET during the minimum turn−on time. Such a steep current brings high−voltage stress on the drain of the SENSEFET when turned off. To protect the device from this abnormal condition, OSP is included. It is comprised of detecting V_{FB} and SENSEFET turn−on time. When the V_{FB} is higher than 2 V and the SENSEFET turn−on time is lower than 1.2 μs, the FSGM0465R recognizes this condition as an abnormal error and shuts down PWM switching until V_{CC} reaches V_{START} again. An abnormal condition output short is shown in Figure 22.

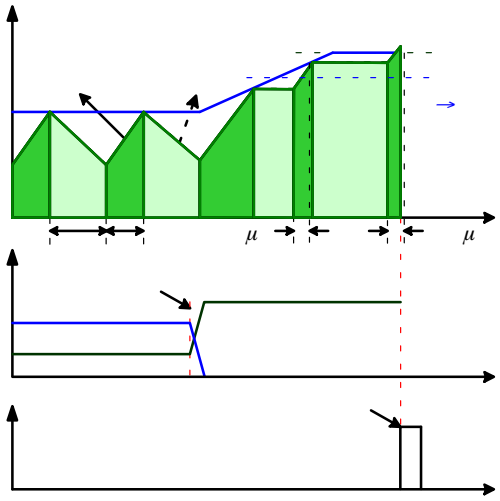


Figure 22. Output−Short Protection

Over−Voltage Protection (OVP)

If the secondary−side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto−coupler transistor becomes almost zero. Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the V_{CC} is proportional to the output voltage and the FSGM0465R uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 24.5 V, an OVP circuit is triggered, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 24.5 V.

Thermal Shutdown (TSD)

The SENSEFET and the control IC on a die in one package makes it easier for the control IC to detect the over temperature of the SENSEFET. If the temperature exceeds ~140°C, the thermal shutdown is triggered and the FSGM0465R stops operation. The FSGM0465R operates in auto−restart mode until the temperature decreases to around 110°C, when normal operation resumes.

Soft Burst−Mode Operation

To minimize power dissipation in standby mode, the FSGM0465R enters burst−mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 23, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (500 mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (700 mV), switching resumes. At this point, the drain current peak increases gradually. This soft burst−mode can reduce audible noise during burst−mode operation. The feedback voltage then falls and the process repeats. Burst−mode operation alternately enables and disables switching of the SENSEFET, thereby reducing switching loss in standby mode.

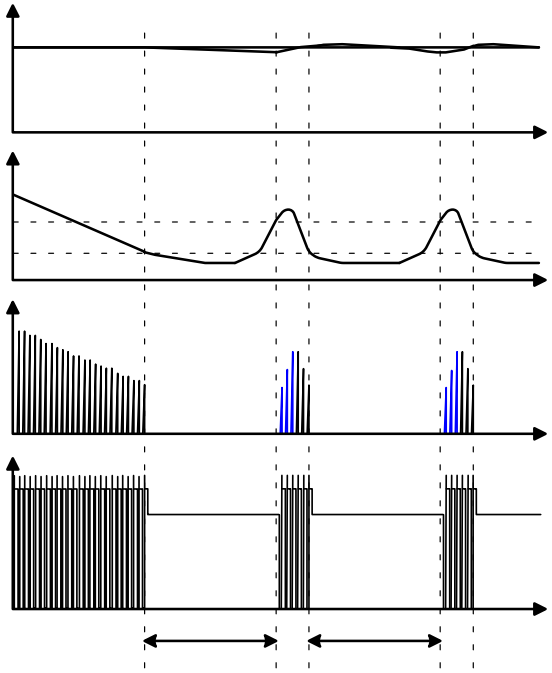


Figure 23. Burst−Mode Operation

TYPICAL APPLICATION CIRCUIT

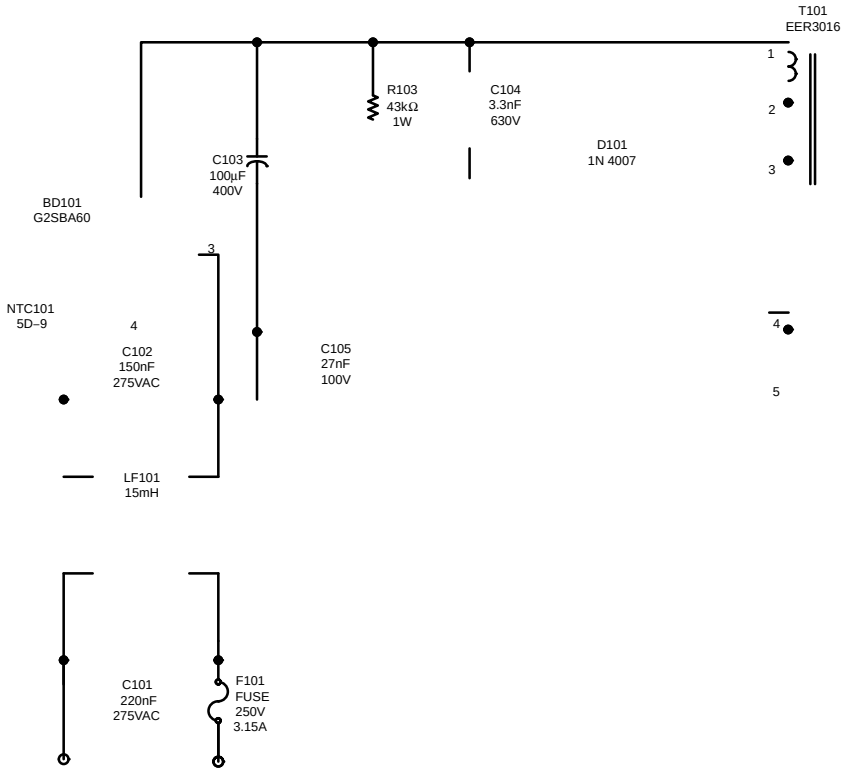
Table 2. TYPICAL APPLICATION CIRCUIT

Application	Input Voltage	Rated Output	Rated Power
LCD TV, Monitor Power Supply	85 ~ 265 V_{AC}	5.0 V (2 A) 14.0 V (2.4 A)	43.6 W

Key Design Notes:

1. The delay time for overload protection is designed to be about 30 ms with C105 (27 nF). OLP time between 25 ms (22 nF) and 50 ms (43 nF) is recommended.
2. The SMD−type capacitor (C106) must be placed as close as possible to the V_{CC} pin to avoid malfunction by abrupt pulsating noises and to improve ESD and surge immunity. Capacitance between 100 nF and 220 nF is recommended.

Schematic



Winding Specification

Table 3. WINDING SPECIFICATION

	Pin (S □ F)	Wire	Turns

Bill of Materials

Table 5. Bill of Materials

Part #	Value	Note
Fuse		
F101	250 V 3.15 A	
NTC		
NTC101	5D−9	DSC
Resistor		
R101	1.5 MΩ, J	1 W
R102	75 kΩ, J	1/2 W
R103	43 kΩ, J	1 W
R104	62 Ω, J	1/2 W
R201	330 Ω, F	1/4 W, 1%
R202	1.2 kΩ, F	1/4 W, 1%
R203	18 kΩ, F	1/4 W, 1%
R204	8 kΩ, F	1/4 W, 1%
R205	8 kΩ, F	1/4 W, 1%
IC		
FSGM0465R	FSGM0465R	ON Semiconductor
IC201	KA431LZ	ON Semiconductor
IC301	FOD817B	ON Semiconductor
Diode		
D101	1N4007	Vishay
D102	UF4004	Vishay
ZD101	1N4749	Vishay
D201	MBR20150CT	ON Semiconductor
D202	FYPF2006DN	ON Semiconductor
BD101	G2SBA60	Vishay
Capacitor		
C101	220 nF / 275 V	Box (Pilkor)
C102	150 nF / 275 V	Box (Pilkor)
C103	100 μF / 400 V	Electrolytic (SamYoung)
C104	3.3 nF / 630 V	Film (Sehwa)
C105	27 nF / 100 V	Film (Sehwa)
C106	220 nF	SMD (2012)
C107	47 μF / 50 V	Electrolytic (SamYoung)
C201	1000 μF / 25 V	Electrolytic (SamYoung)
C202	1000 μF / 25 V	Electrolytic (SamYoung)
C203	2200 μF / 10 V	Electrolytic (SamYoung)
C204	1000 μF / 16 V	Electrolytic (SamYoung)
C205	47 nF / 100 V	Film (Sehwa)
C206	100 nF	SMD (2012)
C207	100 nF	SMD (2012)
C301	4.7 nF / Y2	Y−cap (Samhwa)
Inductor		
LF101	15 mH	

TO−220−6LD LF
CASE 340BG
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