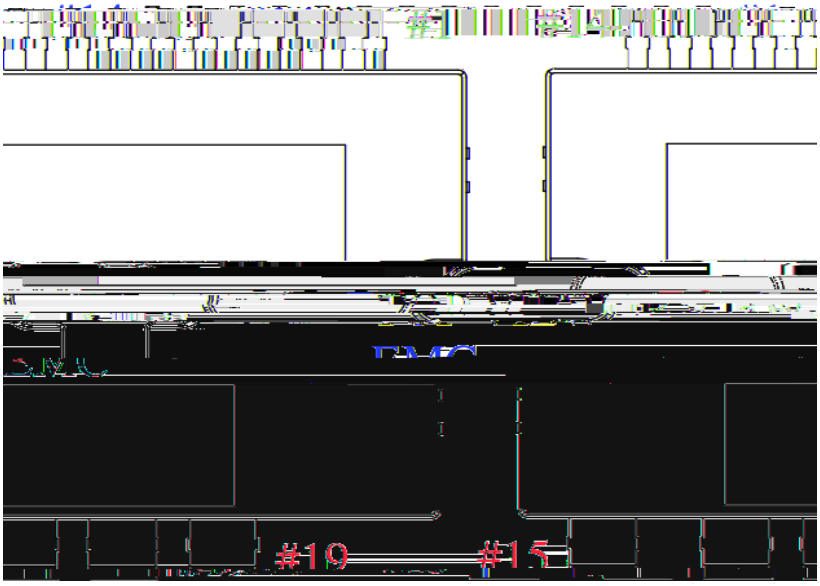


Figure 1. Pin Configuration

Table 1. PIN DESC

Pin No.	Pin Number	Pin Description
1	TEMP 1	NTC Thermistor Terminal 1
2	TEMP 2	NTC Thermistor Terminal 2
3	PHASE 3 SENSE	Source of Q3 and Drain of Q6
4	GATE 3	Gate of Q3, high side Phase 3 MOSFET
5	GATE 6	Gate of Q6, low side Phase 3 MOSFET
6	PHASE 2 SENSE	Source of Q2 and Drain of Q5
7	GATE 2	Gate of Q2, high side Phase 2 MOSFET
8	GATE 5	Gate of Q5, low side Phase 2 MOSFET
9	PHASE 1 SENSE	Source of Q1 and Drain of Q4
10	GATE 1	Gate of Q1, high side Phase 1 MOSFET
11	VBAT SENSE	Sense pin for battery voltage and Drain of high side MOSFETs
12	GATE 4	Gate of Q4, low side Phase 1 MOSFET
13	SHUNT P	Positive CSR sense pin and source connection for low side MOSFETs
14	SHUNT N	Negative CSR sense pin and sense pin for battery return
15	VBAT	Battery voltage power lead
16	GND	Battery return power lead
17	PHASE 1	Phase 1 power lead
18	PHASE 2	Phase 2 power lead
19	PHASE 3	Phase 3 power lead

Figure 2. Internal Equivalent Circuit

Flammability Information

All materials present in the power module meet UL flammability rating class 94V−0 or higher.

Solder

Solder used is a lead free SnAgCu alloy.

Compliance to RoHS

The Power Module is 100% lead free and RoHS compliant with the 2000/53/C directive.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter	FTCO3V85A1	Unit
V_{DS}(Q1~Q6)	Drain to Source Voltage	80	V
V_{GS}(Q1~Q6)	Gate to Source Voltage	±20	V
I_D(high side)	Drain Current Continuous (T_C = 25°C, T_J = 175°C, V_{GS} = 10 V) (Note 1)	125	A
I_D(low side)	Drain Current Continuous (T_C = 25°C, T_J = 175°C, V_{GS} = 10 V) (Note 1)	160	A
E_{AS}(Q1~Q3)	Single Pulse Avalanche Energy (Note 2)	190	mJ
E_{AS}(Q4~Q6)	Single Pulse Avalanche Energy (Note 2)	324	mJ
P_D(high side)	Power dissipation (T_C = 25°C, T_J = 175°C)	115	W
P_D(low side)	Power dissipation (T_C = 25°C, T_J = 175°C)	135	W
T_J	Maximum Junction Temperature	175	°C
T_{STG}	Storage Temperature	125	°C

THERMAL RESISTANCE

Symbol	Parameter	Min.	Typ.	Max.	Unit
Rthjc Thermal Resistance Junction to case, Single FET, (Note 3)	Q1 Thermal Resistance J C		1.0	1.3	°C/W
	Q2 Thermal Resistance J C		1.0	1.3	°C/W
	Q3 Thermal Resistance J C		1.0	1.3	°C/W
	Q4 Thermal Resistance J C		0.8	1.1	°C/W
	Q5 Thermal Resistance J C		0.8	1.1	°C/W
	Q6 Thermal Resistance J C		0.8	1.1	°C/W
T_J	Maximum Junction Temperature			175	°C
T_S	Operating Sink Temperature	40		120	°C
T_{STG}	Storage Temperature	40		125	°C

1. Max value not to exceed Tj=175°C based on max limitation of Rthjc thermal limitation and Rdson. Defined by design, not subject production testing.
2. Defined by design, not subject to production

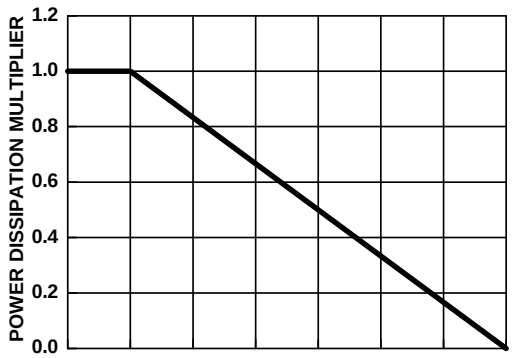
s	Min.	Typ.	Max.	Unit
μA	80			V
tage	20		20	V
T_J = 25°C	2	3	4	V
= 25°C			1	V

DYNAMIC CHARACTERISTIC

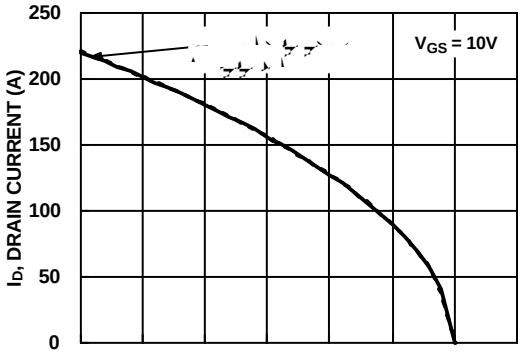
Symbol	Parameter	Min	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input Capacitance		V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MH_Z for Q1				

TYPICAL CHARACTERISTICS

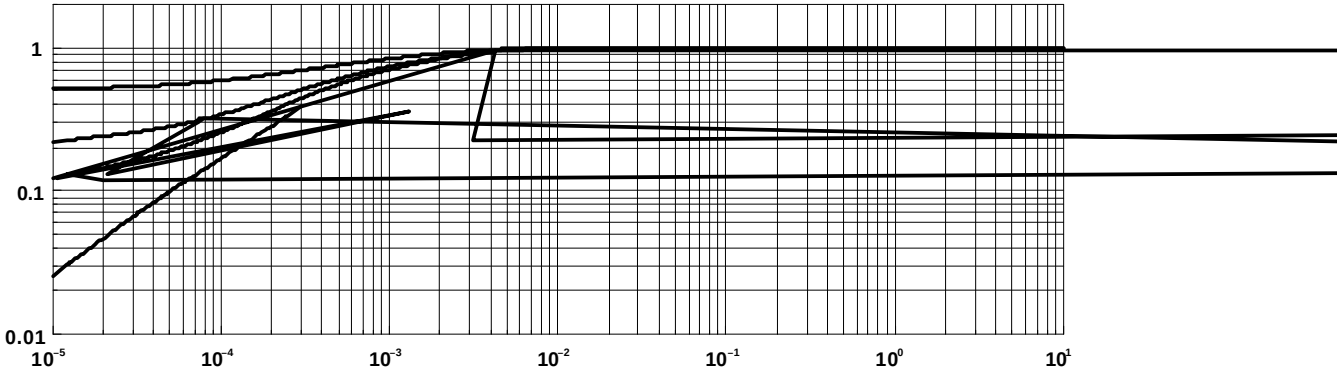
(The dynamic, switching characteristics and Graphs are in reference to the FDBL86366_F085 (TOLL) Datasheet (High side MOSFET)



T_C, CASE TEMPERATURE(°C)

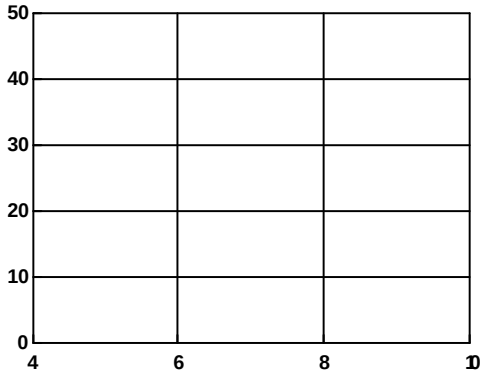


T_C, CASE TEMPERATURE(°C)



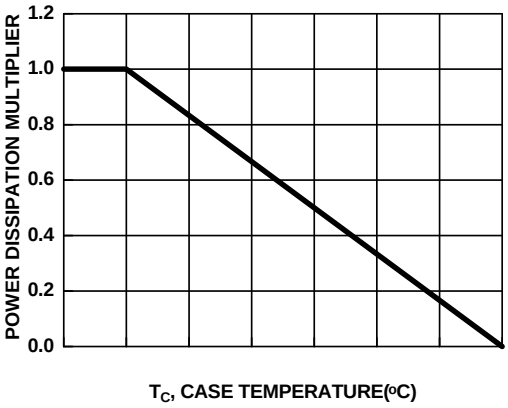
TYPICAL CHARACTERISTICS

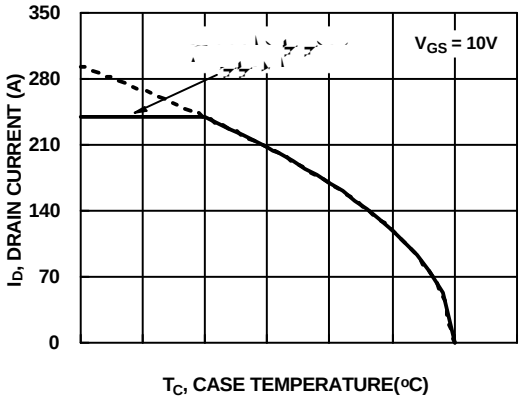
(The dynamic, switching characteristics and Graphs are in reference to the FDBL86366_F085 (TOLL) Datasheet (High side MOSFET)
(Continued)

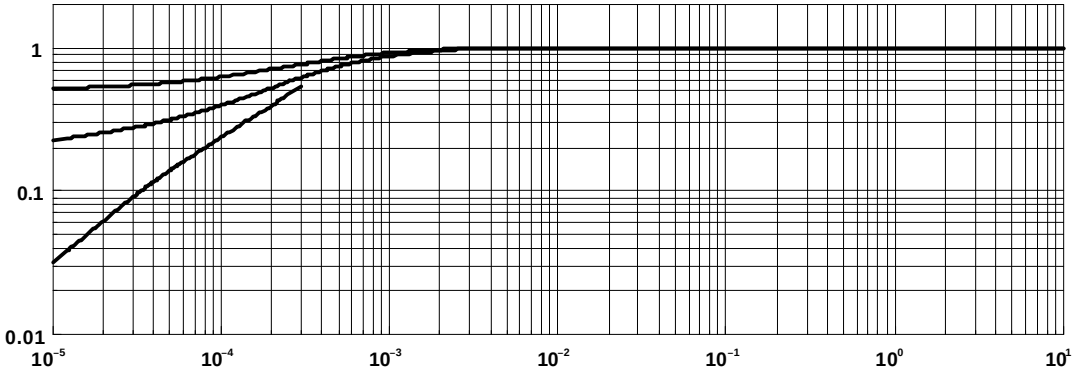


TYPICAL CHARACTERISTICS

(The dynamic, switching characteristics and Graphs are in reference to the FDBL86363_F085 (TOLL) Datasheet (Low side MOSFET)
(Continued)

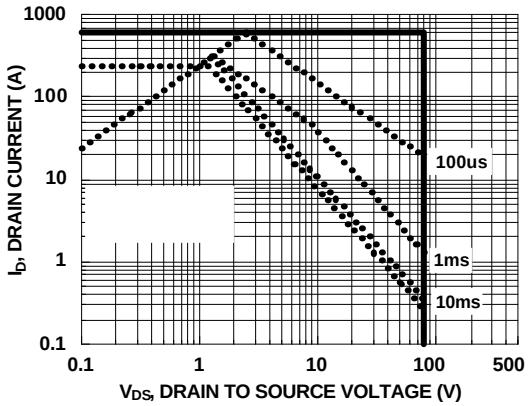






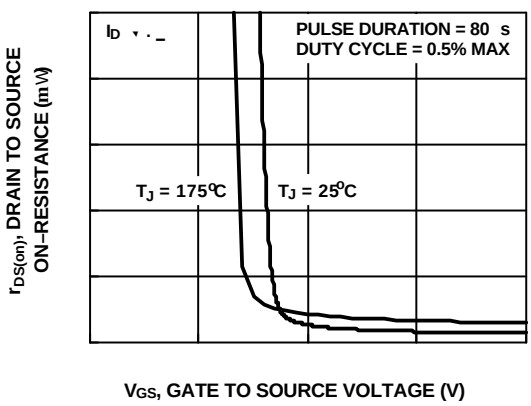
TYPICAL CHARACTERISTICS

(The dynamic, switching characteristics and Graphs are in reference to the FDBL86363_F085 (TOLL) Datasheet (Low side MOSFET)
(Continued)



TYPICAL PERFORMANCE CHARACTERISTICS

(The dynamic, switching characteristics and Graphs are in reference to the FDBL86363_F085 (TOLL) Datasheet (Low side MOSFET)
(Continued)



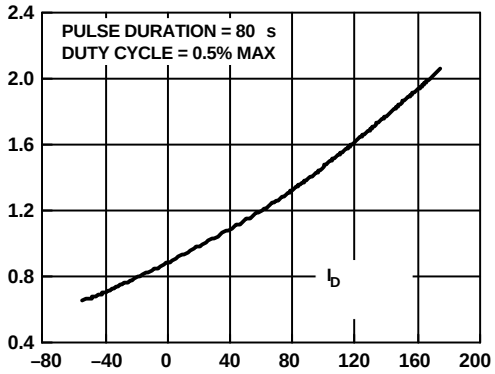


Table 2. MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Limits			Units
		Min.	Typ.	Max.	
Device Flatness	Note Fig. 15	0			

19LD, APM, PDD STD (APM19−CBC)

7.113 39[w 12624(221.4432.-6-20c589.45AN57Ty721.-.062.113 321M69AM72AW-5-87436207587)51977621[w .519776207c58519776211[w .5194362-

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba “**onsemi**” or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**’s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided “as−is” and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**