Programmable USB Type-C® and Power Delivery 3.1 Source Controller with PPS Support

FUSB15101SupThe B15101PD)0 --6810559.0018TD(c4.3w[So

PD, with a minimum of 3.3 V and a maximum of 21 V output volt

control. It includes Constant Voltage (CV) and Constant Current Limit (CL) control blocks, various protection mechanisms and high volt tolerance on connector pins.

Key Features

- 32−bit Arm Cortex−M0+ Processor
- 32 KB OTP (One Time Programmable) Program Memory
- USB PD 3.1 with PPS Support
  - Power Management Unit with VIN Support from 3.3 V to 24 V
  - Integrated VCONN Supply for Interrogating E−Marked Cables
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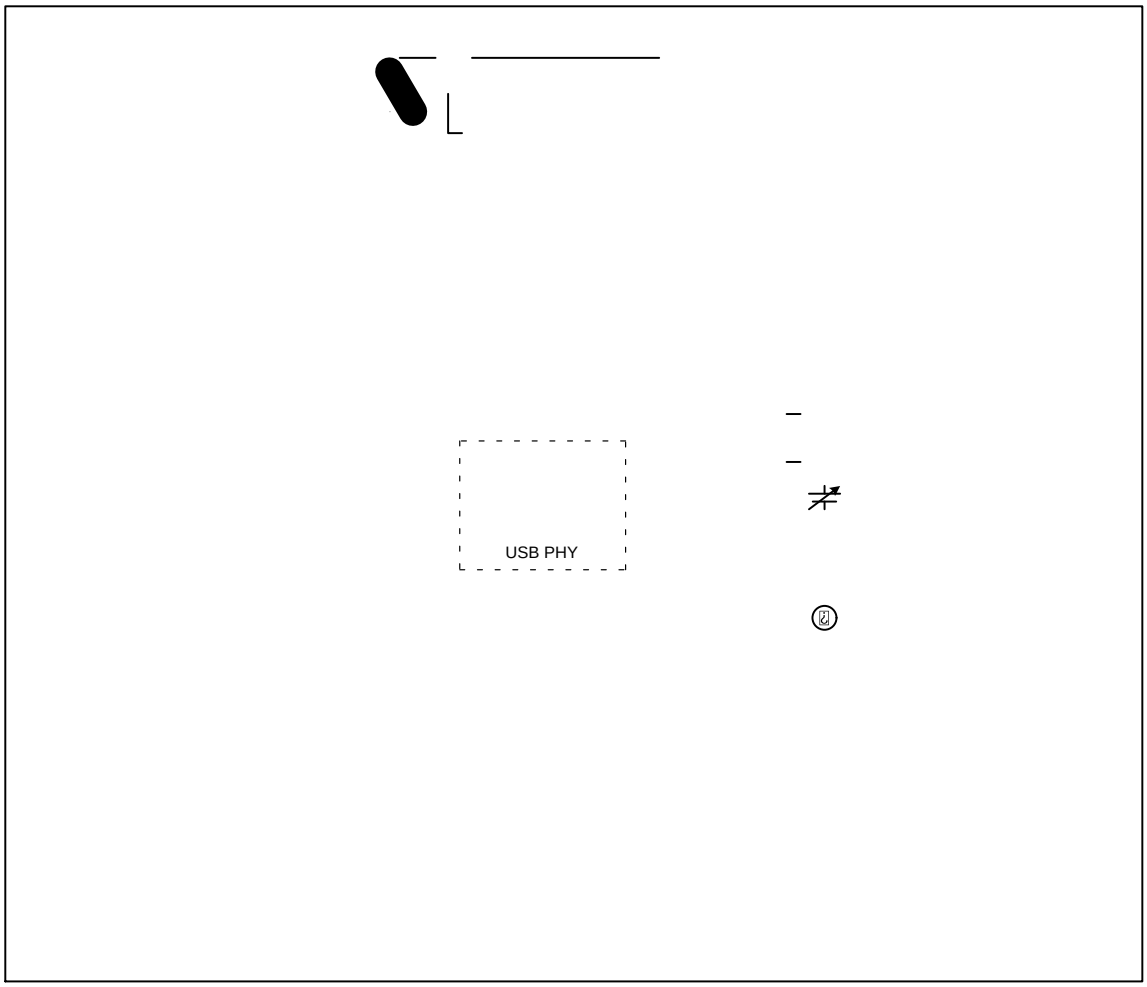
Introduction

The FUSB15101 supports USB Type−C 2.1 and USB PD 3.1 specifications for power source applications with VBUS voltages ranging from 3.3 V to 21 V.

A highly flexible and open firmware environment allows hardware peripherals to be customized to meet a variety application needs.

Key integrated functions and peripherals are highlighted below:

- *Arm Cortex−M0+*: A 32−bit core with flexible clocking up to 12 MHz.
- *Memories*: A total of 32 kB of One Time Programmable Memory (OTP) is available to store program code; 2 KB of SRAM program memory.
- *USB Type−C and PD*: Integrated USB PD PHY and Type−C termination/comparators supporting latest USB−IF specification. Open and customizable USB PD firmware stack allows for tailored vendor specific functions.
- *Integrated VCONN Switch*: Provides power to cable eMarkers to interrogate current capabilities.
- *CC/CV Control*: Firmware controlled feedback voltage and current loop operation with programmable voltage and current DACs, Cable Drop Compensation, OVP, UVP and OCP.
- *Current Sense Amplifier*: Programmable for use with 5 mΩ or 10 mΩ sense resistors.
- *High Voltage Protection*: 26 V DC tolerant BLD, CC and D+/−.
- *ADC*: 10−bit ADC for accurate monitoring of VBUS voltage and current, external temperatures or voltages.
- *I^2C*: Serial communication port capable of acting as a host or device.
- *UART*: UART peripheral available via HVDP/DM.
- *GPIOs*: Fully programmable I/Os with internal terminations. Configurable as input or output (CMOS or open−drain).
- *Multiple Timers*: Three independent 32−bit timers are available: 1 General Purpose, 1 Watchdog, and 1 Wake−up / General Purpose.
- *Dual External NTC*: Integrated current sources are used in conjunction with the ADC to monitor a variety of NTC resistors.
- *Low Power Operation Modes*: Programmable Sleep Modes allowing the device to minimize power usage as needed. Automatic USB−C detection and weak−up functionality from sleep modes.
- *Temperature Range*: Extended operating temperature range of −40°C to 105°C.


USB PHY

PIN CONNECTIONS

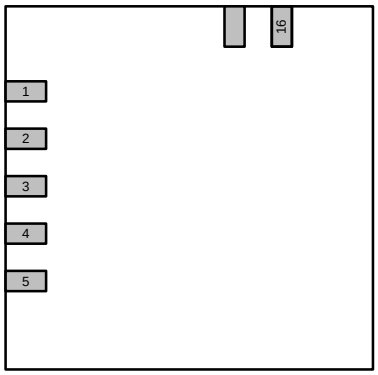


Figure 4. QFN20 Top−View

THERMAL CHARACTERISTICS (Note 3)

Symbol	Characteristic	Value	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance	38.6	°C/W
θ_{JC}	Junction−to−Case Thermal Resistance	4.2	°C/W

3. Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with two−layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature T_J(max) at a given ambient temperature T_A.

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INTERNAL POWER SUPPLY						
VIN						
$I_{IN-OP-5V}$	Operating Supply Current at 5 V	Attached, PD Communication in progress, ADCs enabled, NTCs enabled, CC & CV enabled, Gate Driver Enabled. VIN = 5 V, VCS = −25 mV, RCS = 5 mΩ	−	3.5	−	mA
$I_{IN-OP-20V}$	Operating Supply Current at 20 V	Attached, PD Communication in progress, ADCs enabled, NTCs enabled, CC & CV enabled, Gate Driver Enabled. VIN = 20 V, VCS = −25 mV, RCS = 5 mΩ	−	4.4	−	mA
$I_{IN-Sleep}$	Operating Supply Current at Sleep Mode	No Device Attached, Type−C enabled & Gate Driver OFF or BC1.2 Detection enabled & Gate Driver ON; VIN = 5 V, VCS = 0 V excluding IP−CC1 and IP−CC2 Supply Current and ISFB Current	−	−	0.75	mA
V_{IN-ON}						

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIN OVP SECTION						
$K_{IN-OVP-105}$	Ratio VIN Over−Voltage−Protection (OVP) to VIN	VCS = 0 mV	102	105	108	%
$K_{IN-OVP-110}$		VCS = 0 mV	107	110	113	
$K_{IN-OVP-115}$		VCS = 0 mV	112	115	118	
$K_{IN-OVP-120}$		VCS = 0 mV	117	120	123	
$K_{IN-OVP-125}$		VCS = 0 mV	122	125	128	
$K_{IN-OVP-130}$		VCS = 0 mV	127	130	133	
$K_{IN-OVP-135}$		VCS = 0 mV	132	135	138	
VDD						
V_{DD}	VDD Source Voltage > 6 V	VIN = 6 V to 22.5 V, IVDD = 10 mA	4.75	5.125	5.5	V
I_{DD}	VDD Source Current Capability	VIN = 3.3 V, VDD = 2.9 V	10	−	−	mA
TYPE−C AND PD						
USB PD PHY						
TRANSMITTER						
UI	Unit Interval		3.03	3.33	3.7	μs
$p_{BitRate}$	Maximum Difference between the bit−rate During the Payload and Last 32 Bits of Preamble		−	−	0.25	%
$t_{EndDriveBMC}$	Time to Cease Driving the Line after the End of the Last Bit of the Frame		−	−	23	μs
$t_{HoldLowBMC}$	Time to Cease Driving the Line after the Final High−to−low Transition		1	−	−	μs

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BC1.2						
R_{DCP}	DCP Emulation Resistance	V_{HVDP} or V_{HVDM} = 0 V, 1.0 V, ION = 2 mA	−	75	140	Ω
R_{Dx-DWN}						

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I/OS						
GPIO						
$V_{GPIO-VIH}$	High Level Input Voltage	VIN = 3.1 V to 22.5 V	0.7 x VDD	−	−	V
$V_{GPIO-IL}$	Low Level Input Voltage	VIN = 3.1 V to 22.5 V	−	−	0.3 x VDD	V
$V_{GPIO-VOH}$	Output High Voltage	VIN = 3.1 V to 22.5 V, Iout = −2 mA	VDD − 0.5	−	−	V
$V_{GPIO-VOL}$	Ouptut Low Voltage	VIN = 3.1 V to 22.5 V, Iout = +4 mA	−	−	0.4	V
$V_{GPIO-HYS}$	Input Hysteresis	VIN = 3.1 V to 22.5 V, 5.0 V Typ	−	300	−	mV
$I_{IN-GPIO}$	Input Leakage	VIN = 3.1 V to 22.5 V, Input Voltage 0 V to 5.5 V	−10	−	5	μA
$I_{OFF-GPIO}$	Off Input Leakage	VIN = 0 V, Input Voltage 0 V to 5.5 V	−5	−	5	μA
$R_{PD-GPIO}$	Pull−Down Resistance	PORT_PDx = 1	−	100	−	kΩ
$R_{PU-GPIO}$	Pull−Up Resistance	PORT_PUx = 1	−	100	−	kΩ
C_{GPIO}	Pin Capacitance					

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CONSTANT CURRENT SENSE SECTION						
I_{CS-2A}	Current Threshold on Sensing Resistor between CSP and CSN at IOUT = 2.00 A	Constant Current Limit mode and VCC = 5 V, 20 V	1.85	2.00	2.15	A
I_{CS-3A}	Current Threshold on Sensing Resistor between CSP and CSN at IOUT = 3.00 A	Constant Current Limit mode and VCC = 5 V, 20 V	2.85	3.00	3.15	A
I_{CS-4A}	Current Threshold on Sensing Resistor between CSP and CSN at IOUT = 4.00 A	Constant Current Limit mode and VCC = 5 V, 20 V	3.80	4.00	4.20	A
I_{CS-5A}	Current Threshold on Sensing Resistor between CSP and CSN at IOUT = 5.00 A	Constant Current Limit mode and VCC = 5 V, 20 V	4.75	5.00	5.25	A
$I_{CS-STEP}$	Current Threshold on Sensing Resistor between CSP and CSN at ΔIOUT = 50 mA	Constant Current Limit mode and VCC = 5 V	48	50	52	mA
$I_{CS-EN-BLD}$	Real Current Threshold to Enable Bleeder	VBUS_BLD_EN = 1	200	450	700	mA
$t_{CS-EN-BLD}$	Enable Bleeder Debounce Time	VBUS_BLD_EN = 1	−	0.6	1	ms
OVER CURRENT PROTECTION SENSING SECTION						
$V_{CS-3.6A}$	Voltage Difference between CSP and CSN at Nominal 3.6 A	Rcs = 5 mΩ				

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.135 V to 22.5 V, TA = −40°C to +105°C unless otherwise noted. Typical values are at TA = 25°C, VIN = 5.0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UART						
$V_{UART-VIH}$	High−Level Input Voltage	VIN = 3.5 V − 22.5 V	2	−	−	V
$V_{UART-VIL}$	Low−Level Input Voltage	VIN = 3.5 V − 22.5 V	−	−	0.8	V
$V_{UART-HYS}$	Input Hysteresis	VIN = 3.5 V − 22.5 V	−	200	−	mV

Timers

- *32−bit General Purpose Timer* − FUSB15101 has a 32−bit down−counter that can generate an interrupt request

VCONN Switch

Some applications require that a VCONN voltage be sourced in order to provide additional source capabilities when sourcing greater than 3 A on VBUS. The level of over−current protection on VCONN is fixed at 50 mA.

USB PD PHY State Machine Logic

The FUSB15101 PD module includes the following digital functions to enable USB PD messaging:

- Serialization and de−serialization
- Clock and data recovery (CDR)
- 4B5B coding
- BMC coding
- Packet CRC generation and checking
- Coding and detection of Power Delivery K−Codes
- Automatic GoodCRC packet response

BC1.2 Support

The FUSB15101 has the circuitry to enable emulation BC1.2, QC2.0 and 2.4A Divider Mode via firmware.

VBUS Operation

Gate Driver

VBUS from the USB−C connector is typically connected to a load switch NFET (Q1 in Figure 6) source terminal whose gate terminal is driven by the FUSB15101 gate driver via the LGATE pin. **onsemi** recommends NFETs with low I_{GSS} leakages (<1 μA) for optimal gate drive.

Figure 6. VBUS Discharge via BLD Pin

VBUS Discharge

VBUS is discharged through a resistor (RBLD) via the BLD pin of the FUSB15101 as shown in the highlighted section in Figure 6. The external resistor RBLD value is dependent on the total bulk capacitance (CBULK) of the power source so that VBUS is discharged within the time limits dictated by USB PD. A typical value for RBLD is 30 Ω, 1 W and in addition, there is internal resistance that limits the discharge current within the FUSB15101 ($I_{BLD−SINK}$ in the electrical tables above).

When the load current to the Sink is sufficient (exceeds $I_{CS−EN−BLD}$ for $t_{CS−EN−BLD}$ debounce time) such that the internal discharge is not needed, then the FUSB15101 will automatically disable internal discharge.

Upon power up, firmware in the FUSB15101 may discharge VBUS in case there is a voltage on VBUS since the only way a Sink can be attached per Type C specification is if VBUS is discharged to ground (below VSafe0V) upon attach.

The discharge resistance limits are governed by the Type C specification when not sourcing power on VBUS ($R_{BLD−LEAK}$ in the electrical tables above). It is preferred that no external load/discharge resistor is connected to VBUS other than RBLD to the FUSB15101 discharge BLD pin. A TVS diode connected from VBUS to ground ([SZ]ESD7241) allow operating voltages up to 24 V covering the entire VBUS range of 3.3 V to 21 V for a USB PD PPS contract. This can be replaced by a TVS that covers the VBUS range for the use case of this design if needed.

Voltage and Current Sensing Operation

The resistor ratio from VIN to ground formed by resistors R2 and R3 in Figure 7 (typically 1:10 ratio) is sensed via FUSB15101 VREF pin to set the output voltage.

For the offline design in Figure 2, this will be done via the FUSB15101 SFB pin, the opto−coupler, resistor R1 and the primary side PWM controller operation.

For DC−DC design in Figure 3, this will be done via the FUSB15101 SFB pin controlling the buck−boost PWM via its COMP pin.

The FUSB15101 will automatically control the SFB pin based on the desired voltage as determine by the USB PD contract and the existing VIN voltage sensed by VREF.

The external compensation network formed by C2/R2 and R4/C1 need to be selected to achieve stable operation over the range of VBUS voltage and current transitions as shown in Figure 7.

FUSB15101

Table 2. PROTECTION FEATURES

Symbol	Description	Pin(s) Used	Automatic Hardware Protection Capable?
OVP	Output Over Voltage Protection	VIN	Yes
UVP	Output Under Voltage Protection	VIN	Firmware Controlled
OCP	Over Current Protection	CSP & CSN	Yes
I_OTP	Internal Temperature Protection	N/A	Yes
E_OTP	External Temperature Protection	NTCA / NTCB	Firmware Controlled
CC_OVP	HVCC1 or HVCC2 Over Voltage Protection	HVCC1 / HVCC2	Yes

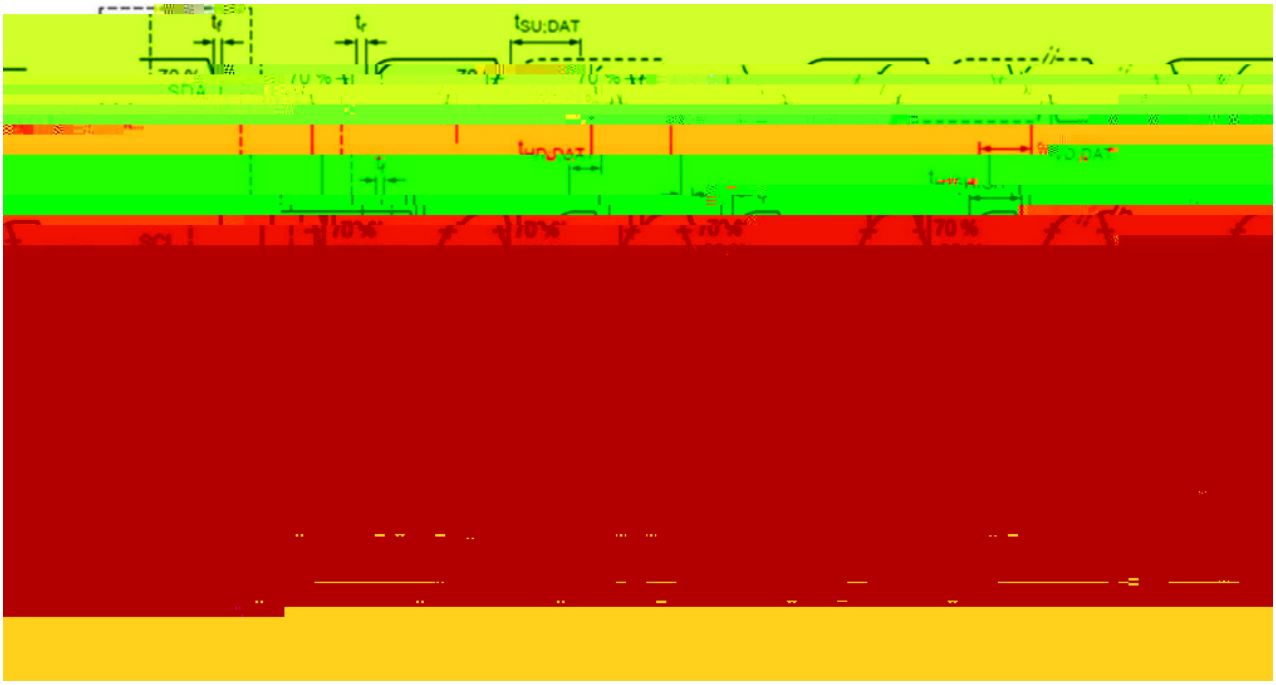


Figure 10. I²C Bus Timing Definition

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH. A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH. During a read from the FUSB15101, the host issues a Repeated Start after sending a data command and before resending the device address. The Repeated Start is a 1−to−0 transition on SDA while SCL is HIGH.

UART

The FUSB15101 implements a UART transceiver that communicates via D+/− when enabled.

When this peripheral is disabled, it should not interfere with D+/− charging protocols such as BC1.2− where the ADC is sensitive to loads.

Clock Requirements and BAUD Rates

The max BAUD rate support is dependent on the CLK_HS speed setting. BAUD rates are supported from 9,600 to 230,400.

Automatic BAUD Rate Detection

The FUSB15101 implements automatic BAUD Rate detection based on the first character received in a message.

The supported characters for automatic BAUD rate detection are 0xAA or 0x55.

Automatic BAUD detection rate works up to 230,400 bps. BAUD Rates detected outside of this range will be flagged as errors to the core.

Port Control and GPIOs

The FUSB15101 includes a number of pins that can be configured to be used as standard GPIO or for use with a dedicated peripheral such as I²C. A subset of these Pins can also be connected as an input to the ADC. Internal pull−up/down resistors are programmable. Pull−up resistors are always connected to VDD.

When the PORT is configured as GPIOs it will have the following capabilities:

- Bi−directional capability
- Push pull or open drain configuration
- Individually configurable interrupt lines
- Rising or Falling edge interrupt
- High− or Low−level interrupt

Table 5. PIN−PORT CONFIGURATION

Pin #	Name	Port
6	GPIO0	PA0
	I2C_INT	
7	GPIO1	PA1
	I2C_SDA	
8	GPIO2	PA2
	I2C_SCL	
9	GPIO3	PA3
	ADC_CH5	
	SWCK	
10	GPIO4	PA4
	ADC_CH6	
	SWD	

ADC

The FUSB15101 allows for up to 7 signals to be measured and converted using the internal 10−bit ADC. For most applications, this will consist of VBUS and VIN voltages,

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NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD