FEATURES

- *Arm® Cortex®−M0+:* A 32−bit core with flexible clocking up to 24 MHz.
- *Memories:* A total of 132 KB of flash is available to store program code. 6 KB of SRAM program memory.
- *USB Type−C and PD:* Integrated hardware USB PD PHY and Type−C termination/comparators supporting latest USB−IF specification.

PIN DESCRIPTION

Pin #	Name	Port	Description
1	VBUS_A	Power	Port A VBUS. Monitoring Discharge (28 V)
2	HVCC2_A	Analog	Port A High Voltage Configuration Channel 2 (28 V)
3	VCONN_A	Power	Port−A VCONN Supply
4	HVCC1_A	Analog	Port A High Voltage Configuration Channel 1 (28 V)
5	VDD	Power	Power Supply
6	I2C_INT2/GPIO2/SWD	PA2	I^2C Port 2 Interrupt/ General Purpose I/O /Serial Wire Debug Data
7	I2C_SDA2/GPIO3	PA3	I^2C Port 2 Data/ General Purpose I/O (Open Drain)
8	I2C_SCL2/GPIO4	PA4	I^2C Port 2 Clock/ General Purpose I/O
9	DP_A	Analog	Port A USB 2.0 D+ (Connector side)
10	DM_A	Analog	Port A USB 2.0 D− (Connector side)
11	DM_HOST_A	Analog	Port A USB 2.0 D− (Host side)
12	DP_HOST_A	Analog	Port A USB 2.0 D+ (Host side)
13	GPIO5/I2C_SDA4/SWCK	PA5	General Purpose I/O/ I^2C Port 4 Data/ Serial Wire Debug Port Clock
14	GPIO6/I2C_SCL4	PA6	General Purpose I/O I^2C Port 4 Clock
15	GPIO7/I2C_INT4	PA7	General Purpose I/O/ I^2C Port 4 Interrupt
16	HPD_A/GPIO8	PA8	Hot Plug Detect/ General Purpose I/O
17	VDDIO	Power	I/O Voltage Supply
18	RESET_N	Input	Active Low chip reset
19	DP_HOST_B	Analog	Port B USB 2.0 D+ (Host side)
20	DM_HOST_B	Analog	Port B USB 2.0 D− (Host side)
21	DM_B	Analog	Port B USB 2.0 D− (Connector side)
22	DP_B	Analog	Port B USB 2.0 D+ (Connector side)
23	I2C_INT1/GPIO9	PA9	I^2C Port 1 Interrupt/ General Purpose I/O
24	I2C_SCL1/GPIO10	PA10	I^2C Port 1 Clock/ General Purpose I/O (Open Drain)

54.6 68.0441 344.9197 Tm(I)4.sid9o.0 D+ (Co841 461.367 47.849 .90707 refBT8 0 0 2 516.8598 329.55[71 Tm(I2C_SCL1)86.6(1.7(A10)] ref1071 344

ELECTRICAL SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VDD = 2.8 V to 5.5 V, TA = −40°C to +85°C unless otherwise noted. Typical values are at TA = 25°C, VDD = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TYPE−C FRONT END						
R_{SW_CCx}	Rdson for VDD to CC1 or VDD to CC2	I_{SW_CCX} = 0 to 600 mA, VCONN_OCP > 80 mA	−	0.85	1.8	Ω
$R_{SW\_CCx\_LOW\_OCP}$	Low OCP Setting Rdson for VDD to CC1 or VDD to CC2	I_{SW_CCX} = 0 to 80 mA, VCONN_OCP ≤ 80 mA	−	2.7	5	Ω
vRdSRCUSB	Source Attach Threshold for CC Pin at Default Current		1.5	1.6	1.65	V
vRdSRC1.5	Source Attach Threshold for CC Pin at 1.5 A Current		1.5	1.6	1.65	V
vRdSRC3.0	Source Attach Threshold for CC Pin at 3 A Current		2.45	2.6	2.75	V
vRaSRCUSB	Source Ra Threshold for CC Pin at Default Current		0.15	0.2	0.25	V
vRaSRC1.5	Source Ra Threshold for CC Pin at 1.5 A Current		0.35	0.4	0.45	V
vRaSRC3.0	Source Ra Threshold for CC Pin at 3 A Current		0.75	0.8	0.85	V
vRdSNKUSB	Attach Threshold for CC Pin SNK (Default Current)		0.61	0.66	0.7	V
vRdSNK1.5	Attach Threshold for CC Pin SNK (1.5 A Current)		1.16	1.23	1.31	V
vRdSNK3.0	Attach Threshold for CC Pin SNK (3 A Current)		2.04	[illegible]		

ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VDD = 2.8 V to 5.5 V, TA = −40°C to +85°C unless otherwise noted. Typical values are at TA = 25°C, VDD = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GPIO						
$V_{OL-GPIO}$	Output Low Voltage	VDDIO = 1.7 V to 5.5 V, Iout = +4 mA	−	−	0.4	V
V_{OH-SNK}	SNKx Pin Output High Voltage		2.5	−	−	V
V_{OL-SNK}	SNKx Pin Output Low Voltage		−	−	0.4	V
V_{OH-NTC}	Output High Voltage for PA4 and PA8	VDD = 2.8 V to 5.5 V, Iout = −2mA	VDD – 0.5	−	−	V

- *External Pin Reset* – The external reset is under user control with the external RESET_N pin. External pin reset resets the entire chip including core, debug port, peripherals, wakeup timer, and watchdog

Power and Sleep Behavior

The FUSB15200 has been optimized to conserve power by utilizing peripheral interrupts and hardware autonomy. The device can be configured via firmware to enter low power states, disable unneeded peripherals and scale clock frequencies based on different application needs.

The Type−C block is designed to function at the lowest

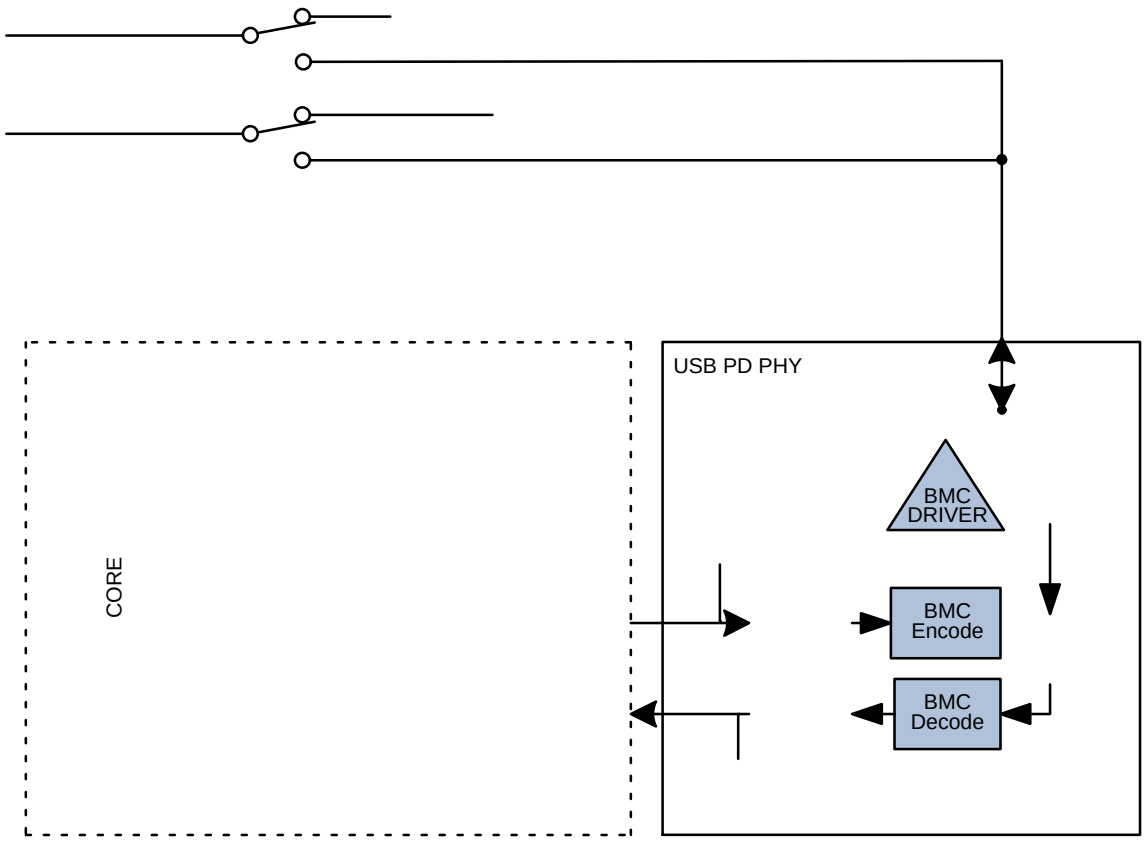

Figure 5. USB Type−C and PD

Fast Role Swap

Fast Role Swap is the process of exchanging the Source and Sink roles between Port Partners rapidly due to the disconnection of an external power supply.

The Fast Role Swap process is intended for use by a capable USB device that presently has an external power supply, and is providing power both through its downstream Ports to USB Devices and upstream to a USB Host such as a laptop. On removal of the external power supply Fast Role Swap enables a VBUS supply to be maintained by allowing the USB Host to apply vSafe5V after having detected Fast Role Swap signaling. The initial Source will signal a Fast Role Swap request by driving CC to ground with a resistance

Table 1. PIN − PORT CONFIGURATION AND POWER DOMAIN

Pin #	Name	Port	Power Supply
40	SRC_SNK_N_A	PA1	VDDIO
	GPIO1		VDDIO
6	I2C_INT2	PA2	VDD
	GPIO2		VDDIO
	SWD		VDDIO
7	I2C_SDA2	PA3	VDD
	GPIO3 (OD)		VDDIO
8	I2C_SCL2	PA4	VDD
	GPIO4		VDDIO
13	I2C_SDA4	PA5	VDD
	GPIO5		VDDIO
	SWCK		VDDIO
14	I2C_SCL4	PA6	VDD
	GPIO6		VDDIO
15	I2C_INT4		

Table 2. PORT DEFAULT CONFIGURATION

Pin #	FUSB15200 Pin Name	Port	Default Configuration on Power Up	I/O State	NMI	Analog Function
40	SRC_SNK_N_A/GPIO1	PA1	GPIO1	Input Float		
6	I2C_INT2/GPIO2/SWD	PA2	SWD	Input		
7	I2C_SDA2/GPIO3	PA3	GPIO3 (OD)	Input Float		
8	I2C_SCL2/GPIO4	PA4	GPIO4	Input Float		
13	GPIO5/I2C_SDA4/SWCK	PA5	SWCK	Input		
14	GPIO6/I2C_SCL4	PA6	GPIO6	Input Float		
15	GPIO7/I2C_INT4	PA7	GPIO7	Input Float	Yes	
16	HPD_A/GPIO8	PA8	GPIO8	Input Float		
23	I2C_INT1/GPIO9	PA9	GPIO9	Input Float		
24	I2C_SCL1/GPIO10	PA10	GPIO10 (OD)	Input Float		
25	I2C_SDA1/GPIO11	PA11	GPIO11	Input Float		
26	HPD_B/GPIO12	PA12	GPIO12	Input Float		
31	GPIO13	PA13	GPIO13	Input	Yes	
32	SRC_SNK_N_B/GPIO14	PA14	GPIO14	Input Float		
33	SNK_B/GPIO15/NTC_B	PA15	GPIO15	Input Float	Yes	Yes
34	GPIO16	PA16	GPIO16	Input		
35	I2C_INT3/GPIO17	PA17	GPIO17	Input Float	Yes	
36	I2C_SDA3/GPIO18	PA18	I2C_SDA	Input		
37	I2C_SCL3/GPIO19	PA19	I2C_SCL	Input		
39	SNK_A/GPIO20/NTC_A	PA20	GPIO20	Input Float		Yes

Non−Maskable Interrupts (NMI)

The FUSB15200 provides a method of selecting one of four GPIOs that can be used as a source of an external non−maskable interrupt. (See table 2)

If a non−maskable external interrupt is not required, all GPIOs provide a method to interrupt the processor. In this case, the Brown−Out detector can be assigned to the NMI slot of the interrupt controller.

The port mapping, power domain and default configuration are shown in the Table 2.

HPD I/Os

HPD I/Os are used in DisplayPort (DP) applications to signal events between the DP Source and DP Receiver.

The FUSB15200 HPD I/Os can be configured as an input (DP receiver) or Output (DP Source).

The HPD I/Os supply is derived from an internal 3.0 V regulator to guarantee levels in all conditions.

DP Receiver Behavior

When the FUSB15200 is implemented in a DP Receiver, the HPD I/O is setup as an input. Debounce timers implemented in HW facilitates HPD IRQ and Level detection. Please see HPD_Rx in Electrical Specifications.

DP Source Behavior

When the FUSB15200 is implemented in a DP Source, the HPD I/O is setup as an Output.

The HPD output will be driven by the firmware. HPD IRQ puld in Displayn areo1.(I2C_SDA3/GP638 Tm-.r)Tj/F5 1 Tf10 0 0 10d i5

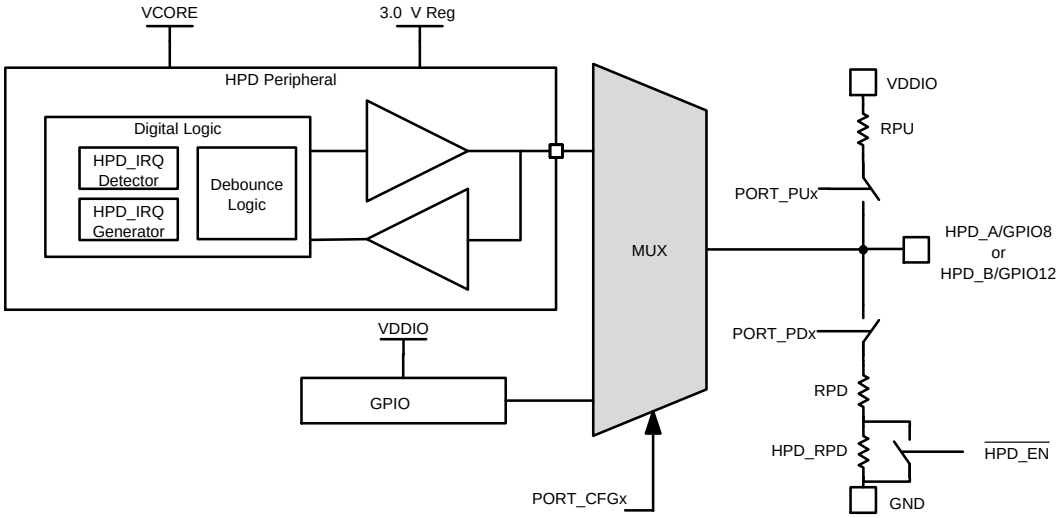

Figure 8. HPD I/O Configuration

External Temperature Measurements

There are two pins that can be configured to monitor external NTC resistors that can be located near where high temperature devices are located. A parallel resistor is recommended for measurement linearity.

These NTC measurements are useful for monitoring temperatures for protection due to excessive thermals.

Firmware implementation of the external temperature measurements make NTC selection flexible.

The pull−up current sources INTCA and INTCB provide a bias to the external NTC resistor networks. If desired, this current source may be turned−off.

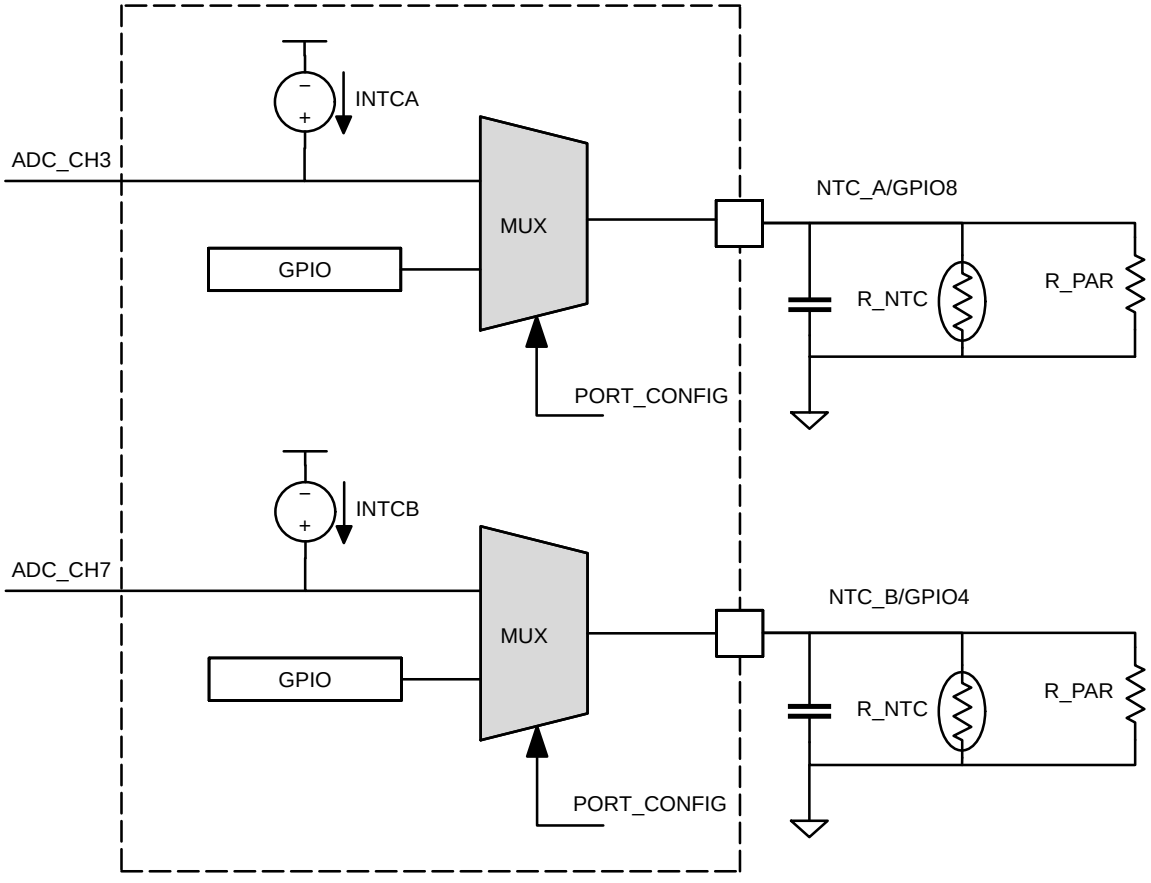

Figure 9. External NTC Diagram

ADC

The FUSB15200 allows for up to 12 signals to be measured and converted using the internal 10−bit ADC. For most applications, this will consist of two VBUS voltages, two NTC temperature channels, two D+/D− BC1.2 and, optionally, two CC1/2 ports. The table below shows the typical FUSB15200 configuration along with the expected settings for the ADC module.

Table 3. ADC CONFIGURATION ADC CHANNEL

ADC Channel	Pin Measurement	Resolution	Range	Full Scale Voltage
0	VBUS_A	10 mV	0 V to 10.23 V	1.024 V
		20 mV	0 V to 20.46 V	2.048 V
		40 mV	0 V to 40.92 V	4.096 V
1	DP_A	4 mV	0 V to 4.096 V	4.096 V
2	DM_A	4 mV	0 V to 4.096 V	4.096 V
3	NTC1 Temperature	1°C	0°C to 160°C	1.28 V
4	HVCC1_A	4 mV	0 V to 4.096 V	4.096 V
5	HVCC2_A	4 mV	0 V to 4.096 V	4.096 V
6	VBUS_B	10 mV	0 V to 10.23 V	1.024 V
		20 mV	0 V to 20.46 V	2.048 V
		40 mV	0 V to 40.92 V	4.096 V
7	DP_B	4 mV	0 V to 4.096 V	4.096 V
8	DM_B	4 mV	0 V to 4.096 V	4.096 V
9	NTC2 Temperature	1°C	0°C to 160°C	1.28 V
10	HVCC1_B	4 mV	0 V to 4.096 V	4.096 V
11	HVCC2_B	4 mV	0 V to 4.096 V	4.096 V

Development Tools

FUSB15200 is supported by a full suite of comprehensive tools including:

- An easy−to−use development board
- Software Development Kit (SDK) including:
  USB PD protocol stacks, shared capacity algorithms, sample code, libraries, and documentation

Specifications References

- Universal Serial Bus Power Delivery specification revision 3.1 Version 1.3, dated January 2022
- Universal Serial Bus Type C Cable and Connection Specification release 2.1, dated May 2021
- USB Battery Charging Specification, revision 1.2, dated December 7, 2010
- I2C−bus specification Rev. 6 – 4 April 2014