Features

- **Arm Cortex−M0+**: A 32−

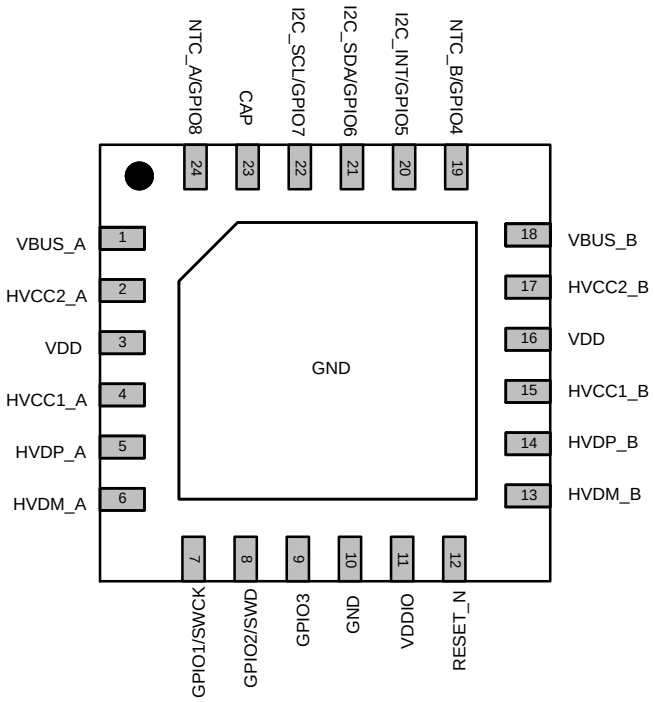

Figure 2. Pin Diagram

Table 1. FUNCTION DESCRIPTION

Pin #	Name	Port	Description
1	VBUS_A	Analog	Port A VBUS. Monitoring Discharge (28 V)
2			

ELECTRICAL SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

Symbol	Parameter	Minimum	Maximum	Unit
VBUS	VBUS Pin Voltage	0.3	28	V
$V_{CONNECTOR}$	HVCC1, HVCC2 Connector Pins	0.3	28	V
V_{USB}	HVDP, HVDM Connector Pins (FUSB15201)	0.3	20	V
	HVDP, HVDM Connector Pins (FUSB15201D)	0.3	28	V
VIO	I/O Voltage	0.5	6.0	V
VDD	Supply Voltage	0.5	6.0	V
VDDIO	VDDIO Supply	0.3	6.0	V
VCAP	CAP Pin	0.5	2.0	V
T_J	Junction Temperature	40	150	°C
T_{STG}	Storage Temperature	40	150	°C
TL	Lead Temperature (Soldering, 10 Seconds)		260	°C
ESD_{HBM}	Human Body Model, ANSI/ESDA/JEDEC JS – 001 – 2012 (Note 3)	2		kV
ESD_{CDM}	Charged Device Model, JESD22 – C101 (Note 3)	750		V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to the GND Pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS 001 2012 and JESD 22 C101.

Table 3. RECOMMENDED ESD DEVICES

Function	Manufacturer	Part Number
Type C Connector Pins ESD	**onsemi**	TBD

Table 4. THERMAL RATINGS (Note 4)

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction to Ambient Thermal Resistance		57		°C/W

4. T_A = 25°C unless otherwise specified with JEDEC 2S2P board with no thermal vias.

Table 5. OPERATING RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range	3.0	3.3	5.5	V
V_{BUS}	V_{BUS} Voltage	3.1		22.05	V
V_{DDIO}	I/O Supply Voltage	1.7		5.5	V
V_{HVCCx}	Communication Channel Pins	0		5.5	V
V_{HVUSB}	HVDM, HVDP Pins	0		3.6	V
V_{IO}	GPIO, I^2C, RESET	0		5.5	V
T_A	Operating Ambient Temperature	40		+105	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ELECTRICAL CHARACTERISTICS
Minimum and maximum values are at V_{DD} = 2.8 V to 5.5 V, T_A = 40°C to +105°C unless otherwise noted.
Typical values are at T_A = 25°C, V_{DD} = 3.3 V

TYPE−C AND PD SECTION						
USB PD PHY						
TRANSMITTER						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
UI	Unit Interval					

Table 6. ELECTRICAL CHARACTERISTICS (continued)
Minimum and maximum values are at V_{DD} = 2.8 V to 5.5 V, T_A = 40°C to +105°C unless otherwise noted.
Typical values are at T_A = 25°C, V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Min	Typ	Max	Units

Table 6. ELECTRICAL CHARACTERISTICS (continued)
Minimum and maximum values are at V_{DD} = 2.8 V to 5.5 V, T_A = 40°C to +105°C unless otherwise noted.

Table 6. ELECTRICAL CHARACTERISTICS (continued)
Minimum and maximum values are at V_{DD} = 2.8 V to 5.5 V, T_A = −40°C to +105°C unless otherwise noted.

FUSB15201

Power and Sleep Behavior

The FUSB15201 has been optimized to conserve power by utilizing peripheral interrupts and hardware autonomy. The device can be configured via firmware to enter low power states, disable unneeded peripherals and scale clock frequencies based on different application needs.

The Type−C block is designed to function at the lowest power states and will automatically wake when a Type−C attach is detected. This minimizes total power consumption when no device is attached.

Clock Sources

FUSB15201's implements a dual oscillator architecture to minimize power consumption.

- A 24 MHz internal RC oscillator to enable full functionality.
- A 120 kHz internal RC oscillator that can be used for very low power sleep modes.

TIMERS

32−bit General Purpose Timers (TIM0/1)

There are two 32−bit down−counters that generate interrupts and status when the counter reaches 0. The timing resolution depends on the programmable clock source and pre−scale ratios.

32−bit Wake−up Timer (WUT)

The main purpose of the wakeup timer is to facilitate scheduled exit from low power modes. It can also be used for general purpose event timing.

32−bit Watchdog Timer (WDT)

The watchdog timer applies a reset to the system in the event of a software failure, providing a way to recover from software crashes. The watchdog timer is disabled by default and must be enabled through software.

The watchdog is protected with a lock mechanism to prevent rogue software from disabling the watchdog functionality. A special value has to be written to the lock register to access watchdog control. The watchdog timer is clocked from the same oscillator as the core, which can be LS_CLK or HS_CLK.

Serial Wire Debug Interface (SWD)

The Arm M0+ implementation includes a Debug Access Port (DAP). The debug mode implementation includes 4 hardware breakpoints and 2 hardware watch points.

The Debug Access Port interface implementation is the Arm Serial Wire Debug Port (SW−DAP) connected to Pins SWCLK and SWDIO. The Serial Wire Debug Port Interface uses a single bi−directional data connection. Each operation consists of three phases: Packet request, Acknowledge response, and Data transfer phase. Use any Serial Wire Debug (SWD) compliant hardware debugger interface to interact with the internals of the FUSB15201.

USB Type−C & PD Peripheral Overview

The USB Type−C and PD peripheral is a fully compliant USB Type−C and PD solution.

This peripheral consists of an analog front end and a digital state machine. Firmware implements the higher level protocol and policy layers whereas the analog and digital components can perform lower level PD protocol and PHY layer functions.

The Type−C block includes all terminations and comparators required for Source/Sink/DRP operation: plug orientation detection, power capability advertisement and power role detection. If no VDD is applied, the CC Pins are high impedance.

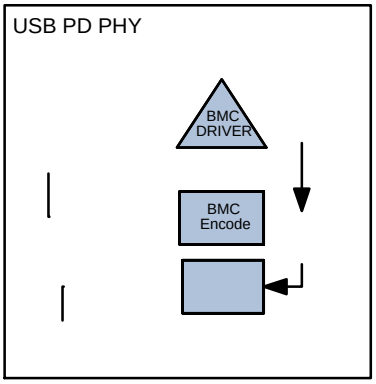

Figure 5. USB Type−C and PD

INTERNAL PROTECTION

The FUSB15201 integrates multiple system level protections to enable robust designs.

VCONN Over−Current Protection

Each port's VCONN Switch provides over−current detection and protection for the switch that is enabled based on the Type−C orientation and can be software configured based on application needs. The level of OCP can be controlled via a register setting.
In case of an over−current event the switch will be opened.

CC, DP, DM Over−Voltage Protection

Over−voltage protection on connector Pins protects the internal circuitry damage from high voltages.
Interrupts can be used to inform the software that an OVP event has occurred and take appropriate actions.

Internal Over Temperature Protection

Internal over temperature protection is always on. Two potential sources of elevated internal temperature are:

- High Current through VCONN Switch
- High current through VBUS discharge

In either case, if the over temperature is triggered (T > Tshut), both ports' VCONN switches and VBUS discharge circuitry will be disabled.

Connector Moisture Detection

If moisture or pollutants are present in the connector and the device provides VBUS, there could be a resistive short between VBUS and other connector Pins.

The FUSB15201 provides a method to detect if there is moisture or other pollutants in the connector.

Moisture detection can be turned on or off as not to conflict with cable attach detection.

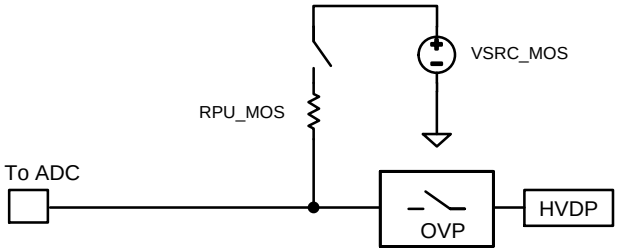

Figure 6. Moisture Detection

Port Control and GPIOs

The FUSB15201 includes a number of Pins that can be configured to be used as standard GPIO or for use with a dedicated peripheral such as I^2C. A subset of these Pins can also be connected as an input to the ADC. Internal pull−up/down resistors are programmable. Pull−up resistors are always connected to VDDIO.

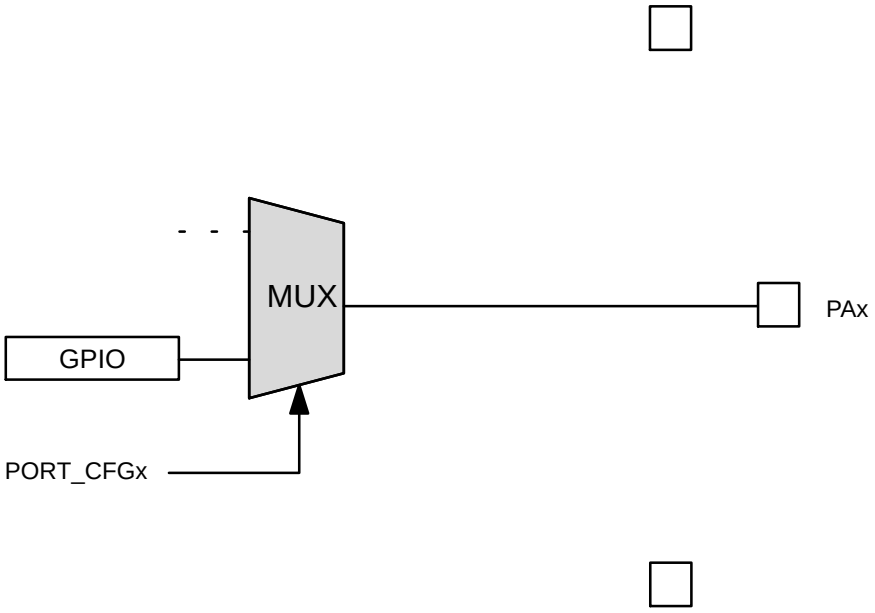

Figure 7. Typical Port Configuration

When the PORT is configured as GPIOs it will have the following capabilities:

- Bi−directional capability
- Push pull or open drain configuration
- Individually configurable interrupt lines
- Rising or Falling edge interrupt
- High or Low level interrupt

The port mapping and power domain is shown in the table below:

BC1.2 Support

The FUSB15201 is capable of emulating and detecting BC1.2 and Divider Mode.
The following modes are supported:

- SDP
- CDP
- DCP
- 2.4 A Divider Mode (Provider only)

The analog circuitry is firmware configurable for the function required by the application and follows the final BC1.2 specification.

I²C

The FUSB15201's serial interface is compatible with Standard, Fast, and Fast Mode Plus I²C bus specifications. The I²C peripheral can be configured for either host or device modes.

Bus Timing

As shown in figure below, for data bits, SDA must be stable while SCL is HIGH. SDA may only transition when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

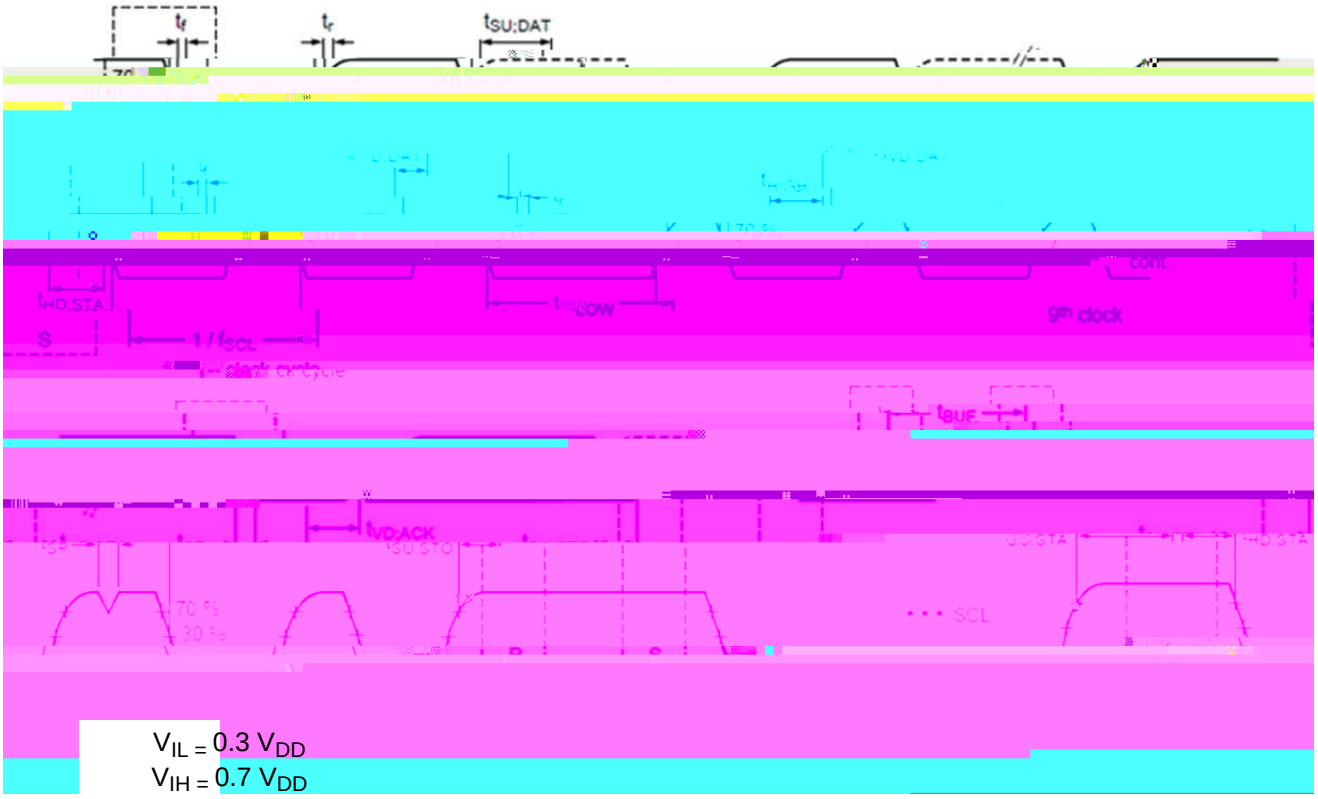

Figure 9. I²C Bus Timing Definition

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH.

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH.

During a read from the FUSB15201, the host issues a Repeated Start after sending a data command and before resending the device address. The Repeated Start is a 1−to−0 transition on SDA while SCL is HIGH.

[1] Bus timing referenced from I²C bus specification Rev. 6 – 4 April 2014

ADC

The FUSB15201 allows for up to 12 signals to be measured and converted using the internal 10−bit ADC. For most applications, this will consist of two VBUS voltages, two NTC temperature channels, two D+/D− BC1.2 and, optionally, two CC1/2 ports. The table below shows the typical FUSB15201 configuration along with the expected settings for the ADC module.

Table 8. ADC CONFIGURATION

ADC Channel	Pin Measurement	Resolution	Range	Full Scale Voltage
0	VBUS_A	10 mV	0 V to 10.23 V	1.024 V
		20 mV	0 V to 20.46 V	2.048 V
		40 mV	0 V to 40.92 V	4.096 V
1	DP_A	4 mV	0 V to 4.096 V	4.096 V
2	DM_A	4 mV	0 V to 4.096 V	4.096 V
3	NTC1 Temperature	1°C	0°C to 160°C	1.28 V
4	HVCC1_A	4 mV	0 V to 4.096 V	4.096 V
5	HVCC2_A	4 mV	0 V to 4.096 V	4.096 V
6	VBUS_B	10 mV	0 V to 10.23 V	1.024 V
		20 mV	0 V to 20.46 V	2.048 V
		40 mV	0 V to 40.92 V	4.096 V
7	DP_B	4 mV	0 V to 4.096 V	4.096 V
8	DM_B	4 mV	0 V to 4.096 V	4.096 V
9	NTC2 Temperature	1°C	0°C to 160°C	1.28 V
10	HVCC1_B	4 mV	0 V to 4.096 V	4.096 V
11	HVCC2_B	4 mV	0 V to 4.096 V	4.096 V

Development Tools

FUSB15201 is supported by a full suite of hardware including:

- An easy−to−use development board
- Software Development Kit (SDK) including:
  USB PD protocol stacks, shared capacity algorithms, sample code, libraries, and documentation

Specifications References

- Universal Serial Bus Power Delivery specification revision 3.1 Version 1.3, dated January 2022
- Universal Serial Bus Type C Cable and Connection Specification release 2.1, dated May 2021
- USB Battery Charging Specification, revision 1.2, dated December 7, 2010
- I^2C−bus specification Rev. 6 – 4 April 2014

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