F B251

-C CC B
P IC

www.onsemi.com

WLCSP15, 1.49x2.06x0.574
CASE 567WV

PRODUCT SUMMARY

General Description

The FUSB251 is an I2C controlled switch with over voltage protection on CC and SBU pins in Type−C interface port. The device has SPST switches on CC1/2 and SBU1/2 which enable automatically with valid VDD so that Type−C/PD controller can use the over voltage protected CC path. The FUSB251 has dead battery mode, CC pulled down hat Tyhrgi0syhrgi0d3,eichip IEC protection with surge
C and SBU. Both CC and SBU ports are 24 V DC
ype is WLCSP with 15 ball 3x5 array.

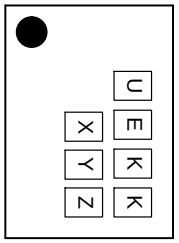
Features

- Low Ron SPST Switches on both CC1/2 and SBU1/2 Path for Type−C
- Dead Battery Mode Provides Default Rd Presenting on CC1/2
- 24 V DC Tolerant on CC and SBU
- ±35 V Surge Protection on CC and SBU
- Over Voltage Protection on CC and SBU
- I2C Interface with Processor with Interrupt for event Notification
- Moisture Detection on CC and SBU Pins
- On−chip IEC ESD Protection with External Capacitor on CAP Pin
- CC Ron 0.3 Ω Typical
- SBU Ron 3 Ω Typical
- 50 MHz Bandwidth on SBU Switch
- 15 ball WLCSP

Applications

- Smart Phones
- Tablets, Netbooks, Ultra−Mobile PCs
- Gaming Devices and E−books
- Portable Devices with Li−ion Battery
- Car Cigarette Jack
- External USB Storage

MARKING DIAGRAM



UE	= 2 digit Device Identifier
KK	= 2 digit Lot Run Code
XY	= 2 digit Date Code
Z	= 1 digit Plant Code
●	= Pin A1 Mark

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

APPLICATION DIAGRAM

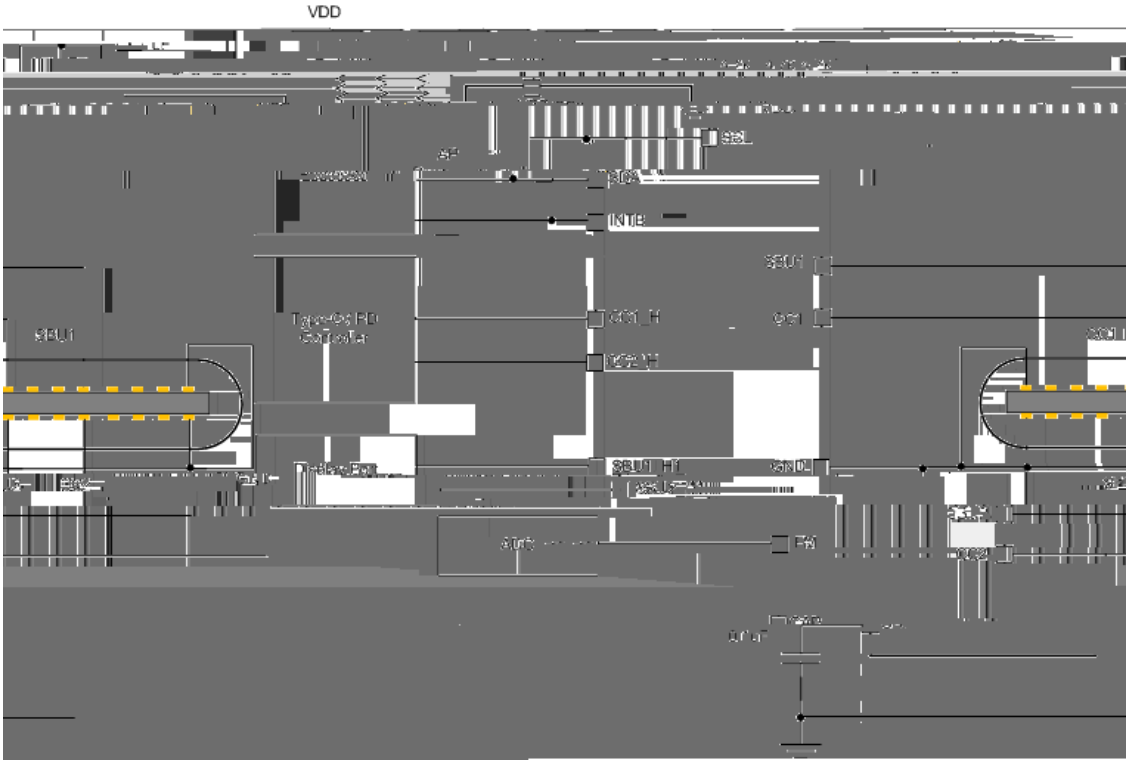


Figure 1. Application Diagram

PART NUMBERING

ORDERING INFORMATION

Part Number	Temperature Range	Package	Packing Method †
FUSB251UCX	40 to 85°C	WLCSP, 3 x 5 array, 15 ball, 1.49 mm x 2.06 mm	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PRODUCT PIN ASSIGNMENTS

Pin Configuration

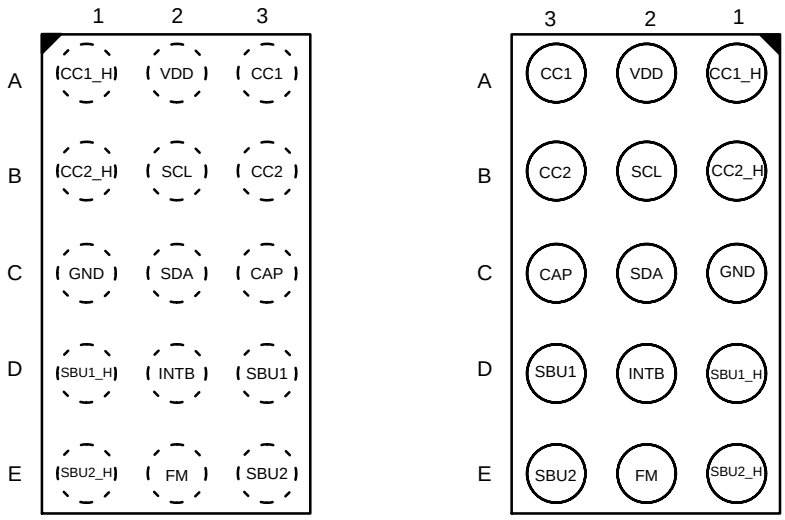


Figure 2. Pin Configuration

Pin Descriptions

PIN DESCRIPTIONS

Pin#	Name	Type	Description
C1	GND	Ground	GND
A2	VDD	Power	Power
A3	CC1	I/O	Type C CC interface. Connect to USB Type C connector CC1 pin
B3	CC2	I/O	Type C CC interface. Connect to USB Type C connector CC2 pin
A1	CC1_H	I/O	Type C CC Host interface, Connect to USB Type C controller CC1 pin
B1	CC2_H	I/O	Type C CC Host interface, Connect to USB Type C controller CC2 pin
D3	SBU1	I/O	Type C SBU interface, Connect to USB Type C connector SBU1 pin
E3	SBU2	I/O	Type C SBU interface, Connect to USB Type C connector SBU2 pin
D1	SBU1_H	I/O	Type C SBU Host Interface, Connect to Host side SBU1 application pin
E1	SBU2_H	I/O	Type C SBU Host Interface, Connect to Host side SBU2 application pin.
E2	FM	I/O	Factory test mode pin, Connect to ADC input of host processor. If not used, connect to GND. FM can be switched over to one of SBU.
C3	CAP	O	Capacitor pin, Connect to 0.1 μF capacitor to GND
B2	SCL	Open Drain Input	I^2C interface, Pull up to Vdd is required, Connect to SCL pin of Processor
C2	SDA	Open Drain I/O	I^2C interface, Pull up to Vdd is required, Connect to SDA pin of Processor
D2	INTB	Open Drain Output	Interrupt for Host alert, Pull up to VDD required, Connect to processor Interrupt input

PRODUCT BLOCK DIAGRAM

Block Diagram

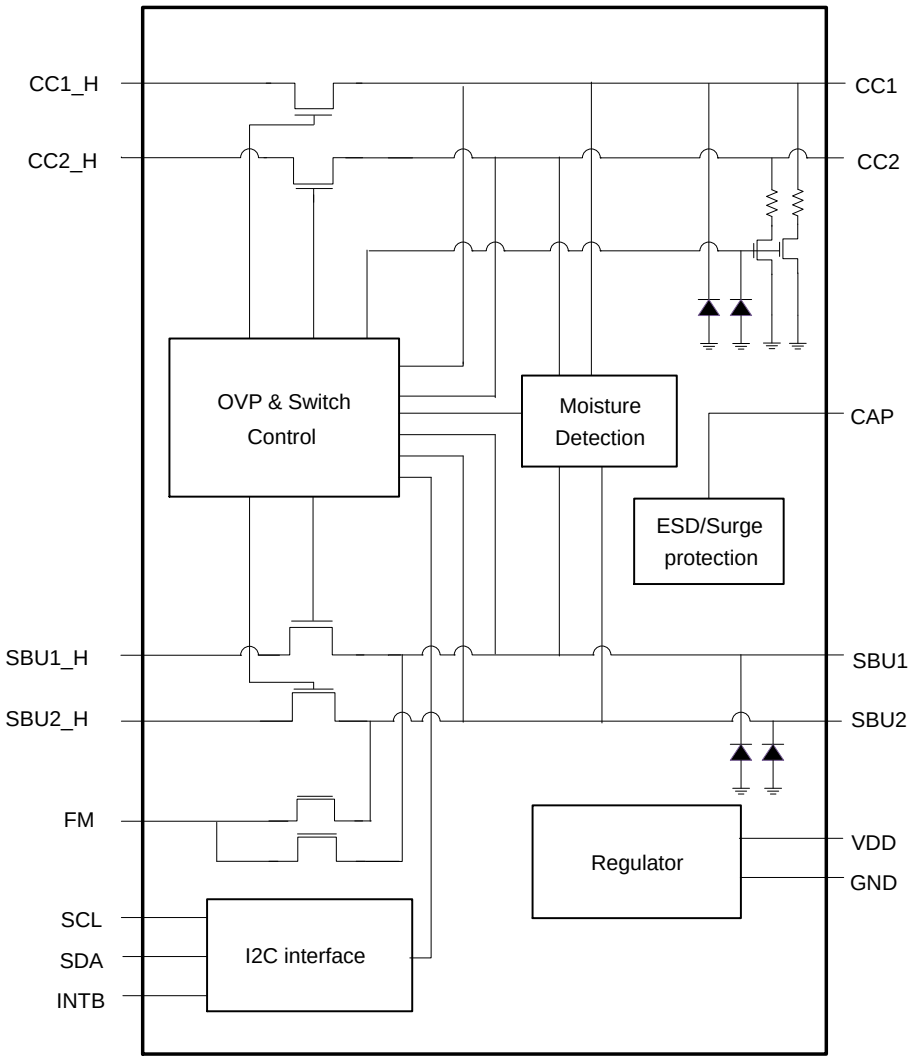


Figure 3. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_J	Junction Temperature		40		+150	°C
T_{STG}	Storage Temp		65		+150	°C
VDD	Supply voltage	Slew Rate 2 V/μs (rising), 1 V/μs (falling)	0.5		12.0	V
VCC	Vccx to GND		0.5		24	V
VSBU	VSBUx to GND		0.5		24	V
VCCx_H and VSBUx_H	VCCX_H, VSBUx_H to GND		0.5		6.0	V
ICCSW	DC CC switch current				1.25	A

[redacted]

ESD RATINGS – JEDEC / IEC SPECIFICATION

Electro Static Discharge (ESD) Specifications	Condition		Value	Unit
Human Body Model, JEDEC JESD22 A114	CCx and SBUx pins to GND		±5000	V
	Other pins		±2000	
Charged Device Model, JEDEC JESD22 C101	All pins		±1000	
IEC 61000 4 2 System ESD	CCx and SBUx pins to GND	Air gap Discharge	±15000	
		Contact Discharge	±8000	
IEC 61000 4 5 Lightning and Surge	CCx and SBUx pins to GND		±35	

OPERATING CONDITIONS

[redacted]

VDD

ELECTRICAL SPECIFICATION TABLE Unless otherwise specified: Recommended T_A and T_J temperature ranges. All typical values are at T_A = 25°C and VDD = 3.8 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_Q	Quiescent supply current	VDD = 2.7 to 5.5 V, Switch is closed, no load, moisture detection is not enabled		15		μA
I_{MOS}	Current with moisture detection enabled	VDD = 2.7 to 5.5 V, Switch is closed, CC toggle and CC moisture detection is enabled, Avg for 1 sec		30		μA
I_{DRY}	Current consumption when Dry check is working on	VDD = 2.7 to 5.5 V, Moisture detected, and Dry check enabled, T(PD, period) = 4 sec		15		μA
I_{OFF}	Power off leakage current	VDD = 0 V, Except CC1/CC2		1		μA
V_{UVLO}	Under voltage Lockout	VDD Rising, VDD Falling		2.45 (Rising), 2.40 (Falling)	2.55 (Rising)	V
T_{SD}	Thermal Shut down	Shutdown Threshold/ Return from Shutdown/ Hysteresis		150°C (shutdown), 130°C (Return), 20°C (Hysteresis)		
I_{CC_LEAK}	CC ON leakage current	VDD = 2.7 to 5.5 V, CC Switch closed, CCx_H float, measure leakage from CCx with 3.3 V			0.5	μA
R_{ON_CC}	CC1, CC2 RON resistance	VDD = 2.7 to 5.5 V, IOUT = 200 mA		300		mΩ
$R_{Flatness\_CC}$	VDD = 2.7 to 5.5 V, Vcc swing = 0 V 1.2 V			10		mΩ
V_{OVP_CC}	CC over voltage protection threshold	VDD = 2.7 to 5.5 V, VCC rising	5.70	5.85	6.00	V
$V_{OVP\_CC\_FALL}$	CC recover threshold when voltage on CC is falling	VDD = 2.7 V to 5.5 V		5.70		V
$V_{OV\_HYS\_CC}$	CC OVP threshold Hysteresis	VDD = 2.7 to 5.5 V			0.15	V
t_{CC_OVP}	CC OVP Trip time (Note 1)	VDD = 2.7 to 5.5 V, CCx rise from 4 V to 6 V with 1 V/ns slew rate, RL = 30 Ω on CCx_H		250		ns
Rd_CC	Dead battery pull down resistance	VDD = 0 to UVLO, Dead battery resistance / Voltage on pin	4.1	5.1	6.1	kΩ
V_{OVP_SBU}	SBU over voltage threshold	VDD = 2.7 to 5.5 V, SBU Rising	4.4	4.5	4.7	V
$V_{OVP\_SBU\_FALL}$	SBU OVP recovery threshold when voltage on SBU is falling	VDD = 2.7 V to 5.5 V		4.35		V
$V_{OV\_SBU\_HYS}$	SBU OVP Hysteresis	VDD = 2.7 to 5.5 V, Measure difference between SBUX rising and falling OVP threshold			0.15	V

FUNCTIONAL SPECIFICATIONS

POR and Reset

The FUSB251 closes both CC and SBU switches with a valid VDD supply after Power On reset. Until valid VDD is supplied, FUSB251 presents Rd on both CC1 and CC2 so that a source device can provide Vbus and Type−C controller can present Rd continuously after POR so VBUS will be consistent. At UVLO condition which is 2.4 volt (falling), CC and SBU switches get open again and Rd will be presented on both CC.

There is device reset register, bit0 in 0x0B register. If the register bit is set, all registers in the device are set to default, so momentarily both switches will be open and closed back.

Dead Battery Mode Characteristics

CC and SBU Switch Characteristics

The FUSB251 has 2x SPSTChara,(vrx0001ches with a)TJ-8957 52 TD0Twx3245that a

I2C Interface

The FUSB251 includes a full I2C slave controller. The I2C slave fully complies with the I2C specification version 6 requirements. This block is designed for fast mode signals. Examples of an I^2C write and read sequence are shown in below figures respectively.

Figure 5. I^2C Write Example

Detection time on CC moisture is dependent on the settling time and number of ADC read, default is 1 time ADC and 400 μs settle time. They can be programmed in Timer2 register, 0x0C.

SBU Moisture Detection

If CC port is on DRP or Source mode, moisture inside connector can make leakage path from CC to SBU, which makes SBU can have float voltage similar to the shape of CC. So the SBU float voltage can be detected if moisture is present while CC is on toggle or SRC mode. SBU float voltage detection can be started with the EN_SBUFT register set. If the bit is set, FUSB251 starts monitoring voltage on both SBU1 and SUB2, and if the voltage on either port is the same or above the threshold, the moisture_status register (0x06, bit 4 and/or 5) is set with an interrupt. With the interrupt, processor can turn off the CC and SBU switch path to protect from corrosion, or processor could further moisture check using force SBU detection.

SBU float voltage detection also can be enabled when CC moisture detection result is timer expire, which can happen where there is no DRP toggle on CC. For example, if CC moisture detection is enabled where Type−C accessory is already plugged−in, the moisture detection will end up timer expire and so SBU float voltage detection will be started instead.

Once SBU float voltage detection is enabled, it keeps monitoring until moisture found. If device is reset or both EN_CC and EN_SBUFT are disabled, the floating detection stops and goes back to disable mode which is idle mode.

Force SBU detection is initiated by EN_SBU or Auto_EN_SBU bit. Auto_EN_SBU bit is for pre−set before moisture is detected, EN_SBU can be set at anytime when SBU moisture detection is needed. After either CC or SBU float voltage detection detected moisture, if Auto_EN_SBU bit is set, FUSB251 goes to moisture detection on SBU with

ADC TABLE FOR MOISTURE DETECTION

	Bit	Pull up (kΩ) to 1 V	Moisture resistance (kΩ)	Voltage (V)
0	0	320	17	0.05
1	1	320	36	0.1
2	10	320	56	0.15
3	11	320	80	0.2
4	100	320	107	0.25
5	101	320	137	0.3
6	110	320	172	0.35
7	111	320	213	0.4
8	1000	320	262	0.45
9	1001	320	320	0.5
10	1010	320	391	0.55
11	1011	320	480	0.6
[redacted]	1100	320	594	0.65
[redacted]	1101	320	747	0.7
[redacted]	1110	320	960	0.75
[redacted]	1111	320	1,280	0.8

[redacted]TABLE

	Read Only	Write Only	Read / Write	Read / Clear	Write / Clear

[redacted]t[7]	Bit[6]	Bit[5]

DEVICE ID
Address: 01h
Reset Value: 0x100X_XXXX
Type: Read

Bit #	Name	R/W/C	Size (Bits)

INTERRUPT_MASK
Address: 04h
Reset Value: 0x0000_0000
Type: Read / Write

3	Mask_Dry_Detect	R/W	1	1 : Mask DRY status change interrupt
2	Mask_MOS_Detect	R/W	1	1 : Mask Moisture status change interrupt
1	Mask_OVP_REC	R/W	1	1 : Mask OVP recovery interrupt
0	Mask_OVP	R/W	1	1 : Mask OVP Interrupt

STATUS
Address: 05h
Reset Value: 0x0000_0000
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Description
7	LOOK4CC	R	1	1 : Device is monitoring moisture on CC1 or CC2
6	LOOK4SBU	R	1	1 : Device is monitoring moisture on SBU1 or SBU2 using float voltage detection
5	LOOK4DRY	R	1	1 : Monitoring Dry check on SBU1 and SBU2
3:2	NU	R	1	Do not use
1	OVP_SBU	R	1	1 : OVP conditions on SBU1 or SBU2
0	OVP_CC	R	1	1 : OVP conditions on CC1 or CC2

MOISTURE_STATUS
Address: 06h
Reset Value: 0x0000_0000
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Description
7:6	FAULT	R	2	These bits are set when moisture detection on SBU using volt-

SWITCH CONTROL

Address: 07h
Reset Value: 0x0000_0000
Type: Read / Write

2:1	SBU	R/W	2	00 : Open both SBU1 and SBU2 switches 01 : SBU1 and SBU2 close to SBU1_H and SBU2_H 10 : SBU2 closes to FM, SBU1, SBU1_H and SBU2_H are open 11 : SBU1 closes to FM, SBU2, SBU1_H and SBU2_H are open
0	CC	R/W	1	0 : CC1 and CC2 switch are open 1 : CC1 and CC2 close to CC1_H and CC2_H

THRESHOLD 1

Address: 08h
Reset Value: 0x1011_1011
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7:4	SBU_MOS_DET	R/W	4	0000 : 17 kΩ 0001 : 36 kΩ … 1011 : 480 k

TIMER

Address: 0Ah
Reset Value: 0x0000_0100
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7:3	NU	R	5	Do not use
2:0	TDRY	R/W	3	000 : 50 ms 001 : 100 ms 010 : 250 ms 011 : 1 sec 100 : 2 sec 101 : 4 sec 110 : 8 sec 111 : 10 sec

RESET

Address: 0Bh
Reset Value: 0x0000_0100
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7:2	NU	R	6	Do not use
1	MOS Reset	R/W/C	1	1 : Reset moisture detection state machine and clear moisture status, Read returns ‘0’. This register bit resets moisture detection state machine and moisture status register is cleared. Control register is not affected by this bit. If any moisture detection enable bit was set, moisture detection will restart by MOS Reset
0	Reset	R/W/C	1	1 : Reset the device, Read returns ‘0’ The Device Reset includes FM pin configuration so FM pin status is checked after this Reset

TIMER2

Address: 0Ch
Reset Value: 0x0000_0100
Type: Read / Write

Bit #	Name	R/W/C	Size (Bits)	Description
7:4	NU	R	4	Do not use
3:2	Number of ADC Read	R/W	2	00 : 1 time 01 : 2 times 10 : 3 timers 11 : Do not use(no change)
1:0	CC Settle time	R/W	2	**00 : 400 µs** 01 : 300 µs 10 : 500 µs 11 : 600 µs

APPLICATION CIRCUIT

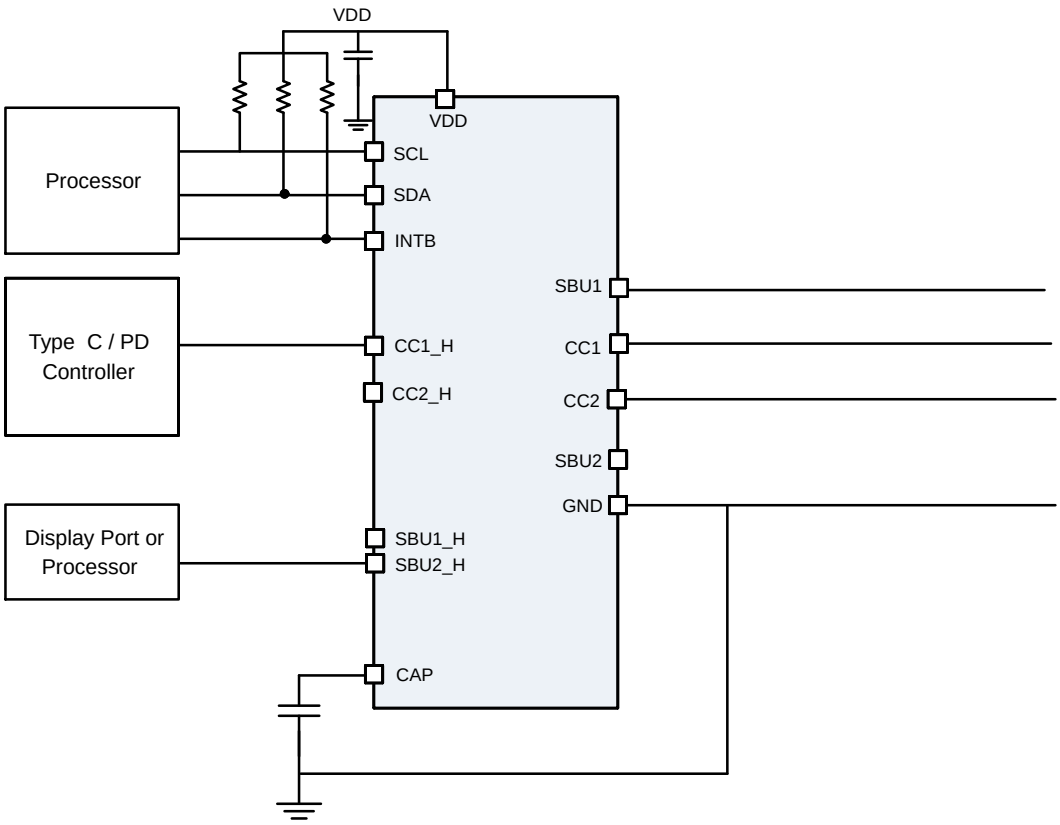
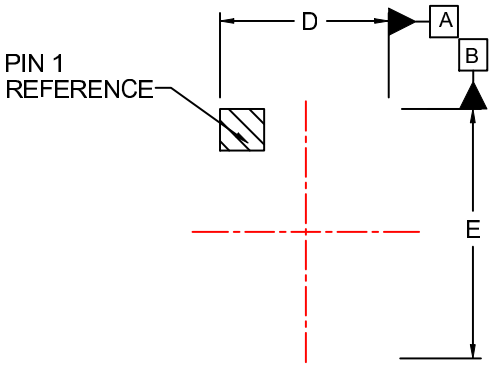


Figure 8. A

CASE 567WV
ISSUE O

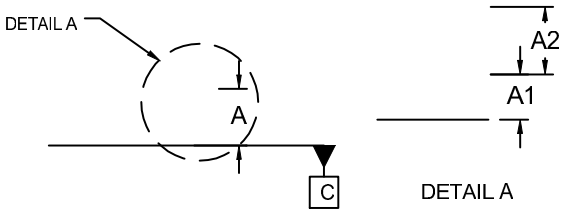
DATE 12 JUL 2018



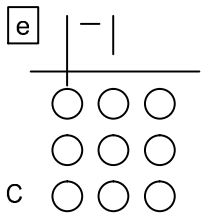
TOP VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS



SIDE VIEW



BOTTOM VIEW

RECOMMENDED
MOUNTING FOOTPRINT
(NSMD PAD TYPE)