TYPICAL APPLICATION

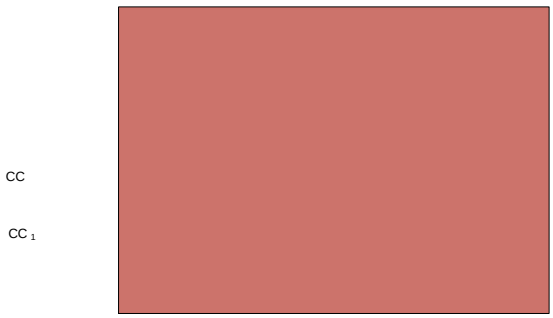


Figure 2. Typical Application

PIN CONFIGURATION

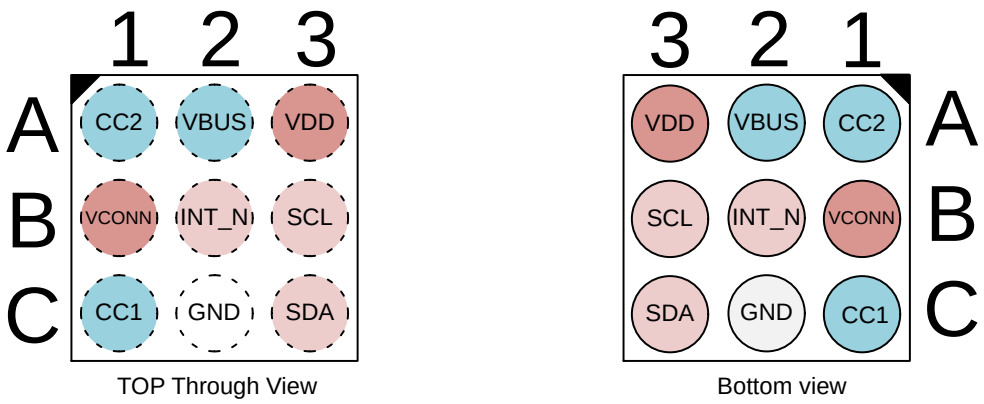


Figure 4. FUSB302BUCX Pin Assignment

Table 2. PIN MAP

	Column 1	Column 2	Column 3
Row A	CC2	VBUS	VDD
Row B	VCONN	INT_N	SCL
Row C	CC1	GND	SDA

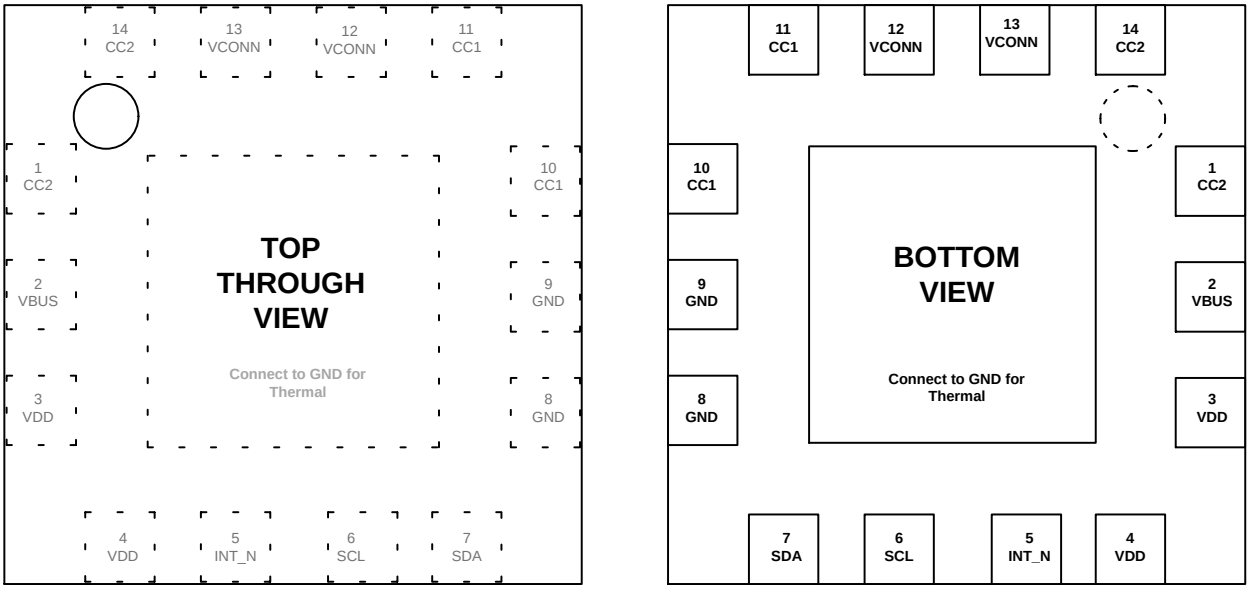


Figure 5. FUSB302BMPX Pin Assignment (N/C = No Connect)

Table 3. PIN DESCRIPTION

Name	Type	Description
USB TYPE-C CONNECTOR INTERFACE		
CC1/CC2	I/O	Type-C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation of the insertion is. Functionality after attach depends on mode of operation detected. Operating as a host: 1. Sets the allowable charging current for VBUS to be sensed by the attached device 2. Used to communicate with devices using USB BMC Power Delivery 3. Used to detect when a detach has occurred Operating as a device: 1. Indicates what the allowable sink current is from the attached host. Used to communicate with devices using USB BMC Power Delivery
GND	Ground	Ground
VBUS	Input	VBUS input pin for attach and detach detection when operating as an upstream facing port (Device). Expected to be an OVP protected input.
POWER INTERFACE		
VDD	Power	Input supply voltage.
VCONN		

CONFIGURATION CHANNEL SWITCH

The FUSB302B integrates the control and detection functionality required to implement a USB Type-C host, device or dual-role port including:

- Device Port Pull-Down (R_D)
- Host Port Pull-Up (I_P)
- VCONN Power Switch with OCP for Full-Featured USB3.1 Cables
-

Table 4. PROCESSOR CONFIGURES THE FUSB302B THROUGH I²C

I²C Registers/Bits	Value
TOGGLE	

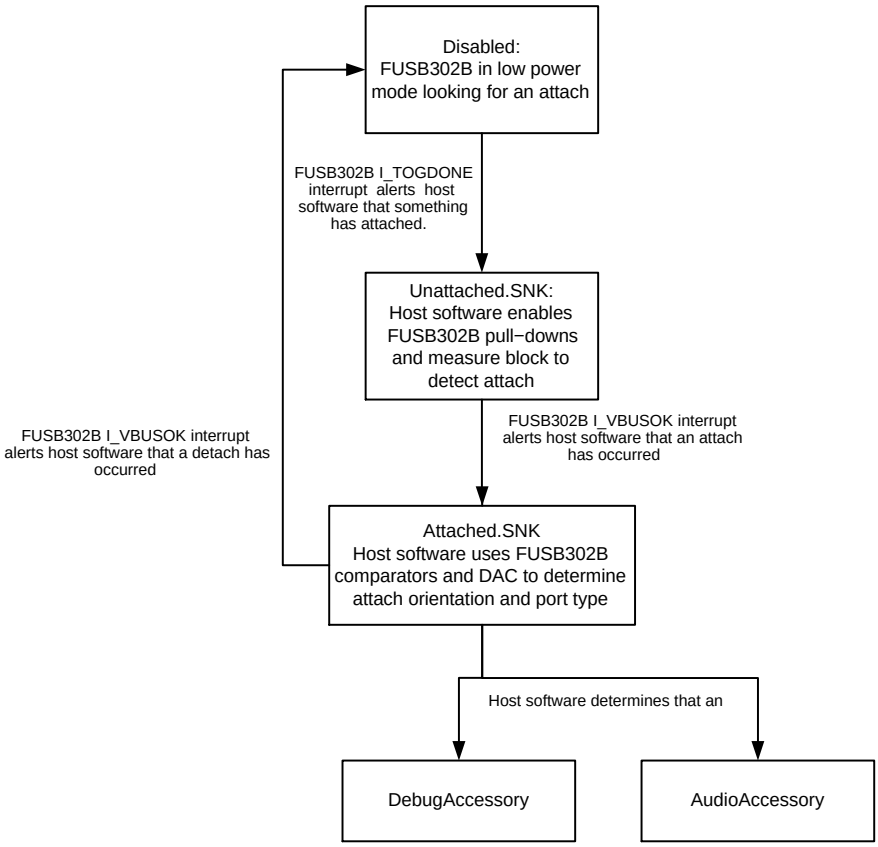


Figure 7. SNK Software Flow

CC

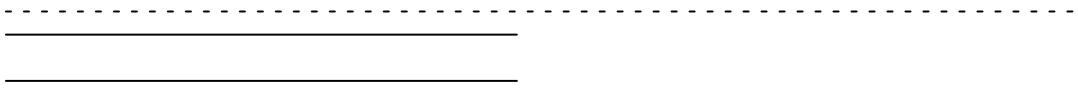


Figure 9. HOST_CUR Changed prior to Attach

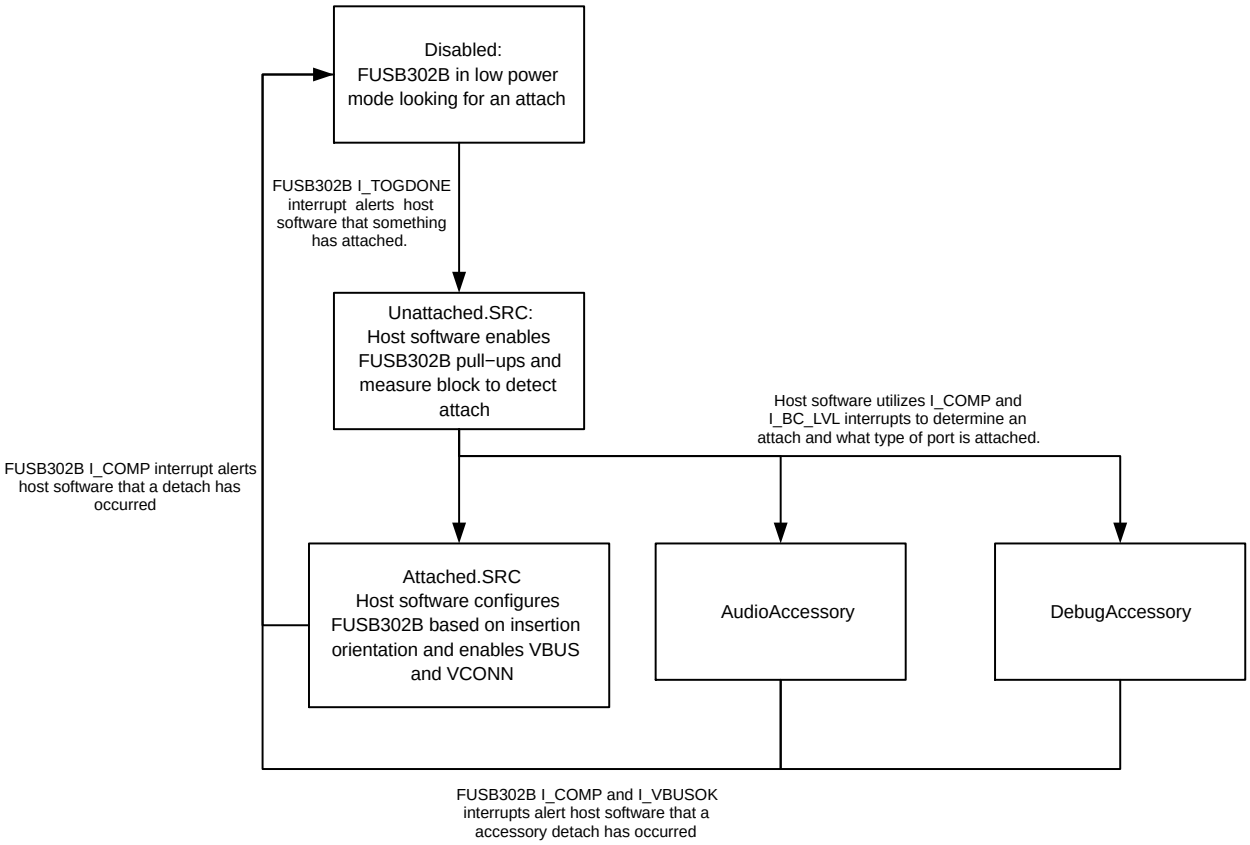


Figure 10. SRC Software Flow

Manual Dual-Role Detection and Configuration

The Type-C specification allows ports to be both a device and a host depending on what type of port has attached. This functionality is similar to USB OTG ports with the current USB connectors and is called a dual-role port. The FUSB302B can be used to implement a dual-role port. A Type-C dual role port toggles between presenting as a Type-C device and a Type-C host. The host software controls the toggle time and configuration of the FUSB302B in each state as shown in Figure 11.

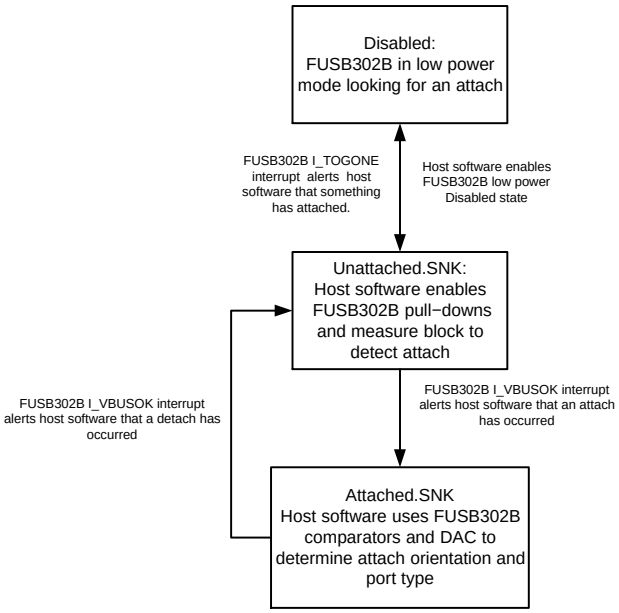


Figure 11. DRP Software Flow

BMC POWER DELIVERY

The Type-C connector allows USB Power Delivery (PD) to be communicated over the connected CC pin between two ports. The communication method is the BMC Power Delivery protocol and is used for many different reasons with the Type-C connector. Possible uses are outlined below.

- Negotiating and controlling charging power levels
- Alternative Interfaces such as MHL, Display Port
- Vendor specific interfaces for use with custom docks or accessories
- Role swap for dual-role ports that want to switch who is the host or device
- Communication with USB3.1 full featured cables

The FUSB302B integrates a thin BMC PD client which includes the BMC physical layer and packet FIFOs (48 bytes for transmit and 80 bytes for receive) which allows packets to be sent and received by the host software through I^2C accesses. The FUSB302B allows host software to implement all features of USB BMC PD through writes and reads of the FIFO and control of the FUSB302B physical interface.

The FUSB302B uses tokens to control the transmission of BMC PD packets. These tokens are written to the transmit FIFO and control how the packet is transmitted on the CC pin. The tokens are designed to be flexible and support all aspects of the USB PD specification. The FUSB302B additionally enables control of the BMC transmitter through tokens. The transmitter can be enabled or disabled by specific token writes which allow faster packet processing by burst writing the FIFO with all the information required to transmit a packet.

The FUSB302B receiver stores the received data and the received CRC in the receive FIFO when a valid packet is received on the CC pin. The BMC receiver automatically enables the internal oscillator when an Activity is sensed on the CC pin and load to the FIFO when a packet is received. The I_ACTIVITY and I_CRC_CHK interrupts alert the host software that a valid packet was received.

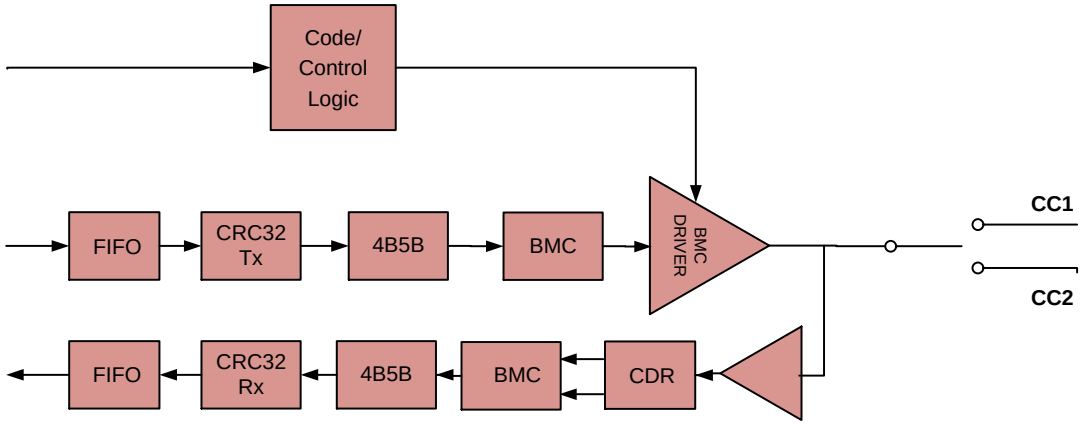


Figure 12. USB BMC Power Delivery Blocks

Power Level Determination

The Type-C specification outlines the order of precedence for power level determination which covers power levels from basic USB2.0 levels to the highest levels of USB PD. The host software is expected to follow the USB Type-C specification for charging current priority based on feedback from the FUSB302B detection, external BC1.2 detection and any USB Power Delivery communication.

The FUSB302B does not integrate BC1.2 charger detection which is assumed available in the USB transceiver or USB charger in the system.

Power Up, Initialization and Reset

When power is first applied through VDD, the FUSB302B is reset and registers are initialized to the default values shown in the register map.

The FUSB302B can be reset through software by programming the SW_RES bit in the RESET register.

The FUSB302B can be reset through software by

s

PD Send

The FUSB302B implements part of the PD protocol layer for sending packets in an autonomous fashion.

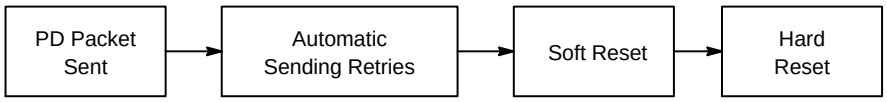


Figure 13.

PD Automatic Sending Retries

If GoodCRC packet is not received and AUTO_RETRY is set, then a retry of the same message that was in the TxFIFO written by the processor is executed within t_{Retry} and that is repeated for NRETRY times.

PD Send Soft Reset

If the correct GoodCRC packet is still not received for all retries then I_RETRYFAIL interrupt is triggered and if AUTO_SOFT_RESET is set, then a Soft Reset packet is created (MessageID is set to 0 and the processor upon servicing I_RETRYFAIL would set the true MessageIDCounter to 0.

If this Soft Reset is sent successfully where a GoodCRC control packet is received with a MessageID = 0 then I_TXSENT interrupt occurs.

If not, this Soft Reset packet is retried NRETRIES times (MessageID is always 0 for all retries) if a GoodCRC acknowledge packet is not received with CRCReceiveTimer expiring ($t_{Receive}$ of 1.1 ms max). If all retries fail, then I_SOFTFAIL interrupt is triggered.

PD Send Hard Reset

If all retries of the soft reset packet fail and if AUTO_HARD_RESET is set, then a hard reset ordered set is sent by loading up the TxFIFO with RESET1, RESET1, RESET1, RESET2 and sending a hard reset. Note only one hard reset is sent since the typical retry mechanism doesn't apply. The processor's policy engine firmware is responsible for retrying the hard reset if it doesn't receive the required response.

Flush Rx-FIFO with BIST (Built-In Self Test) Test Data

During PD compliance testing, BIST test packets are used

reCRe,

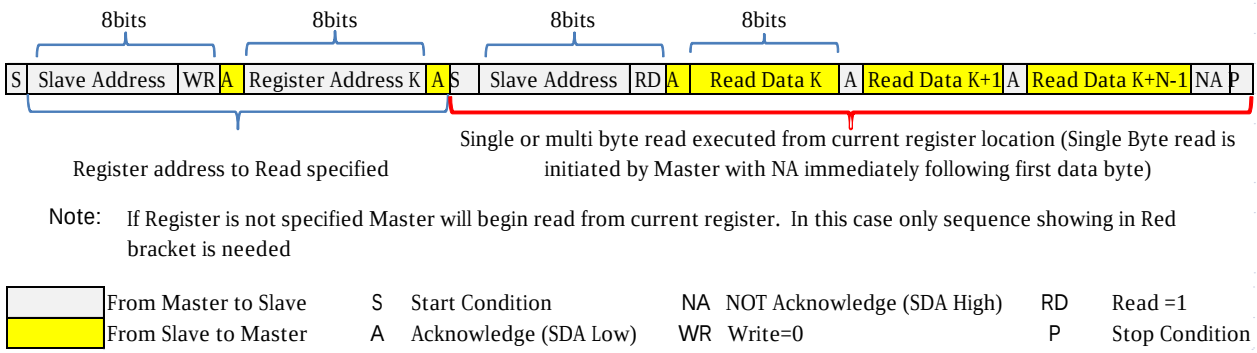


Figure 15. I²C Read Example

Table 7. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
Vv_{DD}	Supply Voltage from V_{DD}	−0.5	6.0	V
V_{CC_HDDRP}	CC pins when configured as Host, Device or Dual Role Port	−0.5	6.0	V

$V_{VBUSHost, Device ordjET59.754 514.602 .68033 154 513.921 59.754 .6803 ref mf(NOT Acko29.228 60.435 .6803 refB8 W 8 394.9228 511.84)m3.406 l-14592 60.435 .6803 refB13.9}$

DC AND TRANSIENT CHARACTERISTICS

All typical values are at T_A = 25°C unless otherwise specified.

Table 9. BASEBAND PD

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
UI	Unit Interval	3.03	−	3.70	μs
TRANSMITTER					
zDriver	Transmitter Output Impedance	33	−	75	Ω
$t_{EndDriveBMC}$	Time to Cease Driving the Line after the end of the last bit of the Frame	−	−	23	μs
$t_{HoldLowBMC}$	Time to Cease Driving the Line after the final High-to-Low Transition	1	−	−	μs
V_{OH}	Logic High Voltage	1.05	−	1.20	V
V_{OL}	Logic Low Voltage	0	−	75	mV
$t_{StartDrive}$	Time before the start of the first bit of the preamble when the transmitter shall start driving the line	−1	−	1	μs
t_{RISE_TX}	Rise Time	300	−	−	ns
t_{FALL_TX}	Fall Time	300	−	−	ns
RECEIVER					
cReceiver	Receiver Capacitance when Driver isn't Turned On	−	50	−	pF
zBmcRx	Receiver Input Impedance	1	−	−	MΩ
tRxFilter	Rx Bandwidth Limiting Filter (Note 4)	100	−	−	ns

4. Guaranteed by Characterization and/or Design. Not production tested.

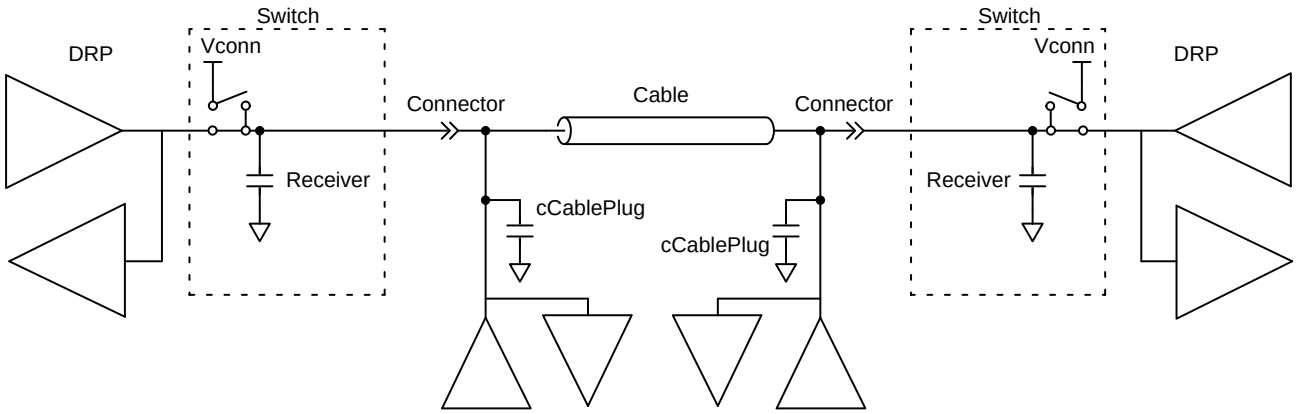


Figure 16. Transmitter Test Load

Table 10. TYPE-C CC SWITCH

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
R					

Table 11. CURRENT CONSUMPTION

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
				Min	Typ	Max	
Idisable	Disabled Current	3.0 to 5.5	Nothing Attached, No I^2C Transactions	−	0.37	5.0	μA
Idisable	Disabled Current (Note 11)	3.0 to 5.5	Nothing Attached, No I^2C Transactions	−	0.37	8.5	μA
Itog	Unattached (standby) Toggle Current	3.0 to 5.5	Nothing attached, TOGGLE = 1, PWR[3:0] = 1h, WAKE_EN = 0, TOG_SAVE_PWR2:1 = 01	−	25	40	μA
Ipd_stby_meas	BMC PD Standby Current	3.0 to 5.5	Device Attached, BMC PD Active But Not Sending or Receiving Anything, PWR[3:0] = 7h	−	40	−	μA

Table 12. USB PD SPECIFIC PARAMETERS

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
tHardReset	If a Soft Reset message fails, a Hard Reset is sent after tHardReset of CRCReceiveTimer expiring	−	−	5	ms
tHardReset Complete	If the FUSB302B cannot send a Hard Reset within tHardResetComplete time because of a busy line, then a I_HARDFAIL interrupt is triggered	−	−	5	ms
tReceive	This is the value for which the CRCReceiveTimer expires. The CRCReceiveTimer is started upon the last bit of the EOP of the transmitted packet	0.9	−	1.1	ms
tRetry	Once the CRCReceiveTimer expires, a retry packet has to be sent out within tRetry time. This time is hard to separate externally from tReceive since they both happen sequentially with no visible difference in the CC output	−	−	75	μs
tSoftReset	If a GoodCRC packet is not received within tReceive for NRETRIES then a Soft Reset packet is sent within tSoftReset time.	−	−	5	ms
tTransmit	From receiving a packet, we have to send a GoodCRC in response within tTransmit time. It is measured from the last bit of the EOP of the received packet to the first bit sent of the preamble of the GoodCRC packet	−	−	195	μs

Table 13. IO SPECIFICATIONS

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
				Min	Typ	Max	
HOST INTERFACE PINS (INT_N)							
V_{OLINTN}	Output Low Voltage	3.0 to 5.5	I_{OL} = 4 mA	−	−	0.4	V
T_{INT_Mask}	Time from global interrupt mask bit cleared to when INT_N goes LOW	3.0 to 5.5		50	−	−	μs
I^2C INTERFACE PINS – STANDARD, FAST, OR FAST MODE PLUS SPEED MODE (SDA, SCL) (Note 6)							
V_{ILI2C}	Low-Level Input Voltage	3.0 to 5.5		−	−	0.51	V
V_{IHI2C}	High-Level Input Voltage	3.0 to 5.5		1.32	−	−	V

Table 13. IO SPECIFICATIONS

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
				Min	Typ	Max	
I²C INTERFACE PINS – STANDARD, FAST, OR FAST MODE PLUS SPEED MODE (SDA, SCL) (Note 6)							
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	3.0 to 5.5		94	–	–	mV
I_{I2C}	Input Current of SDA and SCL Pins	3.0 to 5.5	Input Voltage 0.26 V to 2.0 V	−10	–	10	μA
I_{CCTI2C}	VDD Current when SDA or SCL is HIGH	3.0 to 5.5	Input Voltage 1.8 V	−10	–	10	μA
V_{OLSDA}	Low-Level Output Voltage (Open-Drain)	3.0 to 5.5	I_{OL} = 2 mA	0	–	0.35	V
I_{OLSDA}	Low-Level Output Current (Open-Drain)	3.0 to 5.5	V_{OLSDA} = 0.4 V	20	–	–	mA
C_I	Capacitance for Each I/O Pin (Note 7)	3.0 to 5.5		–	5	–	pF

6. I²C pull up voltage is required to be between 1.71 V and V_{DD}.

Table 14. I²C SPECIFICATIONS FAST MODE PLUS I²C SPECIFICATIONS

Symbol	Parameter	Fast Mode Plus		Unit
		Min	Max	
f_{SCL}	I2C_SCL Clock Frequency	0	1000	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.26	–	μs
t_{LOW}	Low Period of I2C_SCL Clock	0.5	–	μs
t_{HIGH}	High Period of I2C_SCL Clock	0.26	–	μs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.26	–	μs
$t_{HD;DAT}$	Data Hold Time	0	–	μs
$t_{SU;DAT}$	Data Set-up Time	50	–	ns
t_r	Rise Time of I2C_SDA and I2C_SCL Signals (Note 7)	–	120	ns
t_f	Fall Time of I2C_SDA and I2C_SCL Signals (Note 7)	6		

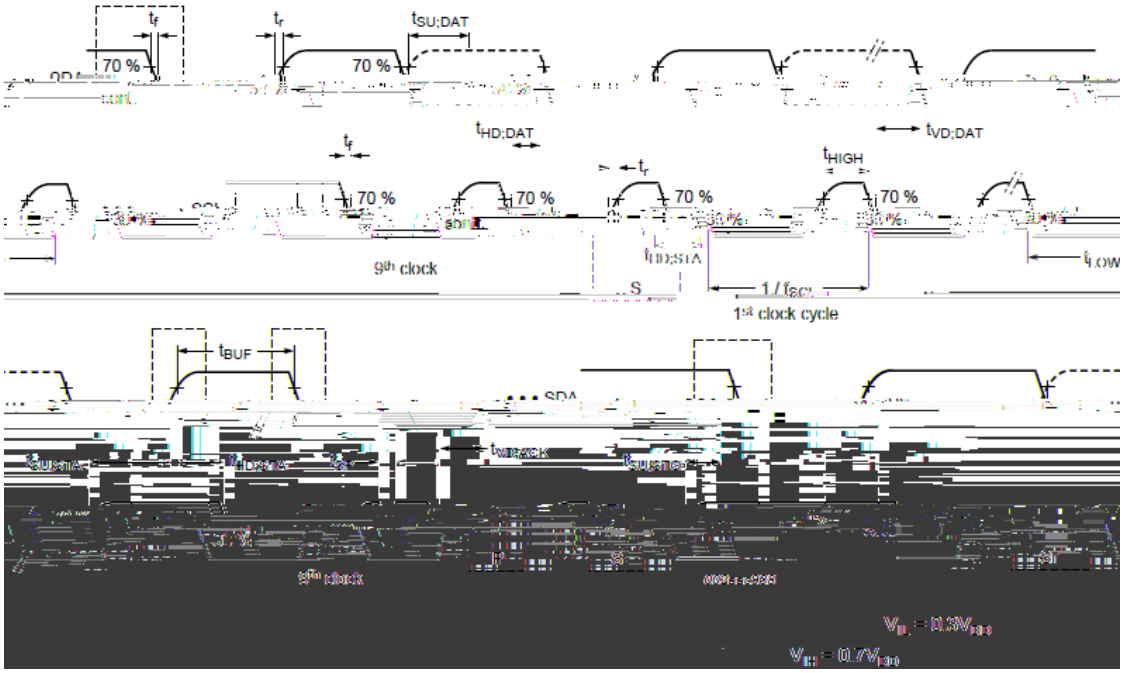


Figure 17. Definition of Timing for Full-Speed Mode Devices on the I²C Bus

Table 15. I²C SLAVE ADDRESS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FUSB302BUCX, FUSB302BMPX, FUSB302BVMPX	0	1	0	0	0	1	0	R/W
FUSB302B01MPX	0	1	0	0	0	1	1	R/W
FUSB302B10MPX	0	1	0	0	1	0	0	R/W
FUSB302B11MPX	0	1	0	0	1	0	1	R/W

Table 16. REGISTER DEFINITIONS

Table 18. SWITCHES0

(Address: 02h; Reset Value: 0x0000_0011; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7	PU_EN2	R/W	1	1: Apply host pull up current to CC2 pin
6	PU_EN1	R/W	1	1: Apply host pull up current to CC1 pin
5	VCONN_CC2	R/W	1	1: Turn on the VCONN current to CC2 pin
4	VCONN_CC1	R/W	1	1: Turn on the VCONN current to CC1 pin
3	MEAS_CC2	R/W	1	1: Use the measure block to monitor or measure the voltage on CC2
2	MEAS_CC1	R/W	1	1: Use the measure block to monitor or measure the voltage on CC1
1	PDWN2	R/W	1	1: Device pull down on CC2. 0: no pull down
0	PDWN1	R/W	1	1: Device pull down on CC1. 0: no pull down

Table 19. SWITCHES1

(Address: 03h; Reset Value: 0x0010_0000; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7	POWERROLE	R/W	1	Bit used for constructing the GoodCRC acknowledge packet. This bit corresponds to the Port Power Role bit in the message header if an SOP packet is received: 1: Source if SOP **0: Sink if SOP**
6:5	SPECREV1: SPECREV0	R/W	2	Bit used for constructing the GoodCRC acknowledge packet. These bits correspond to the Specification Revision bits in the message header: 00: Revision 1.0 **01: Revision 2.0** 10: Do Not Use 11: Do Not Use
4	DATAROLE	R/W	1	Bit used for constructing the GoodCRC acknowledge packet. This bit corresponds to the Port Data Role bit in the message header. For SOP: 1: SRC **0: SNK**
3	Reserved	N/A	1	Do Not Use
2	AUTO_CRC	R/W	1	1: Starts the transmitter automatically when a message with a good CRC is received and automatically sends a GoodCRC acknowledge packet back to the relevant SOP* **0: Feature disabled**
1	TXCC2	R/W	1	1: Enable BMC transmit driver on CC2 pin
0	TXCC1	R/W	1	1: Enable BMC transmit driver on CC1 pin

Table 20. MEASURE
(Address: 04h; ·Reset Value: 0x0011_0001; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7	Reserved	N/A	1	Do Not Use
6	MEAS_VBUS	R/W	1	0: MDAC/comparator measurement is controlled by MEAS_CC* bits 1: Measure VBUS with the MDAC/comparator. This requires MEAS_CC* bits to be 0
5:0	MDAC[5:0]	R/W	6	Measure Block DAC data input. LSB is equivalent to 42 mV of voltage which is compared to the measured CC voltage. The measured CC is selected by MEAS_CC2, or MEAS_CC1 bits. MDAC[5:0] MEAS_VBUS = 0 MEAS_VBUS = 1 Unit 00_0000 0.042 0.420 V 00_0001 0.084 0.840 V 11_0000 2.058 20.58 V 11_0011 2.184 21.84 V 11_1110 2.646 26.46 V 11_1111 > 2.688 26.88 V

Table 21. SLICE
(Address: 05h; Reset Value: 0x0110_0000; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7:6	SDAC_HYS[1:0]	R/W	2	Adds hysteresis where there are now two thresholds, the *lower threshold which is always the value programmed by SDAC[5:0]* and the higher threshold that is: 11: 255 mV hysteresis: higher threshold = (SDAC value + 20hex) 10: 170 mV hysteresis: higher threshold = (SDAC value + Ahex) 01: 85 mV hysteresis: higher threshold = (SDAC value + 5) 00: No hysteresis: higher threshold = SDAC value
5:0	SDAC[5:0]	R/W	6	BMC Slicer DAC data input. Allows for a programmable threshold so as to meet the BMC receive mask under all noise conditions.

Table 22. CONTROL0
(Address: 06h; Reset Value: 0x0010_0100; Type: (see column below))

Bit #	Name	R/W/C	Size (Bits)	Description
7	Reserved	N/A	1	Do Not Use
6	TX_FLUSH	W/C	1	1: Self clearing bit to flush the content of the transmit FIFO
5	INT_MASK	R/W	1	1: Mask all interrupts 0: Interrupts to host are enabled
4				

Table 23. CONTROL1
(Address: 07h; Reset Value: 0x0000_0000; Type: (see column below))

Bit #	Name	R/W/C	Size (Bits)	Description
7				

Table 25. CONTORL3

(Address: 09h; Reset Value: 0x0000_0110; Type: (see column below))

Bit #	Name	R/W/C	Size (Bits)	Description
7	Reserved	N/A	1	Do Not Use
6	SEND_HARD_RESET	W/C	1	1: Send a hard reset packet (highest priority) **0: Don’t send a soft reset packet**
5	BIST_TMODE	R/W	1	1: BIST mode. Receive FIFO is cleared immediately after sending GoodCRC response 0: Normal operation, All packets are treated as usual
4				

Table 35. INTERRUPTA

(Address: 3Eh; Reset Value: 0x0000_0000; Type: Read/Clear)

Bit #	Name	R/W/C	Size (Bits)	Description
7	I_OCP_TEMP	R/C	1	1: Interrupt from either a OCP event on one of the VCONN switches or an over-temperature event
6	I_TOGDONE	R/C	1	1: Interrupt indicating the TOGGLE functionality was terminated because a device was detected
5				

Table 39. INTERRUPT
(Address: 42h; Reset Value: 0x0000_0000; Type: Read/Clear)

Bit #	Name	R/W/C	Size (Bits)	Description
7	I_VBUSOK	R/C	1	1: Interrupt occurs when VBUS transitions through 4.5 V. This bit typically is used to recognize port partner during startup
6	I_ACTIVITY	R/C	1	1: A change in the value of ACTIVITY of the CC bus has occurred
5	I_COMP_CHNG	R/C	1	1: A change in the value of COMP has occurred. Indicates selected CC line has tripped a threshold programmed into the MDAC
4	I_CRC_CHK	R/C	1	1: The value of CRC_CHK newly valid. I.e. The validity of the incoming packet has been checked
3	I_ALERT	R/C	1	1: Alert software an error condition has occurred. An alert is caused by: TX_FULL: the transmit FIFO is full RX_FULL: the receive FIFO is full See **Status1** bits
2	I_WAKE	R/C	1	1: Voltage on CC indicated a device attempting to attach. Software must then power up the clock and receiver blocks
1	I_COLLISION	R/C	1	1: When a transmit was attempted, activity was detected on the active CC line. Transmit is not done. The packet is received normally
0	I_BC_LVL	R/C	1	1: A change in host requested current level has occurred

Table 40. FIFOS
(Address: 43h; Reset Value: 0x0000_0000; Type: (see column below))

Bit #	Name	R/W/C	Size (Bits)

REFERENCE SCHEMATIC

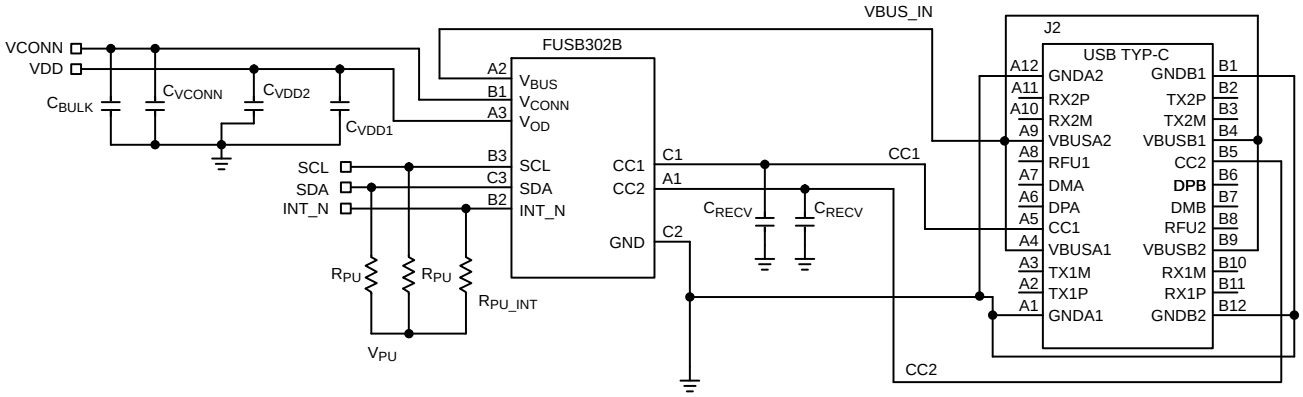


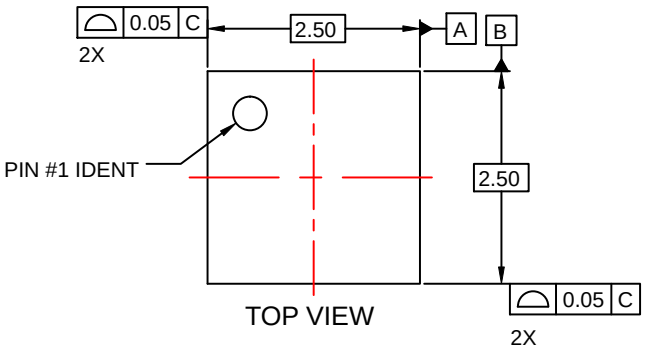
Figure 18. FUSB302/FUSB302B Reference Schematic Diagram

Table 43. RECOMMENDED COMPONENT VALUES FOR REFERENCE SCHEMATIC

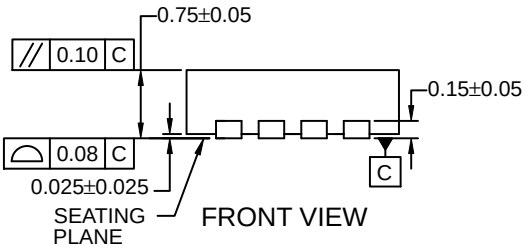
Symbol	Parameter	Recommended Value		Unit
		Min		

WQFN14 2.5x2.5, 0.5P
CASE 510BR
ISSUE O

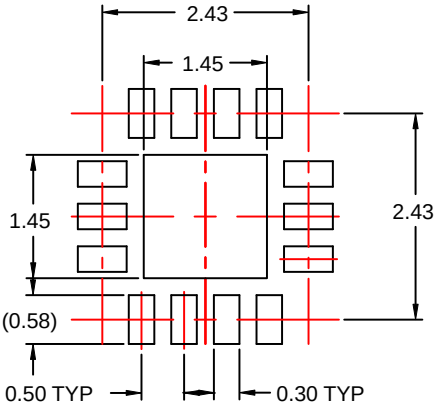
DATE 31 AUG 2016



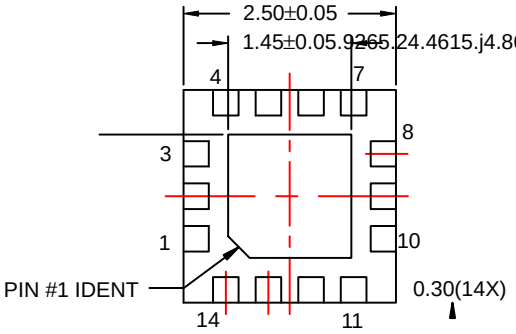
TOP VIEW



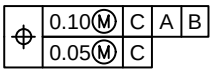
FRONT VIEW



RECOMMENDED LAND PATTERN



BOTTOM VIEW



NOTES:

A. NO JEDEC REGISTRATION.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

WLCSP9 1.26x1.215x0.526
CASE 567TN
ISSUE O

DATE 31 MAR 2017