



QFN12  
CASE 722AG



**MARKING DIAGRAM**

**Description**

The FUSB303B device is a fully autonomous USB Type-C™ controller optimized for 15 W or less applications. The FUSB303B offers CC logic detection for source or sink in USB3.0/USB3.1/USB3.2/USB4.0/USB-C™.

UN	= FUSB303B Device Code
KK	= Lot Trace Code
–	= Pin #1 Identifier
XY	= Two Digit Date Code
Z	= Assembly Plant Code

- ✓ Dead Battery Support (Sink Port role when No Power Applied)
- ✓ 4 kV HBM ESD Protection for Connector Pins
- ✓ Small Packaging, 12 Lead QFN  
(1.6 mm x 1.6 mm x 0.375 mm)

**Applications**

- ✓ Smartphones
- ✓ Tablets
- ✓ Laptops
- ✓ Accessoires
- ✓ Industrial
- ✓ Power Banks



# FUSB303B

## BLOCK DIAGRAM

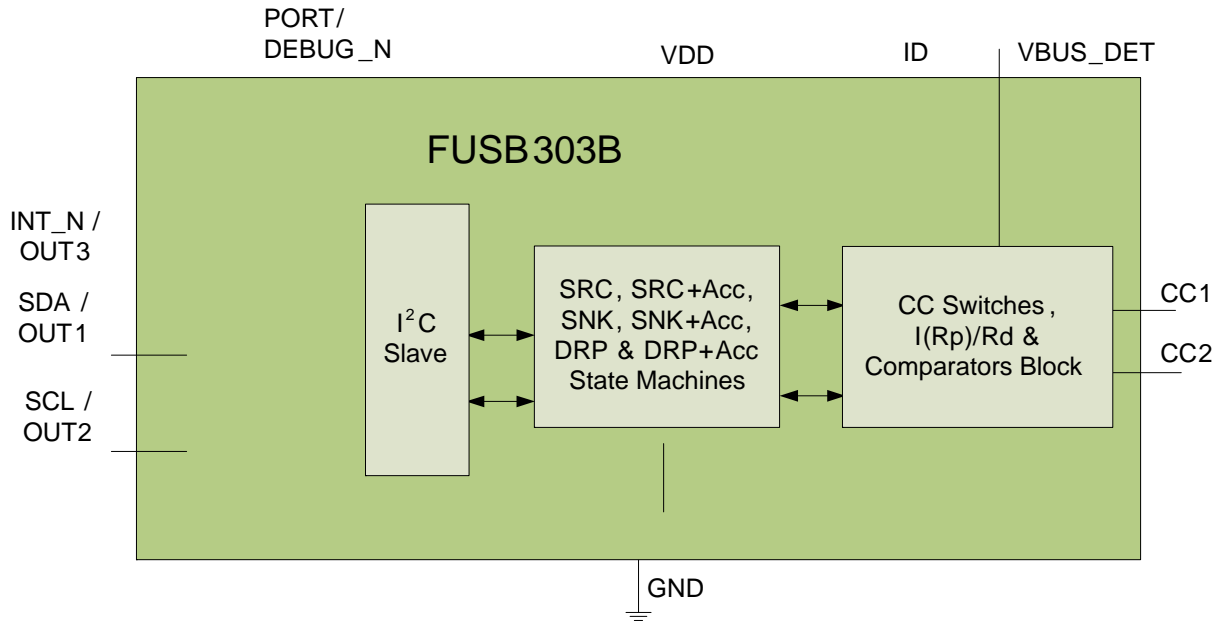


Figure 3. FUSB303B Block Diagram

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## PIN DESCRIPTIONS

Table 1. PIN DESCRIPTIONS

Pin #	Name	Type	Description
<b>USB TYPE-C CONNECTOR INTERFACE</b>			
1, 2	CC1, CC2	I/O	Type-C Configuration Channel pins used for USB-C receptacles
4	VBUS_DET	Input	VBUS input pin for attach and detach detection
<b>POWER AND GROUND</b>			
10	GND	Ground	Ground
12	VDD	Power	Input Supply Voltage
<b>I<sup>2</sup>C SIGNAL INTERFACE</b>			
6	INT_N/OUT3	Open-Drain Output	INT_N/OUT3 is a dual function pin. When in I <sup>2</sup> C mode (see ADDR/ORIENT pin), it is the active LOW open drain interrupt output used to prompt the processor to read the I <sup>2</sup> C

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**Table 2. ORIENT PIN VERSUS ORIENT [1:0] REGISTER BITS MAPPING**

CC1 (A5)	CC2 (B5)	STATUS. ORIENT[1] Bit	STATUS. ORIENT[0] Bit	ADDR/ORIENT pin Output
<b>FUSB303B CONNECTED AS A SINK</b>				
SNK. Open	SNK. Open	0	0	LOW
SNK. Open	SNK. Rp	1	0	HIGH
SNK. Rp	SNK. Open	0	1	LOW
SNK. Rp (Note 2)	SNK. Rp	0	1	LOW
SNK. Rp	SNK. Rp (Note 2)	1	0	HIGH
<b>FUSB303B CONNECTED AS SOURCE</b>				
SRC. Open	SRC. Open	0	0	LOW
SRC. Open or SRC. Ra	SRC. Rd	1	0	HIGH
SRC. Rd	SRC. Open or SRC. Ra	0	1	LOW
SRC. Rd (Note 1)	SRC. Rd	0	1	LOW
SRC. Rd	SRC. Rd (Note 1)	1	0	HIGH

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to a stable attached state. This functionality can be turned on

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## I<sup>2</sup>C Address

The ADDR/ORIENT bit HIGH or LOW is indicated in bit 5 of the slave address shown in Table 3.

### Table 3. FUSB303B I<sup>2</sup>C SLAVE

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**Table 6. DC AND TRANSIENT CHARACTERISTICS**

(Unless otherwise specified: Recommended  $T_A$  and  $T_J$  temperature ranges. All typical values are at  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.)

Symbol	Parameter	$T_A = -40\text{ to }+85^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	Unit
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**Table 7. CURRENT CONSUMPTION**

Symbol	Parameter	VDD (V)	Conditions	TA = -40 to +85°C TJ=-40 to +125°C			Unit
				Min.	Typ.	Max.	
I <sub>disable</sub>	Disabled Current	2.85 to 4.35	Disabled State EN N = HIGH or not connected			5	μA
I <sub>stby</sub>	Unattached Sink (3.3 V I <sup>2</sup> C mode without AUTOSNK or accessories)	2.85 to 4.35	Nothing 252 640.74SJET99.78 14.926 .90709 ected				

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**Table 9. TIMING PARAMETERS** (continued)

Symbol	Parameter		T <sub>A</sub> = -40 to +85°C T <sub>J</sub> = -40 to +125°C			Unit
			Min.	Typ.	Max.	Unit
tRESET	Soft Reset Duration	2.85 to 5.5			100	ms
tAUTOSNK	Debounce time to detect Weak Battery VDD Threshold to trigger I_AUTOSNK if AUTOSNK mode enabled for both entering AUTOSNK and exiting AUTOSNK V <sub>DD</sub> (V) = 2.85 to 5.5		10	15	20	ms

4. Default Value when Configured in GPIO Mode (ADDR/ORIENT = Float)

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**Table 10. FAST MODE I<sup>2</sup>C TIMING SPECIFICATIONS** (see Figure 7)

Symbol	Parameter	Fast Mode		
		Min.	Max.	Unit
f <sub>SCL</sub>	SCL/OUT2 Clock Frequency		400	kHz
t <sub>HD;STA</sub>	Hold Time (Repeated) START Condition	0.6		μs
t <sub>LOW</sub>	Low Period of SCL/OUT2 Clock	1.3		μs
t <sub>HIGH</sub>	High Period of SCL/OUT2 Clock	0.6		μs
t <sub>SU;STA</sub>	Set-up Time for Repeated START Condition	0.6		μs
t <sub>HD;DAT</sub>	Data Hold Time		0.9	μs
t <sub>SU;DAT</sub>	Data Set-up Time (Note 5)	100		ns
t <sub>r</sub>	Rise Time of SDA/OUT1 and SCL/OUT2 Signals (Note 6)	20. (V <sub>DD</sub> /5.5 V)	250	ns
t <sub>f</sub>	Fall Time of SDA/OUT1 and SCL/OUT2 Signals (Note 6)			

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## REGISTER DEFINITIONS

**Table 11. REGISTER MAP**

Address	Register Name	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	Reserved	N/A	N/A	Do Not Use							
01h	Device ID	R	10h	VER_ID[3:0]				REV_ID[3:0]			
02h	Device Type	R	03h	DEVICE_TYPE[7:0]							
03h	Portrole	R/W	4nh (see below)		ORIENTD EB	TRY[1:0]		AUDIOAC C	DRP	SNK	SRC
04h	Control	R/W	43h	T_DRP		DRPTOGGLE[1:0]		DCABLE_ EN	HOST_CUR[1:0]		INT_MAS K
05h	Control1	R/W	23h	REMEDY_ EN	AUTO_SNK_TH[1:0]		AUTO_SN K_EN	ENABLE	TCCDEB[2:0]		
06h-08h	Reserved	N/A	N/A	Do Not Use							
09h	Manual	W/C & R/W	00h			FORCE_S RC	FORCE_S NK	UNATT_S NK	UNATT_S RC	DISABLE D	ERROR_ REC
0Ah	Reset	W/C	00h								

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**Table 13. DEVICE TYPE** (Address: 02h, Type: Read Only)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7:0	DEVICE_TYPE[7:0]	8	7:0 03h	03h: FUSB303B

**Table 14. PORTROLE** (See Note 9)

(Address: 03h, Reset Value: 0100\_1nnnb (Reset value for bits nnn will be set by the state of the PORT/DEBUG\_N pin either during power up when EN\_N is LOW or when Vdd is valid and EN\_N goes HIGH to LOW) or when SW\_RES is set HIGH. In dead battery mode, nnn = 010 or configured as SNK) Type: Read/Write)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7	Reserved	1	7 0b	Do Not Use
6	ORIENTDEB	1	6 1b	1: When a Debug Accessory is found, continue to orientation detection if CC is on CC1 or CC2 (result is in Status.Orient[1:0])
5:4	TRY[1:0]	2	5:4 00b	00: Disable (normal DRP detection for DRPs) 01: Enable Try.SNK state machine detection for DRP only 10: Enable Try.SRC state machine detection for DRP only 11: Disable (cannot have Try.SNK and Try.SRC active together)
3				



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**Table 19. MASK**

(Address: 0Eh, Reset Value: 0000\_0000b, Type: Read/Write)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7	Reserved	1	7 0b	Do Not Use
6				

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**Table 22. STATUS1**

(Address: 12h, Reset Value: 0000\_0000b, Type: Read Only)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7:2	Reserved	6	7:2 00h	Do Not Use
1	FAULT	1	1 0b	1: Status to indicate that as a Sink, CC has exceed the normal vRd voltage range
0	REMEDY	1	0 0b	1: Status to indicate that FUSB303B is employing internal methods to achieve a stable attach

**Table 23. TYPE**

(Address: 13h, Reset Value: 0000\_0000b, Type: Read Only)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7	Reserved	1	7 0b	Do Not Use
6	DEBUGSRC	1	6 0b	1: FUSB303B is attached as a Source Debug Accessory ([Unoriented/Oriented]DebugAccessory.SRC)
5	DEBUGSNK	1	5 0b	1: FUSB303B is attached as a Sink Debug Accessory (DebugAccessory.SNK)
4	SINK	1	4 0b	1: FUSB303B is attached as a Sink (Attached.SNK)
3	SOURCE	1	3 0b	1: FUSB303B is attached as a Source (Attached.SRC)
2	ACTIVECABLE	1	2 0b	1: FUSB303B is attached to an Active Cable (Ra detected)
1	AUDIOVBUS	1	1 0b	1: Indicates an Audio Accessory mSource Deh ETceed been42.306 .9Ce. recsa.515

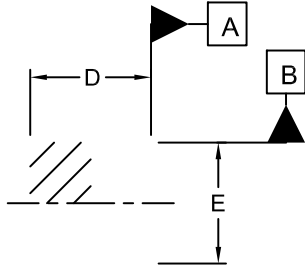




X2QFN12 1.6x1.6, 0.4P  
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PIN ONE  
REFERENCE



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