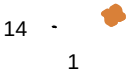
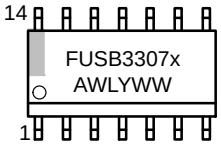
USB Power Delivery 3.0 Adaptive Source Charging Controller

FUSB3307



FUSB3307 is a highly integrated USB Power Delivery (PD) power source controller that can control a DC-DC port power regulator or the opto-coupler in the secondary side of an AC-DC adapter. It implements the Source finite state machines of USB Power Delivery 3.0 (PD 3.0) and Type-C™ which includes Programmable Power Supplies (PPS). In order to meet the PPS specification, FUSB3307 supports minimum 3.3 V and maximum 21 V output voltage control. It includes Constant Voltage (Cp < 0 Tc <00ef>Tj /TTB7r9rcm0 to meecrts L' includ includes Constan . 3Cn7C0TsV outpute



FUSB3307x = Specific Device Code

APPLICATION DIAGRAM

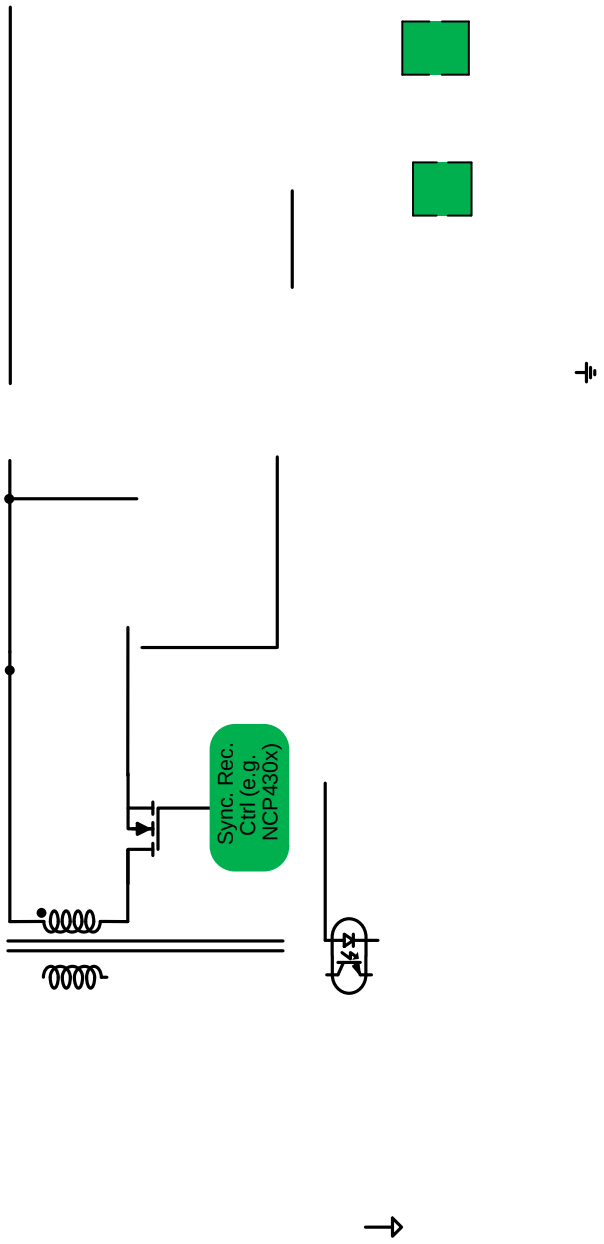


Figure 1. Offline Application Diagram

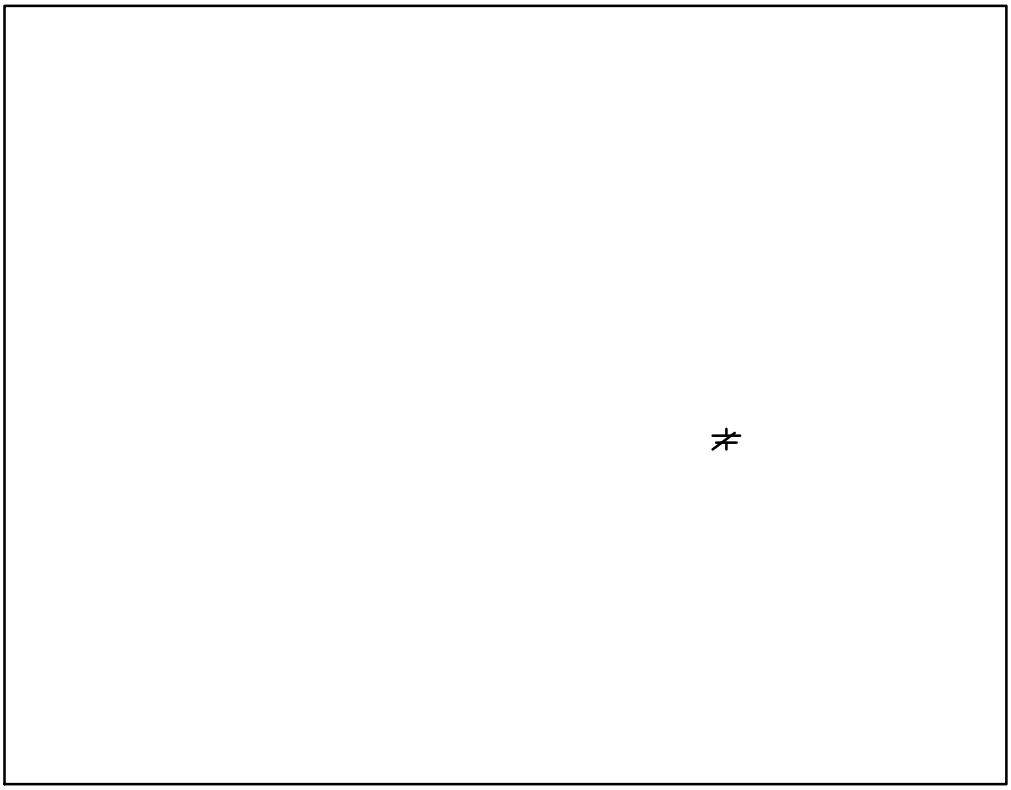


Figure 3. Block Diagram

PIN FUNCTION DESCRIPTION

SOIC Pin Number	QFN Pin Number	Pin Name	I/O Type	Description
1	14	VCC	Supply	Output voltage (Input voltage to the FUSB3307). This pin is tied to the output of the power source to monitor its output voltage and supply internal bias to the FUSB3307 via the VDD pin.
4	19	VDD	Supply	Internal supply voltage regulator output. This pin should be connected to an 1 F external capacitor
2	4, 15, DAP	GND		

ORDERING INFORMATION

Part Number

Table 4. ELECTRICAL CHARACTERISTICS V_{CC} = 5 V, T_J = ï40°C to 125°C unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VCC SECTION						

Table 4. ELECTRICAL CHARACTERISTICS V_{CC} = 5 V, T_J = ï40°C to 125°C unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CONSTANT VOLTAGE SENSING SECTION						
VFB Reference Voltage at 5.0 V (Power ïon reset, default)	V_{CC} = 5.0 V, V_{CS} = 0 V	$V_{CVR\ ï5.0V}$	0.485	0.500	0.515	V
VFB Reference Voltage at 9 V	V_{CC} = 9 V, V_{CS} = 0 V	$V_{CVR\ ï9V}$	0.873	0.900	0.927	V
VFB Reference Voltage at 12 V	V_{CC} = 12 V, V_{CS} = 0 V	$V_{CVR\ ï12V}$	1.164	1.200	1.236	V
VFB Reference Voltage at 15 V	V_{CC} = 15 V, V_{CS} = 0 V	$V_{CVR\ ï15V}$	1.455	1.500	1.545	V
VFB Reference Voltage at 20 V	V_{CC} = 20 V, V_{CS} = 0 V	$V_{CVR\ ï20V}$	1.940	2.000	2.060	V
VFB Reference Voltage of 20 mV step	V_{CC} = 20 mV, V_{CS} = 0 V	$V_{CVR\ ïSTEP\ ï20mV}$	1.940	2.000	2.060	mV
FEEDBACK SECTION						
CATH Pin Sink Current	Minimum guaranteed sink current expected from CATH pin	$I_{CATH\ ïSink}$	2			mA
DISCHARGE SECTION						
VBUS to GND leakage resistance when VBUS is not being sourced	GATE = 0 V	$R_{DISC\ ïBUS}$	72.4	155		k
VCC Pin Sink Current when discharging (Note 5)	Discharging current on VCC after a fault has trif 0 0 8j 0 -1.226.148 504.6804N.928 Ux. -.0004 Trif 0 0 .0019 T4 0 8 64.8 504.6804 Tm -.0015 Tc (					

Application Information

FUSB3307 has the entire PD Device Policy Manager (DPM), PD Policy Engine, Protocol and PHY layers within hardware and it responds to all the messages typical for PD Power Sources. No external processor is needed and it is completely USB PD 3.0 with PPS compliant.

Two Reference Design Examples

Below are two reference design example applications of the FUSB3307. One is an AC/DC design on the secondary side of the offline design and the other is a DC/DC design where the FUSB3307 directly controls the DC/DC controller. In the descriptions that follow, both of these designs are discussed when describing the operation of the FUSB3307. Interspersed within these descriptions is how it relates to USB Power Delivery (PD) and Type C specifications. These are just two example designs since there are considerably more use cases of the FUSB3307 in reference designs for power source applications. For more information on specific design needs, please contact your onsemi field application engineers.

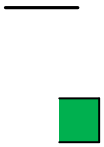


Figure 5. Offline Reference Design Example

Power Up and Assumptions

For Figure 5, the focus is on only the secondary side of this power source and only on the interactions with the FUSB3307 device. For Figure 6, only the interconnections of the FUSB3307 with the buck−boost shown will be discussed, not the buck−boost operation. It is assumed all other functionality ofthese AC/DC and DC/DC designs is known.

For Figure 5, upon application of an AC source, the secondary side VCC starts at 5 V and for Figure 6, upon application of input VBAT, the buck−boost regulates VCC at 5 V for USB−C operation. The FUSB3307 takes its input from the resistor divider ratio comprising of R8 and R9 in Figure 5 and Figure 6 above. In Figure 5, FUSB3307 controls the CATH pin current through the opto−coupler, R11 and R10 resistors for providing the feedback to the primary side controller to regulate to 5 V as shown in Figure 7.

Figure 7. Constant Voltage / Constant Current (CV/CC) section of Application Diagram

In Figure 6, FUSB3307 controls the CATH pin voltage which is tied to the COMP pin of the buck−boost which directly regulates the output voltage to 5 V. The ratio of R9:(R8+R9) is expected to be 1:10 to achieve 5 V on VCC upon power up which is typically R8 = 120 kohms and R9 = 13.3 kohms.

In Figure 6, the buck−boost has its feedback FB pin which has the resistor that also expects a 1:10 resistor divider in typical default operation. However this buck−boost resistor divider is

CC1 and CC2 Lines and USB Type-C Receptacle Assumptions

If a USB Type-C receptacle is used, CC1 and CC2 are connected from the receptacle to the FUSB3307's CC1 and CC2 pins. If a hardwired connection (called "captive cable" in Type-C and USB PD specifications) is desired, the CC line is connected to CC1 (or CC2 if more convenient for routing) and the VCONN line is connected to CC2 (or CC1) pin not used above.

The design in the figures above assumes a Type C receptacle (as opposed to captive cable) and all the following descriptions are consistent with this configuration. Also assumed is a USB 2.0 only receptacle (D+ and D−) for a power source application without data (that is, the USB D+ and D− do not go to a USB PHY). All SuperSpeed lines (TX1+, TX1−, RX1+, RX1−

Figure 10. VBUS Discharge by FUSB3307 via DISC Pin

VBUS is discharged through a resistor (R1) to the DISC pin of the FUSB3307 as shown in the highlighted section in Figure 10.

The external resistor R1 value is dependent on the total bulk capacitance (C8) of this power source so that VBUS is discharged within the time limits dictated by USB PD. A typical value for R1 is 39 , 1 W and in addition, there is internal resistance that causes a expected discharge current within the FUSB3307 in its discharge path (I_{DISC_iSink} in the electrical tables above). If the load current to the Sink is sufficient (exceeds $I_{CS\_iEN\_iDSCG}$ for $t_{CS\_iEN\_iDSCG}$ debounce time) such that the internal discharge is not needed, then the FUSB3307 will automatically disable internal discharge.

Upon power up, the FUSB3307 will discharge VBUS in case there is any voltage on VBUS since the only way a Sink can be attached per Type C specification is if VBUS is discharged to ground (below VSafe0V) upon attach. The discharge resistance limits are governed by the Type C specification when not sourcing power on VBUS (R_{DISC_iBUS} in the electrical tables above). It is preferred that no external load/discharge resistor is connected to VBUS other than R1 to the FUSB3307 discharge DISC pin.

A TVS diode connected from VBUS to ground and shown in the figures ([SZ]ESD7241) allow operating voltages up to 24 V covering the entire VBUS range of 3.3 V to 21 V for a USB PD PPS contract. This can be replaced by a TVS that covers the VBUS range for the use case of this design if needed.

USB Type C specification requires that the supply voltage is not sourced on VBUS until an attach per Type C specification has been determined. Dual back−to−back FET's for the load switch are not needed for reverse voltage protection since it is unlikely that VBUS is charged from an external source. For interoperability with legacy connectors, there is a case where a Type A to Type C cable is first plugged into a Type A port of a power source which then supplies 5 V on VBUS of the cable. Then the Type C connector is plugged into this design which is not plugged into the AC outlet nor gets it power from the DC input depending on the design. The 5 V from the cable will forward conduct through the Q1 FET and charge the bulk capacitor C8. This doesn't cause an issue, since the FUSB3307 will power up, check the CC1 and CC2 lines and realize it is not a legitimate Sink device plugged in and stay detached. Upon unplugging the A to C cable, the discharge resistance (R_{DISC_iBUS} in the electrical tables above) will discharge VBUS to ground if the input voltage is still unavailable. Even if the input power is supplied to this design during this incorrect connection, VCC will regulate to 5 V which will prevent the previously forward−bias body diode of Q1 FET from conducting and the FUSB3307 will wait for a legitimate Sink to be attached before turning on FET Q1. The maximum bulk capacitance is specified in the Type C specification to handle this fault case as shown in Table 5 from the USB Type C specification so as to allow for just one FET use for optimum efficiency.

Table 5. TYPE−C SPECIFICATION FOR VBUS BULK CAPACITANCE

Symbol	Notes	Min	Max	Units
VBUS Capacitance	Capacitance for source−only ports between VBUS and GND pins on receptacle when VBUS is not being sourced.		3000	F
	Capacitance for DRP ports between VBUS and GND pins on receptacle when VBUS is not being sourced.		10	F

Capacitance to ground on the connector side VBUS connection (source of Q1) can be added if needed but it hasn't been shown in the application diagrams above. If added, it is recommended it doesn't exceed 1 µF for recovery from the source−source case mentioned above.

Voltage and Current Sensing Operation

As mentioned above (see **Power Up and Assumptions**), the resistor ratio from VCC to ground formed by resistors R8 and R9 (typically 1:10 ratio where R8=120k and R9=13.3k) and sensed via FUSB3307 VFB pin will sense the voltage for VCC in order to set a new voltage. For Figure 5 offline design, this will be done via the FUSB3307 CATH pin, the opto−coupler, resistor R10 and the primary side PWM controller operation. R11 provides a bias current to the CATH pin feedback circuit within the FUSB3307 and is optional. For Figure 6 buck−boost design, this will be done via the FUSB3307 CATH pin controlling the buck−boost PWM via its COMP pin. The FUSB3307 will automatically control the CATH pin based on the desired voltage as determine by the USB PD contract and the existing VCC voltage sensed by VFB. If FUSB3307's PD communication is not responded to by the Sink upon initial attach, the

USB 2.0 Data Lines

The USB 2.0 Data Lines D+ and D− can be externally connected together via a 100 ohms resistor to provide the maximum power, a legacy USB device can take, which is 1.5 A per USB Battery Charging v1.2 (BC1.2) specification. This will usually be the case when a USB 2.0 to micro−B cable is plugged into this design where this adapter cable has the required Sink Rd resistors within it to allow the FUSB3307 to recognize a Type C attach and to source 5 V

When a Sink device is connected via the USB connector, as mentioned above, the FUSB3307 will detect a legitimate Type C attach and drive the GATE pin to turn on the VBUS load switch Q1. The initial voltage on VBUS is always 5 V (4.75 V to 5.5 V voltage range) and the CC pin will advertise 3 A capability which is the maximum power allowed by a Type C (without PD) port. FUSB3307 is not expected to S0B us>Tj5 5 V (4.75 B a w [W9c 0 Tw [a 9a the USB

PD Status message sent to indicate that the source is 5 A capable but the cable has limited the source capabilities to 3 A. In Table 7 the section of the SOP Status Data Block (SDB) is shown that communicates this power limitation.

Table 7. PD Status Message to Sink Showing Power is Limited by the Cable

Offset	Field	Bit	Description
5	Power Status	0	...
		1	Source power limited due to cable supported current
		2	...
		6...7	...

The FUSB3307 follows all USB PD specifications including dropping down to USB PD 2.0 operation when it detects a USB PD 2.0 Sink and USB PD2.0 cable eMarker (if applicable). All subsequent operation will follow the USB PD 2.0 specification until the FUSB3307 is reset via a Hard Reset message or undergoes a power cycle.

Standby Operation

When the FUSB3307 is in standby, where the source power supply still has to be maintained at 5 V via the CATH pin for a typical Type C connection but no Sink device has been attached to the FUSB3307, then the current consumed is just I_{CC_iGREEN} (< 870 A typical). This low standby current allows for all the energy standard specifications to be well exceeded for offline designs (typically the FUSB3307 within the offline design can achieve 21 mW standby power).

PDIVx Operation

The FUSB3307P6A0BF version of the FUSB3307 can adjust the output power to have any PDP (Power Delivery Power) from 16 W to 60 W in 7.5 W increments using the PDIV pins. Other FUSB3307 versions in the SOIC package will only advertise full power. The FUSB3307 versions in QFN package have the PDIV2 pin which will reduce the total power by 50% when set high. All other versions of the FUSB3307 will advertise the PDPs as shown in Table 6. The output power adjustment is accomplished through the PDIV2, PDIV1 and PDIV0 pins which are shared with the D+ and D− pins of other FUSB3307 versions.

The FUSB3307P6A0BF version can control the power as shown below (Table 8).

Table 8. MODIFIED ADVERTISED PDP BASED ON PDIVx

PDIV2	PDIV1	PDIV0	Total Power (W)	% of 60 W Total	Advertised PDP (Power Delivery Power)
1	1	1	60	100%	PDO's:5,9,12,15,20V @ 3A
1	1	0	52.5	87.50%	PDO's:5,9,12,15 @ 3A, 20V @ 2.6A
1	0	1	45	75%	PDO's:5,9,12,15V @ 3A, 20V @ 2.25A
1	0	0	37.5	62.50%	PDO's:5,9,12V @ 3A, 15V @ 2.46A
0	1	1	30	50%	PDO's:5,9V @ 3A, 12V @ 2.5A, 15V @ 2A
0	1	0	22.5	37.50%	PDO's:5V @ 3A, 9V @ 2.44A, 12V @ 1.83A
0	0	X	16	25%	PDO's:5V@3A, 9V @ 1.77A, 12V @ 1.33A

PDIV0 and PDIV1 are sampled during POR or when the FUSB3307P6A0BF executes a Soft_Reset or Hard_Reset which causes the new advertised capabilities to be sent to the sink by the FUSB3307P6A0BF. Alternatively, recovery from any protection operation would cause the FUSB3307P6A0BF to advertise the new PDP values based on the PDIV0 and PDIV1 pin settings.

Protection Operation

FUSB3307 has a number of ways it protects itself as shown in Table 9.

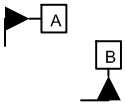
PACKAGE DIMENSIONS

SOIC ï14 NB
CASE 751A ï03
ISSUE L

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

PACKAGE DIMENSIONS

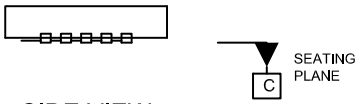
QFNW20 4x4, 0.5P
CASE 484AT
ISSUE O



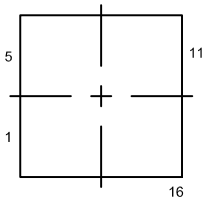
1.

3. DIMENSION b APPLIES TO THE PLATED

TOP VIEW



SIDE VIEW



BOTTOM VIEW

A
A1

D
D2

E2
e