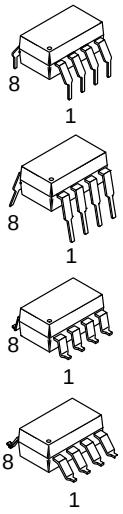
# 8-Pin DIP High Speed Transistor Optocouplers

# Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M, HCPL2531M




The 6N135M, 6N136M, HCPL4503M, HCPL2530M, and HCPL2531M optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor for each channel.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base−collector capacitance of the input transistor.

The HCPL4503M has no internal connection to the phototransistor base for improved noise immunity. An internal noise shield provides superior common mode rejection of up to 50,000 V/μs.

- High Speed – 1 MBit/s
- Dual−Channel: HCPL2530M, HCPL2531M
- CTR Guaranteed 0°C to 70°C
- No Base Connection for Improved Noise Immunity (HCPL4503M)
- Superior CMR of 15,000 V/μs Minimum (HCPL4503M)
- Safety and Regulatory Approvals
  - UL1577, 5,000 $VAC_{RMS}$ for 1 Minute
  - DIN EN/IEC60747−5−5
- These are Pb−Free Devices

- Line Receivers
- Pulse Transformer Replacement
- Output Interface to CMOS−LSTTL−TTL
- Wide−Bandwidth Analog Coupling

- https://www.onsemi.com/products/interfaces/high−performance−optocollecng
  https://www.onsemi.com/products/interfaces/high−performance−optocouplers/high−performance−transistor−optocouplers/hcpl0500
- https://www.onsemi.com/products/interfaces/high−performance−optocouplers/high−performance−transistor−optocouplers/fodm452
- https://www.onsemi.com/products/interfaces/high−performance−optocouplers/low−voltage−high−performance−optocouplers/fod050l

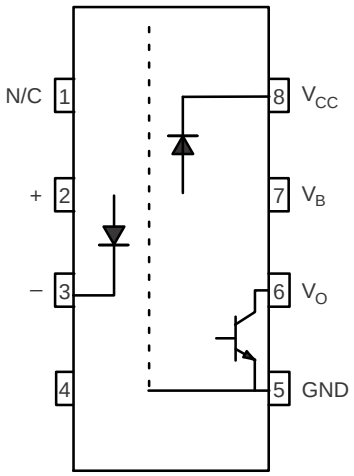

6N135 = Device Number
V = DIN EN/IEC60747−5−5 Option (only appears on component ordered with this option)
XX = Two Digit Year Code, e.g., ‘15’
YY = Two Digit Work Week Ranging from ‘01’ to ‘53’
B = Assembly Package Code

See detailed ordering and shipping information on page 11 of this data sheet.

NOTE: Some of the devices on this data sheet have been . Please refer to the table on page 11.



Publication Order Number:




6N135M, 6N136M,
HCPL4503M

HCPL2530M,
HCPL2531M

($T_A$ = 25°C unless otherwise noted)

| | | | | |
|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | | −40 to +125 | °C |
| $T_{OPR}$ | Operating Temperature | | −40 to +100 | °C |
| $T_J$ | Junction Temperature | | −40 to +125 | °C |
| $T_{SOL}$ | Lead Solder Temperature | | 260 for 10 s | °C |

| | | | | |
|---|---|---|---|---|
| $I_F$ (avg) | DC/Average Forward Input Current Each Channel (Note 2) | | 25 | mA |
| $I_F$ (pk) | Peak Forward Input Current Each Channel (Note 3) | 50% Duty Cycle, 1 ms P.W. | 50 | mA |
| $I_F$ (trans) | Peak Transient Input Current Each Channel | ≤1 μs P.W., 300 pps | 1.0 | A |
| $V_R$ | Reverse Input Voltage Each Channel | | 5 | V |
| $P_D$ | Input Power Dissipation Each Channel (Note 4) | | 45 | mW |

| | | | | |
|---|---|---|---|---|
| $I_O$ (avg) | Average Output Current Each Channel | | 8 | mA |
| $I_O$ (pk) | Peak Output Current Each Channel | | 16 | mA |
| $V_{EBR}$ | Emitter−Base Reverse Voltage | 6N135M and 6N136M | 5 | V |
| $V_{CC}$ | Supply Voltage | | −0.5 to 30 | V |
| $V_O$ | Output Voltage | | −0.5 to 20 | V |
| $I_B$ | Base Current | 6N135M and 6N136M | 5 | mA |
| $P_D$ | Output Power Dissipation Each Channel (Note 5) | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

($V_{CC}$ = 5.0 V, $T_A$ = 0°C to 70°C unless otherwise specified.)

| | | | |
|---|---|---|---|
| $V_F$ | Input Forward Voltage | All | $I_F$ |

(continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

($T_A$ = 0°C to 70°C unless otherwise specified.)

| | | | |
|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time to Logic LOW | 6N135M | $T_A$ |

(continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

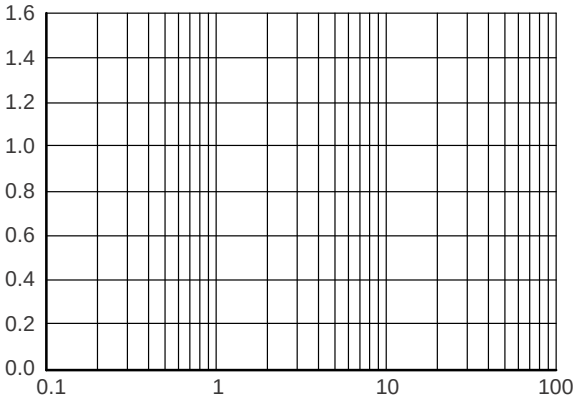
($T_A$ = 25°C, unless otherwise noted.)

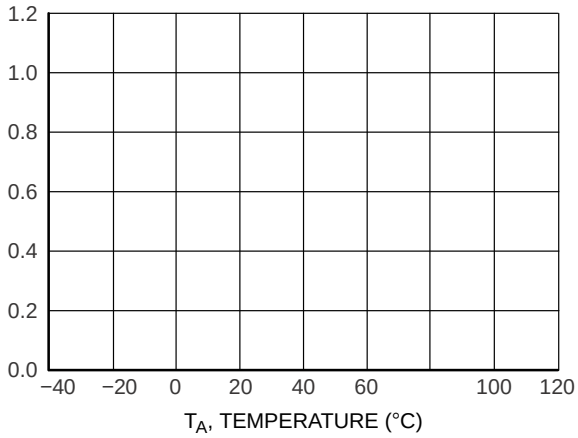
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_{ISO}$ | Withstand Isolation Test Voltage | All | RH ≤ 50%, $I_{I-O}$ ≤ 10 μA<br>t = 1 minute,<br>f = 50 Hz (Note 11) (Note 13) | 5,000 | − | − | $VAC_{RMS}$ |
| $R_{I-O}$ | Resistance (Input to Output) | All | $V_{I-O}$ = 500 $V_{DC}$ (Note 11) | − | $10^{11}$ | − | Ω |
| $C_{I-O}$ | Capacitance (Input to Output) | All | f = 1 MHz, $V_{I-O}$ = 0 $V_{DC}$ (Note 11) | − | 1 | − | pF |
| $I_{I-I}$ | Input−Input Insulation Leakage Current | HCPL2530M, HCPL2531M | RH ≤ 45%, $V_{I-I}$ = 500 $V_{DC}$, t = 5 s (Note 12) | − | <1 | − | nA |
| $R_{I-I}$ | Input−Input Resistance | HCPL2530M, HCPL2531M | $V_{I-I}$ = 500 $V_{DC}$ (Note 12) | − | $10^{12}$ | − | Ω |
| $C_{I-I}$ | Input−Input Capacitance | HCPL2530M, HCPL2531M | f = 1 MHz (Note 12) | − | 0.2 | − | pF |

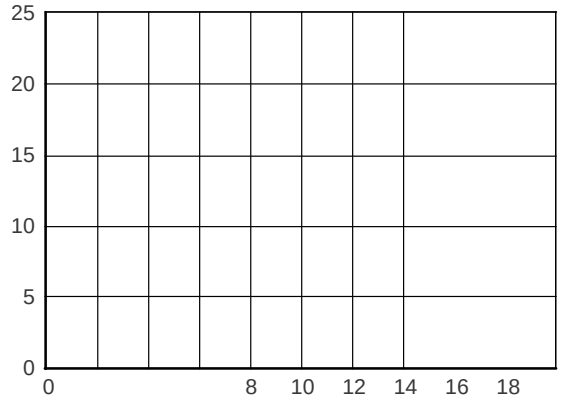
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

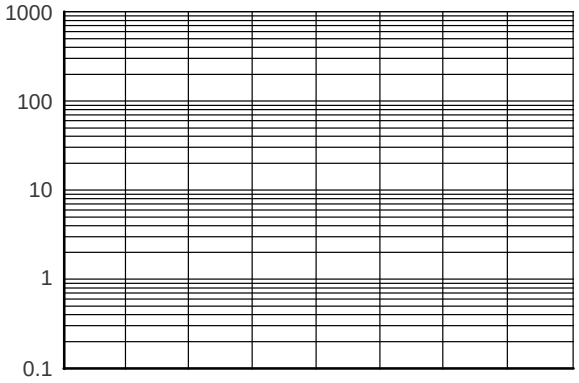
7. Current Transfer Ratio is defined as a ratio of output collector current, $I_O$, to the forward LED input current, $I_F$, times 100%.
8. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull−up resistor.
9. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and 5.6 kΩ pull−up resistor.
10. Common mode transient immunity in logic high level is the maximum tolerable (positive) $dV_{cm}/dt$ on the leading edge of the common mode pulse signal, $V_{CM}$, to assure that the output will remain in a logic high state (i.e., $V_O$ > 2.0 V).
    Common mode transient immunity in logic low level is the maximum tolerable (negative) $dV_{cm}/dt$ on the trailing edge of the common mode pulse signal, $V_{CM}$, to assure that the output will remain in a logic low state (i.e., $V_O$ < 0.8 V).
11. Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.
12. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
13. 5000 $V_{RMS}$ for 1 minute duration is equivalent to 6000 $V_{RMS}$ for 1 second duration.

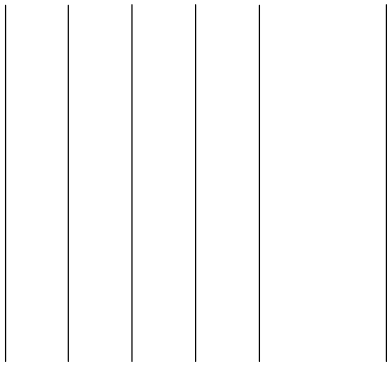
(For single−channel devices; 6N135M, 6N136M, and HCPL4503M.)



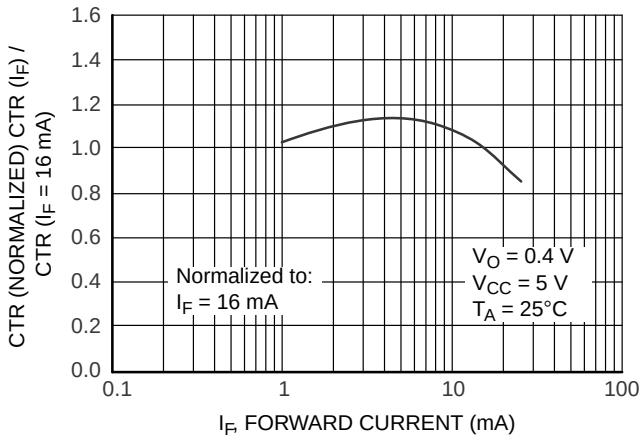



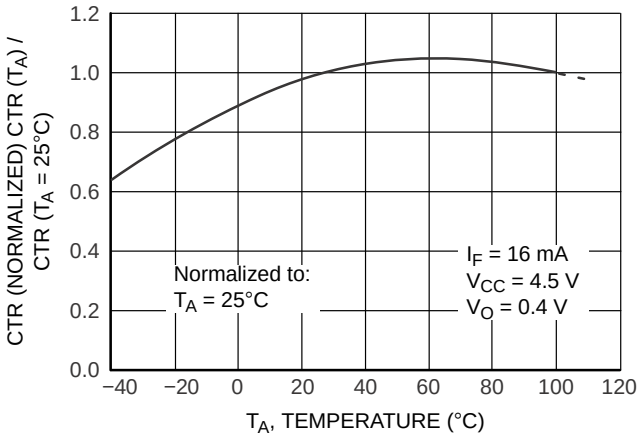



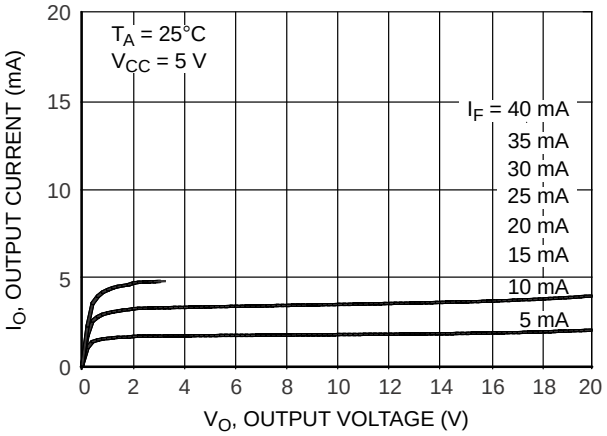



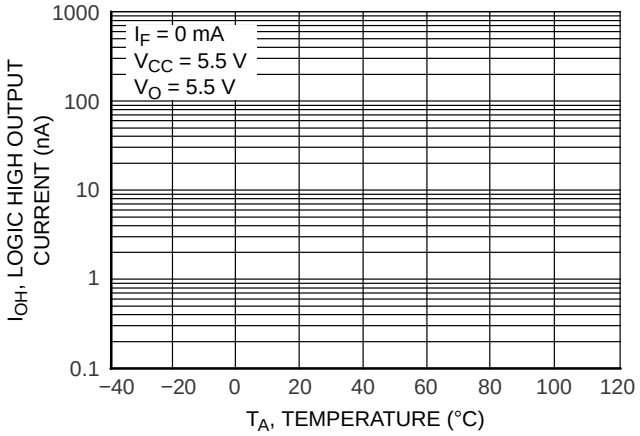



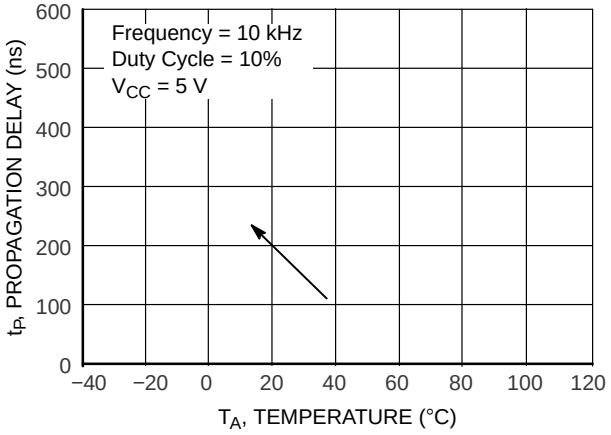
(For dual−channel devices; HCPL2530M and HCPL2531M.)

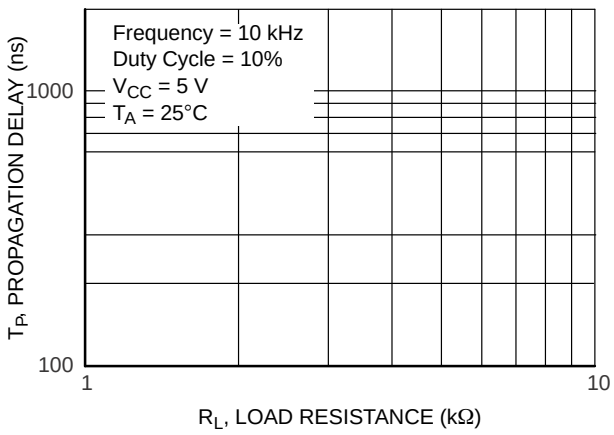


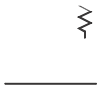



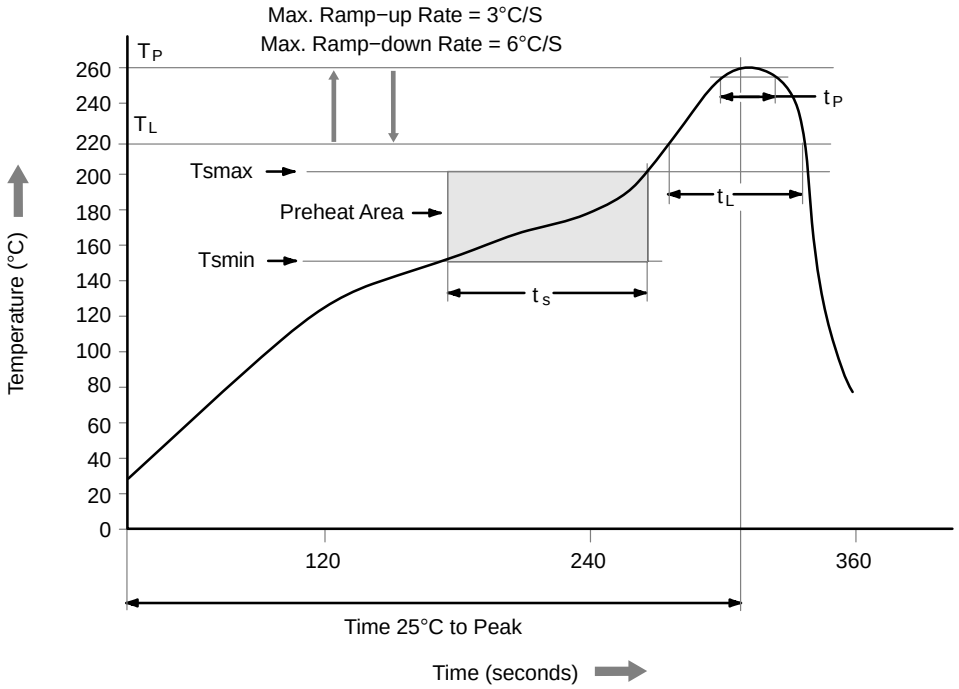








| | |
|---|---|
| | 150°C |
| | 200°C |
| | to 120 s |

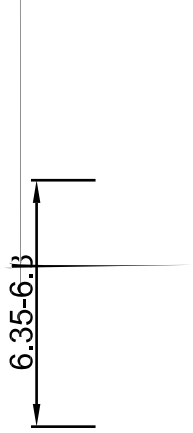
| | | † |
|---|---|---|
| 6N135M | PDIP8 9.655x6.61, 2.54P<br>DIP 8−Pin | 50 Units / Tube |
| 6N135SM | PDIP8 GW<br>SMT 8−Pin (Lead Bend) | 50 Units / Tube |
| 6N135SDM | PDIP8 GW<br>SMT 8−Pin (Lead Bend) | 1,000 / Tape and Reel |
| 6N135VM | PDIP8 9.655x6.61, 2.54P<br>DIP 8−Pin, DIN IEC60747−5−5 Option | 50 Units / Tube |
| 6N135SVM | PDIP8 GW<br>SMT 8−Pin (Lead Bend), DIN EN/IEC 60747−5−5 Option | 50 Units / Tube |
| 6N135SDVM | PDIP8 GW<br>SMT 8−Pin (Lead Bend), DIN EN/IEC 60747−5−5 Option | 1,000 / Tape and Reel |
| 6N135TSVM | PDIP8 GW<br>SMT 8−Pin, 0.4” Lead Spacing, DIN EN/IEC 60747−5−5 Option | 50 Units / Tube |
| 6N135TSR2VM | PDIP8 GW<br>SMT 8−Pin, 0.4” Lead Spacing, DIN EN/IEC 60747−5−2 Option | 1,000 / Tape and Reel |

(Note 14)

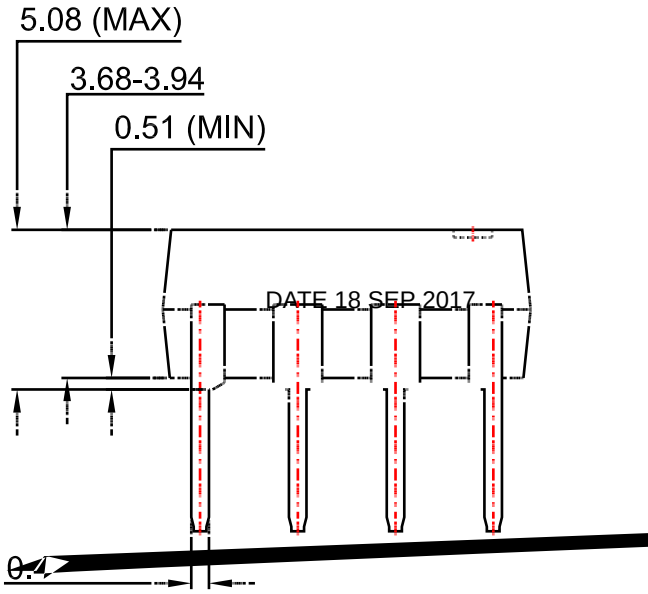
| | | |
|---|---|---|
| 6N135TVM | PDIP8 6.6x3.81, 2.54P<br>DIP 8−Pin, 0.4” Lead Spacing, DIN EN/IEC 60747−5−5 Option | 50 Units / Tube |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**PDIP8 6.6x3.81, 2.54P**



**PDIP8 9.655x6.6, 2.54P**
CASE 646CQ
ISSUE O



**PDIP8 GW**
CASE 709AC
ISSUE O

LAN

TO THIS PACKAGE

B) ALL DIMEN

**PDIP8 GW**
CASE 709AD
ISSUE O

DATE 31 JUL 2016




NOTES:
A) NO STA