

8-Pin DIP High Speed Transistor Optocouplers

Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M, HCPL2531M

Description

The 6N135M, 6N136M, HCPL4503M, HCPL2530M, and HCPL2531M optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor for each channel.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base collector capacitance of the input transistor.

The HCPL4503M has no internal connection to the phototransistor base for improved noise immunity. An internal noise shield provides superior common mode rejection of up to 50,000 V/ μ s.

Features

- High Speed 1 MBit/s
- Dual Channel: HCPL2530M, HCPL2531M
- CTR Guaranteed 0°C to 70°C
- No Base Connection for Improved Noise Immunity (HCPL4503M)
- Superior CMR of 15,000 V/µs Minimum (HCPL4503M)
- Safety and Regulatory Approvals
 - ◆ UL1577, 5,000 VAC_{RMS} for 1 Minute
 - ◆ DIN EN/IEC60747 5 5
- These are Pb Free Devices

Applications

- Line Receivers
- Pulse Transformer Replacement
- Output Interface to CMOS LSTTL TTL
- Wide Bandwidth Analog Coupling

Related Resources

• <u>https://www.onsemi.com/products/interfaces/high_performance_opto</u> collecng

https://www.onsemi.com/products/interfaces/high_performance_opto couplers/high_performance_transistor_optocouplers/hcpl0500

- https://www.onsemi.com/products/interfaces/high_performance_opto couplers/high_performance_transistor_optocouplers/fodm452
- <u>https://www.onsemi.com/products/interfaces/high_performance_opto</u> <u>couplers/low_voltage_high_performance_optocouplers/fod0501</u>



MARKING DIAGRAM



6N135 = Device Number

- = DIN EN/IEC60747–5–5 Option (only appears on component ordered with this
 - option)
- XX = Two Digit Year Code, e.g., '15'
- YY = Two Digit Work Week Ranging from '01' to '53'
- B = Assembly Package Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

NOTE: Some of the devices on this data sheet have been DISCONTINUED. Please refer to the table on page 11.

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HCPL2530M, HCPL2531M



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Symbol	Parameter	Test Conditions	Value	Unit
T _{STG}	Storage Temperature		-40 to +125	°C
T _{OPR}	Operating Temperature		-40 to +100	°C
TJ	Junction Temperature		-40 to +125	°C
T _{SOL}	Lead Solder Temperature		260 for 10 s	°C
EMITTER				
I _F (avg)	DC/Average Forward Input Current Each Channel (Note 2)		25	mA
I _F (pk)	Peak Forward Input Current Each Channel (Note 3)	50% Duty Cycle, 1 ms P.W.	50	mA
I _F (trans)	Peak Transient Input Current Each Channel	≤1 μs P.W., 300 pps	1.0	А
V _R	Reverse Input Voltage Each Channel		5	V
PD	Input Power Dissipation Each Channel (Note 4)		45	mW
DETECTOR				
I _O (avg)	Average Output Current Each Channel		8	mA
l _O (pk)	Peak Output Current Each Channel		16	mA
V _{EBR}	Emitter-Base Reverse Voltage	6N135M and 6N136M	5	V
V _{CC}	Supply Voltage		-0.5 to 30	V
V _O	Output Voltage		-0.5 to 20	V
Ι _Β	Base Current	6N135M and 6N136M	5	mA
PD	Output Power Dissipation Each Channel (Note 5)	7	-	-

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$ unless otherwise noted)

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Device	Test Conditions	Min	Тур	Max	Unit
INDIVIDUAL COMPONENT CHARACTERISTICS ($V_{CC} = 5.0 \text{ V}$, $T_A = 0^{\circ}\text{C}$ to 70°C unless otherwise specified.)							
EMITTER							
V _F	Input Forward Voltage	All	I _F				
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ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Device	Test Conditions	Min	Тур	Max	Unit
SWITCHIN	SWITCHING CHARACTERISTICS ($T_A = 0^{\circ}C$ to 70°C unless otherwise specified.)						
t _{PHL}	Propagation Delay Time to Logic LOW	6N135M	T _A				

Symbol	Parameter	Device	Test Conditions	Min	Тур	Max	Unit
ISOLATIO	N CHARACTERISTICS (T _f	∖ = 25°C, unless o	otherwise noted.)				
V _{ISO}	Withstand Isolation Test Voltage	All	RH \leq 50%, I _{I-O} \leq 10 µA t = 1 minute, f = 50 Hz (Note 11) (Note 13)	5,000	-	-	VAC _{RM} S
R _{I–O}	Resistance (Input to Output)	All	V _{I–O} = 500 V _{DC} (Note 11)	-	10 ¹¹	-	Ω
C _{I–O}	Capacitance (Input to Output)	All	$f = 1 \text{ MHz}, V_{I-O} = 0 V_{DC}$ (Note 11)	-	1	-	pF
I _{I-I}	Input–Input Insulation Leakage Current	HCPL2530M, HCPL2531M	RH ≤ 45%, V _{I–I} = 500 V _{DC} , t = 5 s (Note 12)	-	<1	-	nA
R _{I-I}	Input-Input Resistance	HCPL2530M, HCPL2531M	V _{I-I} = 500 V _{DC} (Note 12)	-	10 ¹²	-	Ω
C _{I-I}	Input–Input Capacitance	HCPL2530M, HCPL2531M	f = 1 MHz (Note 12)	-	0.2	-	pF

ELECTRICAL CHARACTERISTICS (continued)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Current Transfer Ratio is defined as a ratio of output collector current, IO, to the forward LED input current, IF, times 100%.

8. The 4.1 k Ω load represents 1 LSTTL unit load of 0.36 mA and 6.1 k Ω pull-up resistor.

9. The 1.9 k Ω load represents 1 TTL unit load of 1.6 mA and 5.6 k Ω pull-up resistor.

10. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode

pulse signal, V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0$ V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O > 0.8$ V).

11. Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.

12. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

13.5000 V_{RMS} for 1 minute duration is equivalent to 6000 V_{RMS} for 1 second duration.

TYPICAL PERFORMANCE CURVES

(For single-channel devices; 6N135M, 6N136M, and HCPL4503M.)









TYPICAL PERFORMANCE CURVES

(For dual-channel devices; HCPL2530M and HCPL2531M.)







Figure 10. Output Current vs. Output Voltage



Figure 12. Propagation Delay vs. Temperature



Figure 9. Normalized CTR vs. Temperature



Figure 11. Logic High Output Current vs. Temperature



Figure 13. Propagation Delay vs. Load Resistance

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Profile Feature	Pb-Free Assembly Profile
	150°C
	200°C
	to 120 s

ORDERING INFORMATION

Part Number	Package	Shipping [†]
6N135M	PDIP8 9.655x6.61, 2.54P DIP 8–Pin	50 Units / Tube
6N135SM	PDIP8 GW SMT 8-Pin (Lead Bend)	50 Units / Tube
6N135SDM	PDIP8 GW SMT 8-Pin (Lead Bend)	1,000 / Tape and Reel
6N135VM	PDIP8 9.655x6.61, 2.54P DIP 8–Pin, DIN IEC60747–5–5 Option	50 Units / Tube
6N135SVM	PDIP8 GW SMT 8–Pin (Lead Bend), DIN EN/IEC 60747–5–5 Option	50 Units / Tube
6N135SDVM	PDIP8 GW SMT 8–Pin (Lead Bend), DIN EN/IEC 60747–5–5 Option	1,000 / Tape and Reel
6N135TSVM	PDIP8 GW SMT 8–Pin, 0.4" Lead Spacing, DIN EN/IEC 60747–5–5 Option	50 Units / Tube
6N135TSR2VM	PDIP8 GW SMT 8–Pin, 0.4" Lead Spacing, DIN EN/IEC 60747–5–2 Option	1,000 / Tape and Reel

DISCONTINUED (Note 14)

6N135TVM	PDIP8 6.6x3.81, 2.54P	50 Units / Tube
	DIP 8–Pin, 0.4" Lead Spacing, DIN EN/IEC 60747–5–5 Option	

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.









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