# onsemi

### 8-Pin DIP High-Speed 10 MBit/s Logic Gate Optocouplers

### Single-Channel: 6N137M, HCPL2601M, HCPL2611M Dual-Channel: HCPL2630M, HCPL2631M

#### Description

The 6N137M, HCPL2601M, HCPL2611M single-channel and HCPL2630M, HCPL2631M dual-channel optocouplers consist of a 850 nm AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The switching parameters are guaranteed over the temperature range of -40 C to +85 C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8).

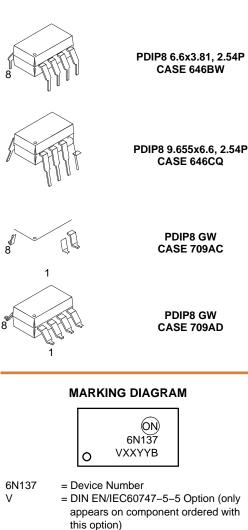
An internal noise shield provides superior common mode rejection of typically 10 kV/ $\mu$ s. The HCPL2601M and HCPL2631M has a minimum CMR of 5 kV/ $\mu$ s. The HCPL2611M has a minimum CMR of 10 kV/ $\mu$ s.

#### Features

Very High Speed – 10 MBit/s Superior CMR – 10 kV/µs Fan–out of 8 Over –40 C to +85 C Logic Gate Output Strobable Output Wired OR–open Collector Safety and Regulatory Approvals UL1577, 5,000 VAC<sub>RMS</sub> for 1 Minute DIN EN/IEC60747–5–5 These are Pb–Free Devices

#### Applications

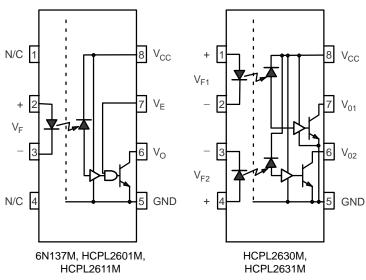
Ground Loop Elimination LSTTL to TTL, LSTTL or 5 V CMOS Line Receiver, Data Transmission Data Multiplexing Switching Power Supplies Pulse Transformer Replacement Computer-peripheral Interface



- XX = Two-Digit Year Code, e.g., '16' YY = Two-Digit Work Week, Ranging from '01' to '53' B = Assembly Package Code
  - = Assembly Package Code

#### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 14 of this data sheet.



A 0.1  $\mu F$  bypass capacitor must be connected between pins 8 and 5 (Note 1).

Figure 1. Schematics

Input	Enable	Output
Н	Н	L
L	Н	Н
Н	L	Н
L	L	Н
Н	NC	L
L	NC	Н

TRUTH TABLE (Positive Logic)

**SAFETY AND INSULATION RATINGS** (As per DIN EN/IEC 60747–5–5, this optocoupler is suitable for "safe electrical insulation" only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Parameter	Characteristics	
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	<150 V <sub>RMS</sub>	I–IV
	<300 V <sub>RMS</sub>	
	<450 V <sub>RMS</sub>	I–III
	<600 V <sub>RMS</sub>	I–III
Climatic Classification		40/100/21
Pollution Degree (DIN VDE 0110/1.89)	2	
Comparative Tracking Index	175	

Symbol	Parameter	Value	Unit
V <sub>PR</sub>	Input-to-Output Test Voltage, Method A, $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test with $t_m = 10$ s, Partial Discharge < 5 pC	1,335	V <sub>peak</sub>
	Input–to–Output Test Voltage, Method B, $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1 \text{ s}$ , Partial Discharge < 5 pC	1,669	V <sub>peak</sub>
VIORM	Maximum Working Insulation Voltage	890	V <sub>peak</sub>

ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 C unless otherwise noted)

Symbol	Parameter	Device	Value	Unit
T <sub>STG</sub>	Storage Temperature		-40 to +125	С
T <sub>OPR</sub>	Operating Temperature		-40 to +100	С
TJ	Junction Temperature		-40 to +125	С
T <sub>SOL</sub>	Lead Solder Temperature		260 for 10 s	С

EMITTER

I <sub>F</sub> (avg)	DC/Average Forward Input Current Per Channel	Single Channel	50	mA
		Dual Channel	30	
VE	Enable Input Voltage Not to Exceed $V_{CC}$ by More than 500 mV	Single Channel	5.5	V
V <sub>R</sub>	Reverse Input Voltage Per Channel	All	5.0	V
Pl	Input Power Dissipation Per Channel	Single Channel	100	mW
		Dual Channel	45	

#### DETECTOR

V <sub>CC</sub>	Supply Voltage	All	-0.5 to 7.0	V
I <sub>O</sub> (avg)	Average Output Current Per Channel	All	25	mA
I <sub>O</sub> (pk)	Peak Output Current Per Channel	All	50	mA
V <sub>O</sub>	Output Voltage Per Channel	All	-0.5 to 7.0	V
Po	Output Power Dissipation Per Channel	Single Channel	85	mW
		Dual Channel	60	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.5	V
I <sub>FL</sub>	Input Current, Low Level	0	250	μΑ
I <sub>FH</sub>	Input Current, High Level	6.3 (Note 3)	20.0	mA
V <sub>EL</sub>	Enable Voltage, Low Level	0	0.8	V
$V_{EH}$	Enable Voltage, High Level	2.0	V <sub>CC</sub>	V
T <sub>A</sub>	Ambient Operating Temperature	-40	+85	С
Ν	Fan Out (TTL Load)	-	8	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. 6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

Symbol	Parameter	Test Conditions	Device	Min	Тур	Max	Unit
NDIVIDUAL	COMPONENT CHARACTER	<b>RISTICS</b> ( $V_{CC} = 5.5 \text{ V}, T_A = 0 \text{ C to } 70 \text{ C}$	unless otherwise	specified	l)	•	
EMITTER							
VF	Input Forward Voltage	I <sub>F</sub> = 10 mA, T <sub>A</sub> = 25 C	All	_	1.45	1.70	V
		I <sub>F</sub> = 10 mA	1	_	-	1.80	
$B_{VR}$	Input Reverse Breakdown Voltage	I <sub>R</sub> = 10 μA	All	5.0	-	-	V
C <sub>IN</sub>	Input Capacitance	V <sub>F</sub> = 0, f = 1 MHz	All	_	60	-	pF
$\Delta V_{F} / \Delta T_{A}$	Temperature Coefficient of Forward Voltage	I <sub>F</sub> = 10 mA	All	-	-1.4	-	mV/ C
DETECTOR						•	
I <sub>CCL</sub>	Logic Low Supply Current	$I_F$ = 10 mA, $V_O$ = Open, $V_E$ = 0.5 V	Single Channel	-	8	13	mA
		$I_{F1} = I_{F2} = 10 \text{ mA}, V_0 = \text{Open}$	Dual Channel	-	14	21	
I <sub>CCH</sub>	Logic High Supply Current	$I_F = 0$ mA, $V_O = Open$ , $V_E = 0.5$ V	Single Channel	-	6	10	mA
		$I_F = 0 \text{ mA}, V_O = \text{Open}$	Dual Channel	-	10	15	
I <sub>EL</sub>	Low Level Enable Current	V <sub>E</sub> = 0.5 V	Single Channel	-	-0.7	-1.6	mA
I <sub>EH</sub>	High Level Enable Current	V <sub>E</sub> = 2.0 V	Single Channel	-	-0.5	-1.6	mA
V <sub>EL</sub>	Low Level Enable Voltage	I <sub>F</sub> = 10 mA (Note 4)	Single Channel	-	-	0.8	V
V <sub>EH</sub>	High Level Enable Voltage	I <sub>F</sub> = 10 mA	Single Channel	2.0	-	-	V
TRANSFER	CHARACTERISTICS (V <sub>CC</sub> =	5.5 V, $T_A = -40$ C to +85 C unless oth	erwise specified)				
I <sub>FT</sub>	Input Threshold Current	$V_{O} = 0.6 \text{ V}, V_{E} = 2.0 \text{ V}, I_{OL} = 13 \text{ mA}$	All	-	3	5	mA
I <sub>OH</sub>	HIGH Level Output Current	$V_{O}$ = 5.5 V, $I_{F}$ = 250 $\mu A,~V_{E}$ = 2.0 V	All	-	-	100	μΑ
V <sub>OL</sub>	LOW Level Output Voltage	$I_F = 5 \text{ mA}, V_E = 2.0 \text{ V}, I_{OL} = 13 \text{ mA}$	All	_	0.4	0.6	V
SWITCHING	G CHARACTERISTICS (V <sub>CC</sub> =	= 5 V, I <sub>F</sub> = 7.5 mA, T <sub>A</sub> = -40 C to +85 C	unless otherwise	specified	d)	-	
t <sub>PHL</sub>	Propagation Delay Time to Logic LOW	$R_L$ = 350 Ω, $C_L$ = 15 pF, $T_A$ = 25 C (Note 5) (Figure 23)	All	25	40	75	ns
		R <sub>L</sub> = 350 Ω, C <sub>L</sub> = 15 pF (Note 5) (Figure 23)		-	-	100	
t <sub>PLH</sub>	Propagation Delay Time to Logic HIGH	$R_L$ = 350 Ω, $C_L$ = 15 pF <sup>,</sup> $T_A$ = 25 C (Note 6) (Figure 23)	All	20	40	75	ns
		$R_L$ = 350 Ω, $C_L$ = 15 pF (Note 6) (Figure 23)		-	-	100	
t <sub>PHL</sub> -t <sub>PLH</sub>	Pulse Width Distortion	$R_L$ = 350 $\Omega$ , $C_L$ = 15 pF (Figure 23)	All	-	1	35	ns
t <sub>R</sub>	Output Rise Time (10% to 90%)	$R_L$ = 350 Ω, $C_L$ = 15 pF (Note 7) (Figure 23)	All	-	30	-	ns
t <sub>F</sub>	Output Fall Time (90% to 10%)	$R_L$ = 350 Ω, $C_L$ = 15 pF(Note 8) (Figure 23)	All	-	10	-	ns
<sup>t</sup> EHL	Enable Propagation Delay Time to Output LOW Level	$V_{EH}$ = 3.5 V, R <sub>L</sub> = 350 Ω, C <sub>L</sub> = 15 pF (Note 9) (Figure 24)	Single Channel	-	15	-	ns
t <sub>ELH</sub>	Enable Propagation Delay Time to Output HIGH Level	$V_{EH}$ = 3.5 V, R <sub>L</sub> = 350 Ω, C <sub>L</sub> = 15 pF (Note 10) (Figure 24)	Single Channel	-	15	-	ns

Symbol	Parameter	Test Conditions	Device	Min	Тур	Max	Unit	
SWITCHING CHARACTERISTICS ( $V_{CC}$ = 5 V, $I_F$ = 7.5 mA, $T_A$ = -40 C to +85 C unless otherwise specified)								
CM <sub>H</sub>	Common Mode Transient Immunity at Logic High	$    I_F = 0 \text{ mA, } V_{CM} = 50 \text{ V}_{PEAK}, \\ R_L = 350 \ \Omega, \text{ T}_A = 25 \text{ C} \text{ (Note 11)} \\ \text{(Figure 25)} $	6N137M, HCPL2630M	-	10,000	-	V/µs	
			HCPL2601M, HCPL2631M	5000	10,000	-		
		I <sub>F</sub> = 0 mA, V <sub>CM</sub> = 400 V <sub>PEAK</sub> , R <sub>L</sub> = 350 Ω, T <sub>A</sub> = 25 C (Note 11) (Figure 25)	HCPL2611M	10,000	15,000	-		
CM <sub>L</sub>	Common Mode Transient Immunity at Logic Low	$V_{CM} = 50 V_{PEAK}, R_L = 350 \Omega,$ $T_A = 25 C$ (Note 11) (Figure 25)	6N137M, HCPL2630M	-	10,000	-	V/µs	
			HCPL2601M, HCPL2631M	5000	10,000	-		
		$V_{CM}$ = 400 V <sub>PEAK</sub> , R <sub>L</sub> = 350 Ω, T <sub>A</sub> = 25 C (Note 11) (Figure 25)	HCPL2611M	10,000	15,000	-		

#### ELECTRICAL CHARACTERISTICS (continued) Darameter

#### **ISOLATION CHARACTERISTICS** (T<sub>A</sub> = 25 C, unless otherwise noted)

V <sub>ISO</sub>	Withstand Insulation Test Voltage	$\begin{array}{ll} \mbox{Relative Humidity} & 50\%, \\ I_{I-O} & 10 \ \mu A, \ t = 1 \ min, \ f = 50 \ Hz \\ (Note \ 12) \ (Note \ 13) \end{array}$	All	5,000	-	-	VAC <sub>RMS</sub>
R <sub>I-O</sub>	Resistance (Input to Output)	$V_{I-O} = 500 V_{DC}$ (Note 12)	All	-	10 <sup>11</sup>	-	Ω
C <sub>I–O</sub>	Capacitance (Input to Output)	f = 1 MHz, $V_{I-O}$ = 0 $V_{DC}$ (Note 12)	All	-	1	-	pF
I <sub>I–O</sub>	Input–Output Insulation Leakage Current	Relative Humidity 45%, $V_{I-I} = 3000 V_{DC}$ , t = 5 s (Note 12)	All	-	-	1.0	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Enable Input - No pull up resistor required as the device has an internal pull up resistor.

5. t<sub>PHL</sub> - Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.

6. tPLH - Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.

7. t<sub>R</sub> – Rise time is measured from the 10% to the 90% levels on the LOW to HIGH transition of the output pulse.

8.  $t_{F}$  – Fall time is measured from the 90% to the 10% levels on the HIGH to LOW transition of the output pulse.

9. t<sub>EHL</sub> - Enable input propagation delay is measured from the 1.5 V level on the LOW to HIGH transition of the input voltage pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.

10.t<sub>ELH</sub> - Enable input propagation delay is measured from the 1.5 V level on the HIGH to LOW transition of the input voltage pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.

11. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV<sub>cm</sub>/dt on the leading edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic high state (i.e.,  $V_O > 2.0$  V). Common mode transient immunity in logic low level is the maximum tolerable (negative)  $dV_{cm}/dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic low state (i.e., V<sub>O</sub> < 0.8 V).

12. Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.

13.5000 VAC<sub>RMS</sub> for 1 minute duration is equivalent to 6000 VAC<sub>RMS</sub> for 1 second duration

### **TYPICAL PERFORMANCE CURVES**

(FOR SINGLE-CHANNEL DEVICES: 6N137M, HCPL2601M, AND HCPL2611M)

0.9

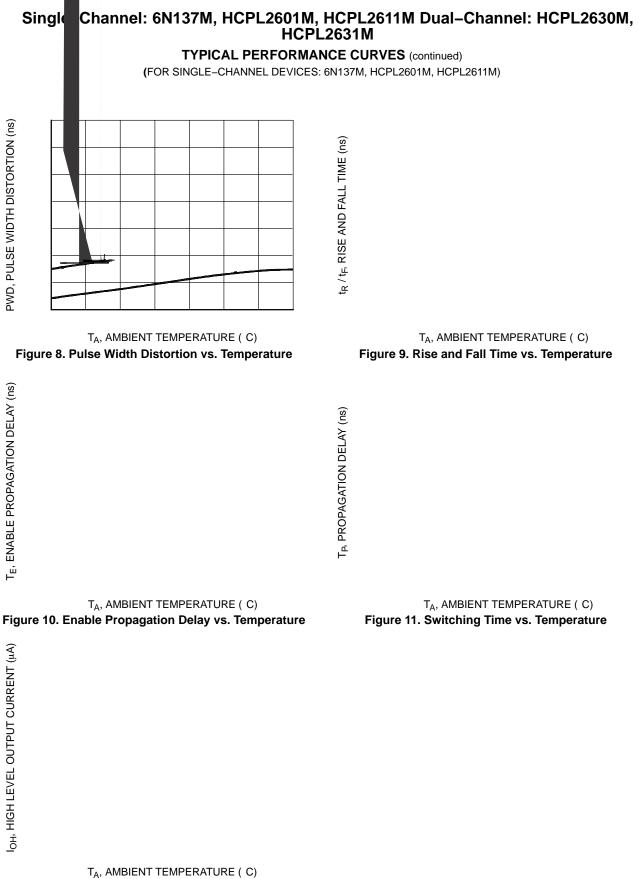
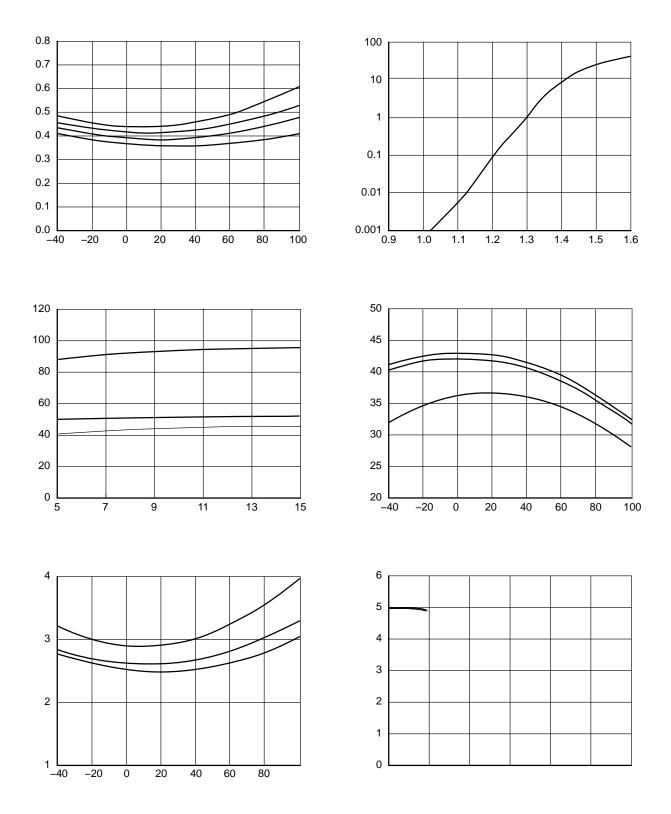


Figure 12. High Level Output Current vs. Temperature

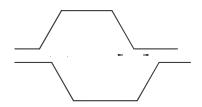
TYPICAL PERFORMANCE CURVES (continued)

(FOR DUAL-CHANNEL DEVICES: HCPL2630M AND HCPL2631M)



TYPICAL PERFORMANCE CURVES (continued)

(FOR DUAL-



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Pulse Generator tr = 5 ns  $Z_0 = 50 \Omega$ 

TEST CIRCUITS (continued)

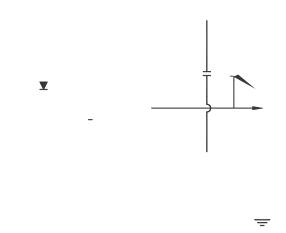
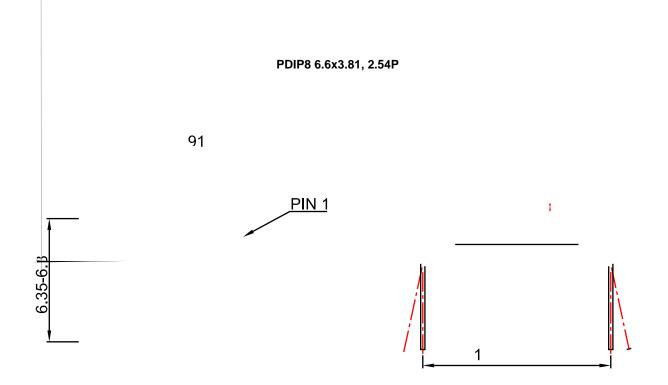


Figure 25. Test Circuit Common Mode Transient Immunity

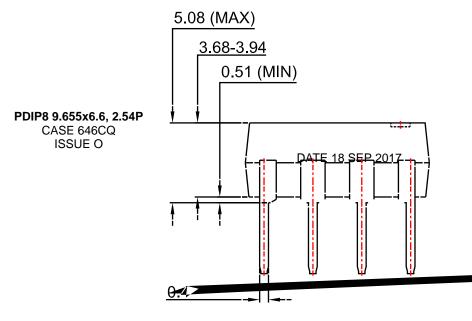
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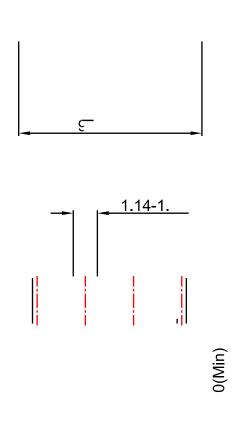
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DATE 31 JUL 2016





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