Application Circuit Example

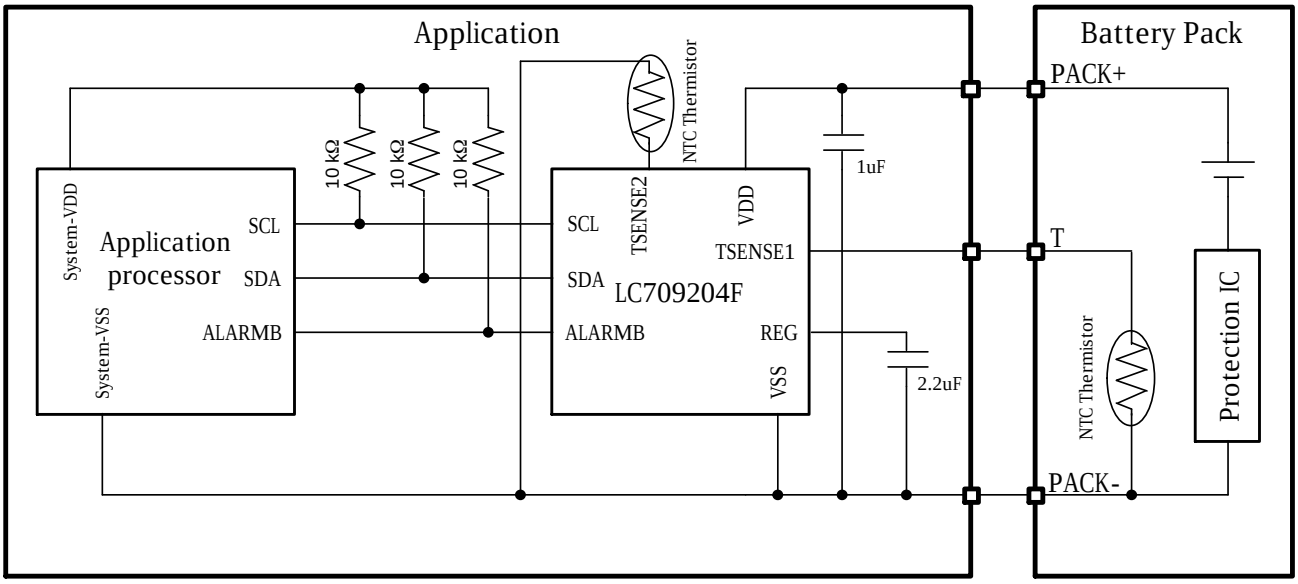


Figure 1. Example of an Application Schematic using LC709204F
(The temperature is measured using TSENSE1 pin.)

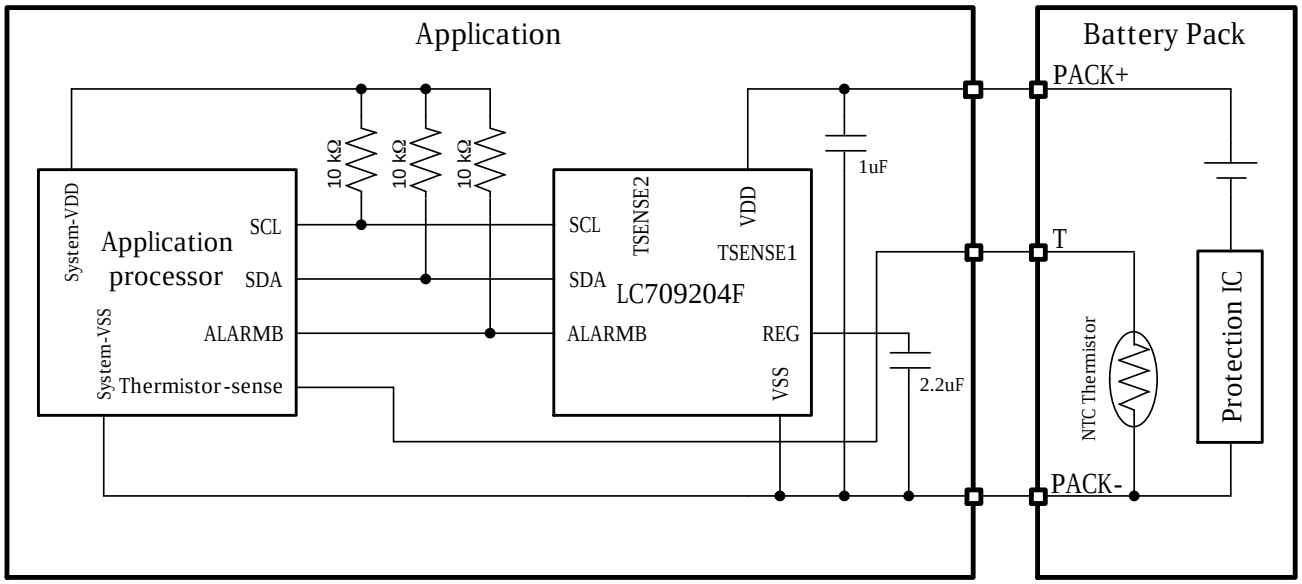


Figure 2. Example of an Application Schematic using LC709204F
(The Temperature is sent via I^2C.)

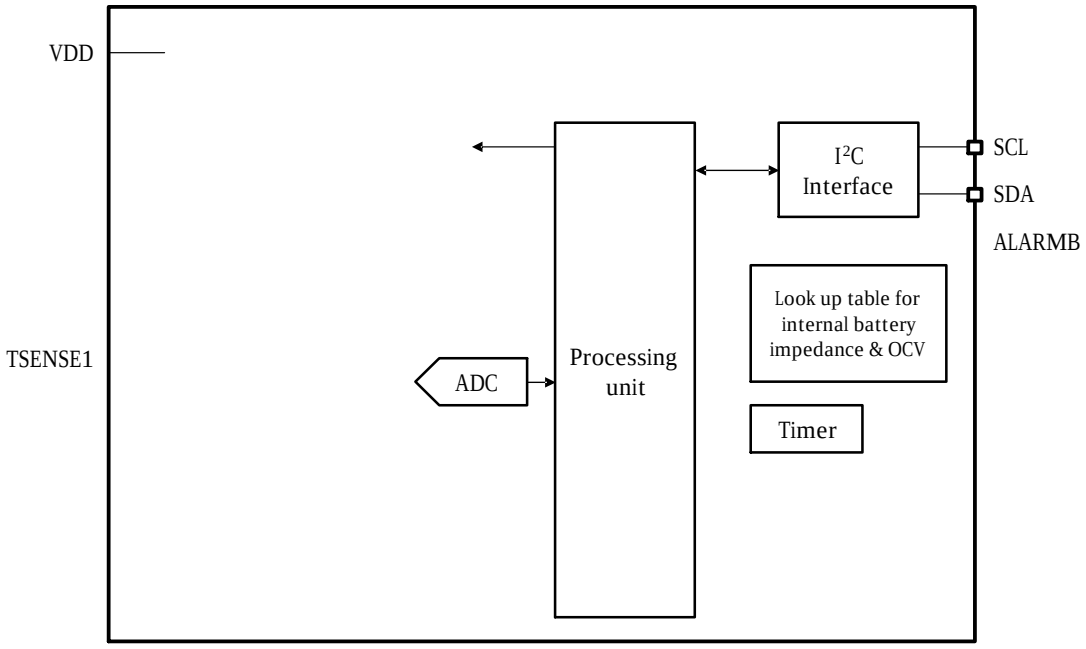


Figure 3. Block Diagram

Table 1. PIN FUNCTION

WLCSP12	Name	I/O	Description
A1	SDA	I/O	I^2C Data pin (open drain). Pull−up must be done externally.
B1	SCL	I/O	I^2C Clock pin (open drain). Pull−up must be done externally.
C1	ALARMB	O	This pin indicates alarm by low output (open drain). Pull−up must be done externally. Keep this pin OPEN when not in use.
A2	V_{SS}	−	Connect this pin to the battery's negative (−) pin.
B2	TEST2	I	Connect this pin to the battery's negative (−) pin.
C2	TEST1	I	Connect this pin to the battery's negative (−) pin.
A3	REG	O	Regulator output. Connect this pin to the capacitor.
B3	TSENSE2	I/O	Sense input and power supply for a thermistor. Connect 10 kΩ NTC thermistor to measure "Ambient temperature (0x30)". Keep this pin OPEN when not in use.
C3	NF1	−	No function pin. Keep this pin OPEN. Short−pin with TSENSE2 is permitted to pull out it.
A4	VDD	−	Connect this pin to the battery's positive (+) pin.
B4	TSENSE1	I/O	Sense input and power supply for a thermistor. Connect 10 kΩ NTC thermistor to measure "Cell temperature (0x08)". Keep this pin OPEN when not in use.
C4	NF2	−	No function pin. Keep this pin OPEN.

Table 2. ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} (V)	Specification	Unit

Table 4. ELECTRICAL CHARACTERISTICS (T_A = −40 to +85°C, V_{SS} = 0 V, Typ: 4 V, T_A = 25°C)

Parameter	Symbol	Pin/ Remarks	Conditions		Specification			Unit
				V_{DD} [V]	Min	Typ	Max	
LDO								
LDO Output Voltage	V_{REG}	REG		2.5 to 5.0	2.3	2.7	3.0	V
CONSUMPTION CURRENT								
Operational Mode	I_{DD} (1)	VDD	Ta = −20°C to +70°C Average current with 0.01C Constant discharge.	2.5 to 5.0		2		μA
Sleep Mode	I_{DD} (2)		Ta = −20°C to +70°C	2.5 to 5.0		1.3		
INPUT / OUTPUT								
High Level Input Voltage	V_{IH}	ALARMB, SDA, SCL		2.5 to 5.0	1.4		5.5	V
Low Level Input Voltage	V_{IL}	ALARMB, SDA, SCL		2.5 to 5.0			0.5	
High Level Input Current	I_{IH}	ALARMB, SDA, SCL, NF1, NF2	V_{IN} = V_{DD} (including output transistor off leakage current)	2.5 to 5.0			1	μA
Low Level Input Current	I_{IL}	ALARMB, SDA, SCL, NF1, NF2	V_{IN} = V_{SS} (including output transistor off leakage current)	2.5 to 5.0	−1			
Low Level Output Voltage	V_{OL} (1)	ALARMB, SDA, SCL	I_{OL} = 3.0 mA	3.3 to 5.0			0.4	V
	V_{OL} (2)		I_{OL} = 1.3 mA	2.5 to 5.0			0.4	
Hysteresis Voltage	VHYS	ALARMB, SDA, SCL		2.5 to 5.0		0.2		
Pull−up Resistor Resistance	Rpu	TSENSE1, TSENSE2		2.5 to 5.0		10		kΩ
Pull−up Resistor Temperature Coefficient	Rpuc	TSENSE1, TSENSE2	Ta = −20°C to +70°C	2.5 to 5.0	−0.05		+ 0.05	%/°C
POWER ON RESET								
Reset Release Voltage	V_{RR}	VDD					2.4	V
Initialization Time after Reset Release	T_{INIT}			2.4 to 5.0			90	ms

Table 5. I²C SLAVE CHARACTERISTICS (T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} (V)	Specification		Unit
					Min	Max	
Clock Frequency	T_{SCL}						

Table 6. FUNCTION OF REGISTERS

Command Code	Register Name	R/W	Range	Unit	Description	Initial Value
0x00, 0x01	No Function	–	–	Registers that the access is prohibited		–
0x03	TimeToEmpty	R	0x0000 to 0xFFFF	minutes	Displays estimated time to empty.	0xFFFF
0x04	Before RSOC	W	0xAA55: 1st sampling 0xAA56: 2nd sampling 0xAA57: 3rd sampling 0xAA58: 4th sampling			

Table 6. FUNCTION OF REGISTERS (continued)

Command Code	Register Name	R/W	Range	Unit	Description	Initial Value
0x1C	Termination Current Rate	R/W	0x0002 to 0x001E: Threshold (0.02C to 0.3C)	0.01C	Sets termination current rate.	0x0002
0x1D	Empty Cell Voltage	R/W	0x0000: Disable 0x09C4 to 0x1388: Threshold (2.5 V to 5 V)	mV	Sets empty cell voltage.	0x0000
0x1E	ITE Offset	R/W	0x0000 to 0x03E8 (0.0% to 100.0%)	0.1%	Sets ITE so that RSOC is 0%.	0x0000
0x1F	Alarm High Cell Voltage	R/W	0x0000: Disable 0x09C4 to 0x1388: Threshold (2.5 V to 5 V)	mV	Sets Voltage threshold to generate High Cell Voltage Alarm signal.	0x0000
0x20	Alarm Low Temperature	R/W	0x0000: Disable 0x0980 to 0x0DCC: Threshold (−30°C to 80°C)	0.1K (0.0°C = 0x0AAC)	Sets Voltage threshold to generate Low Temperature alarm signal.	0x0000
0x21	Alarm High Temperature	R/W	0x0000: Disable 0x0980 to 0x0DCC: Threshold (−30°C to 80°C)	0.1K (0.0°C = 0x0AAC)	Sets Voltage threshold to generate High Temperature alarm signal.	0x0000
0x25, 0x24	Total Run Time	R/W	0x00000000 to 0x00FFFFFF 0x24: Lower 16bits 0x25: Higher 8bits	minutes	Displays operating time.	0x0000
0x27, 0x26	Accumulated Temperature	R/W	0x00000000 to 0xFFFFFFFF 0x26: Lower 16bits 0x27: Higher 16bits	2K minutes	Displays accumulated temperature.	0x0000
0x29, 0x28	Accumulated RSOC	R/W	0x00000000 to 0xFFFFFFFF 0x28: Lower 16bits 0x29: Higher 16bits	% minutes	Displays accumulated RSOC.	0x0000
0x2A	Maximum Cell Voltage	R/W	0x09C4 to 0x1388 (2.5V to 5V)	mV	Displays the maximum historical Cell Voltage.	0x0000
0x2B	Minimum Cell Voltage	R/W	0x09C4 to 0x1388 (2.5V to 5V)	mV	Displays the minimum historical Cell Voltage.	0x1388 (5V)
0x2C	Maximum Cell Temperature (TSENSE1)	R/W	0x0980 to 0x0DCC (−30°C t 80°C)	0.1K (0.0°C = 0x0AAC)	Displays the historical maximum temperature of TSENSE1.	0x0980 (−30°C)
0x2D	Minimum Cell Temperature (TSENSE1)	R/W	0x0980 to 0x0DCC (−30°C t 80°C)	0.1K (0.0°C = 0x0AAC)	Displays the historical minimum temperature of TSENSE1.	0x0DCC (80°C)
0x30	Ambient Temperature (TSENSE2)	R	0x0980 to 0x0DCC (−30°C t 80°C)	0.1K (0.0°C = 0x0AAC)	Displays Ambient Temperature.	0x0BA6 (25°C)
0x32	State of Health	R	0x0000 to 0x0064	%	Displays State of Health of a battery on a 0−100 scale	0x0064 (100%)
0x37, 0x36	User ID	R	0x00000000 to 0xFFFFFFFF 0x36: Lower 16bits 0x37: Higher 16bits	Displays 32bits User ID.		(Note 3)
More than 0x40	No Function	−	−	Registers that the access is prohibited.		−

0xXXXX = Hexadecimal notation

3. The initial value of User ID is set on IC at ID Writing process. Please refer to an application note about how to write.

TimeToEmpty (0x03)

This register contains estimated time to empty in minutes. The empty is defined as the state that RSOC(0x0D) is 0%.

Before RSOC (0x04)

This command is the optional Command, used especially for obtaining the voltage with intentional timing after power on reset. Generally the LSI will get initial RSOC by Open Circuit Voltage (OCV) of a battery. It is desirable for battery current to be less than 0.025C to get expected OCV. (i.e. less than 75 mA for 3000 mAh design capacity battery.) The LSI initializes RSOC by measured battery voltage in initial sequence. But if reported RSOC after reset release is not expected value, “Before RSOC” command or “Initial RSOC” command can initialize RSOC again.

The LSI samples battery voltage four times during initial sequence. The sampling interval is around 10 ms. See Figure 9. RSOC is initialized using the 1st sampled voltage automatically with the initial sequence. The four sampled voltage are maintained until the LSI is reset. “Before RSOC” command can select a voltage for RSOC initialization from them. See Table 7. If the battery is not charged during initial sequence the maximum voltage is suitable for more accurate initial RSOC. Try all “Before RSOC” command and read RSOC (0x0D) to search the maximum voltage. The higher RSOC after the command is caused by the higher voltage.

Figure 9. Sampling order for Before RSOC Command

Table 7. BEFORE RSOC COMMAND

Command Code	DATA	Sampling order of Battery Voltage for RSOC Initialization
0x04	0xAA55	1st sampling
	0xAA56	2nd sampling
	0xAA57	3rd sampling
	0xAA58	4th sampling

TimeToFull (0x05)

This register contains estimated time to full in minutes. The full is defined as the state that RSOC (0x0D) is 100%.

TSENSE1 Thermistor B (0x06)

Sets B-constant of the thermistor which is connected to TSENSE1. Refer to the specification sheet of the thermistor for the set value to use.

Initial RSOC (0x07)

The LSI can be forced to initialize RSOC by sending the Before RSOC Command (0×04 = AA55) or the Initial RSOC Command (0×07 = AA55).

The LSI initializes RSOC by the measured voltage at that time when the Initial RSOC command is written. (See Figure 10). The maximum time to initialize RSOC after the command is written is 1.5 ms.

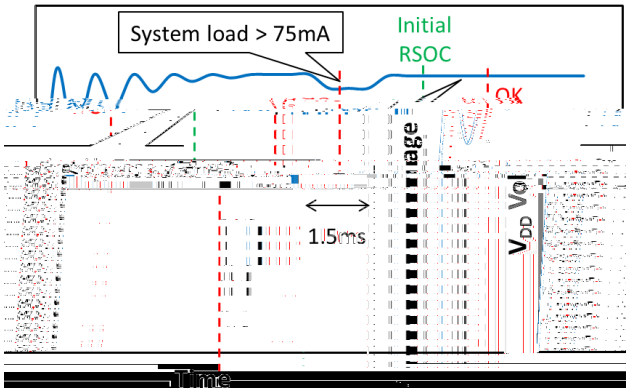


Figure 10. Initial RSOC Command

Cell Temperature (TSENSE1) (0x08)

This register contains the cell temperature from –30°C (0×0980) to +80°C (0×0DCC) measured in 0.1°C units. When Bit 0 of Status Bit (0x16) is 1 the LSI measures the attached thermistor and loads the temperature into the Cell Temperature register. For this mode, the thermistor shall be connected to the LSI as shown in Figure 1. TSENSE1 pin provides power to the thermistor and senses it. Temperature measurement timing is controlled by the LSI, and the power to the thermistor is supplied only at the time.

The Cell Temperature is used for battery measurement that includes RSOC. Then when Bit 0 of Status Bit (0x16) is 0 the application processor must input temperature of the battery to this register. Update of Cell temperature is recommended if the temperature changes more than 1°C during battery charging and discharging.

Cell Voltage (0x09)

This register contains the V_{DD} voltage in mV.

Current Direction (0x0A)

This register is used to control the reporting of RSOC. In Auto mode the RSOC is reported as it increases or decreases. In Charge mode the RSOC is not permitted to decrease. In Discharge mode the RSOC is not permitted to increase.

With consideration of capacity influence by temperature, we recommend operating in Auto because RSOC is affected

by the cell temperature. A warm cell has more capacity than a cold cell. Be sure not to charge in the Discharge mode and discharge in the Charge mode; it will create an error.

An example of RSOC reporting is shown in Figure 11 and Figure 12.

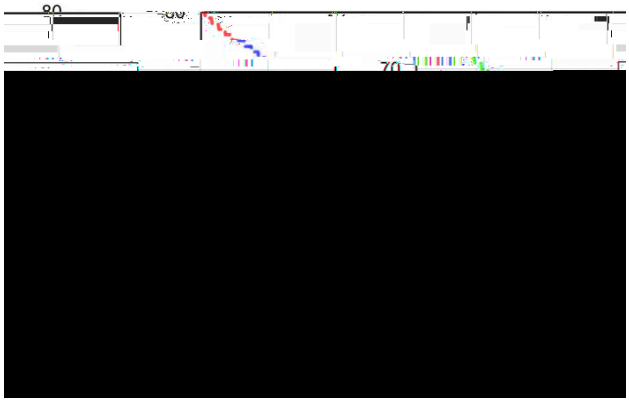


Figure 11. Discharge Mode (An example with increasing in temperature. A warm cell has more capacity than a cold cell. Therefore RSOC increases without charging in Auto mode)

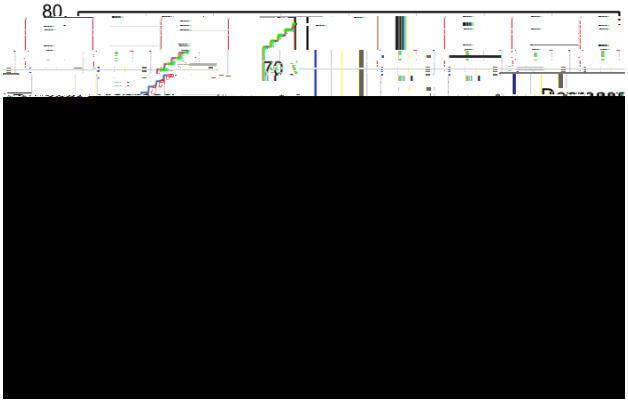


Figure 12. Charge Mode (An example with decreasing in temperature. A cold cell has less capacity than a warm cell. Therefore RSOC decreases without discharging in Auto mode)

Adjustment Pack Application (0x0B)

This register contains APA values which are parameter to fit installed battery profiles in a target battery characteristics. Appropriate APA values for the target battery will improve

on for the charging. This register contains the delay time from the turn−on to the temperature measurement. The delay time is calculated by following formula.

$$\text{Delay} = 0.167\ \mu\text{s} \times (200 + \text{APT}) \quad \text{(eq. 2)}$$

The both of TSENSE1 and TSENSE2 resistors turn on at the same time. See Figure 13 about the delay and waveform. The default APT (0x001E) will meet most of circuits where a capacitor as shown in Figure 14 is not placed. This will delay the measurement with this register if there is a capacitor in target battery pack.

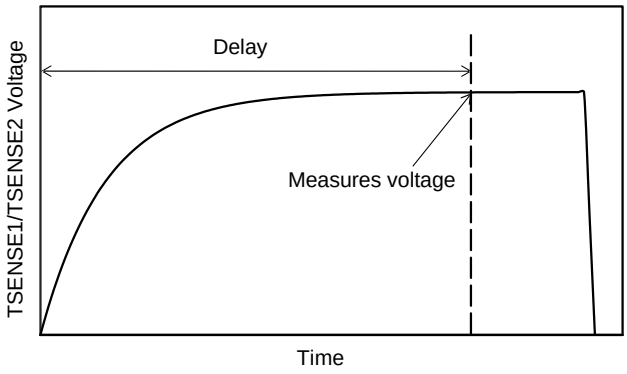


Figure 13. Example of TSENSE1 and TSENSE2 Voltage at Temperature Measurement

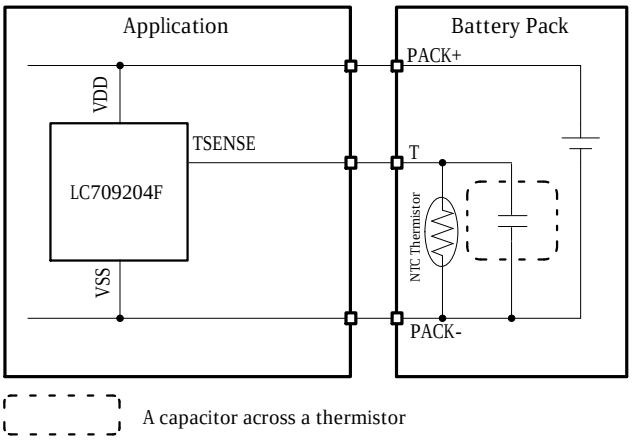


Figure 14. An Example of a Capacitor Across the Thermistor

RSOC (0x0D)

This register contains rescaled RSOC in 1%. It is same as ITE (0x0F) when Termination current rate (0x1C) and Empty Cell Voltage (0x1D) are default values.

When this register is written in Operational mode the data may be updated by following two behaviors of the LSI. One is the automatic convergence to close RSOC to actual value of a battery. The other is rescaling. Set Sleep mode to keep the data. Writing to this register is not necessary in normal operation. ITE (0x0F) will be updated with the writing too.

TSENSE2 Thermistor B (0x0E)

Sets B−constant of the thermistor which is connected to

Table 10. BATTERY PROFILE VS. REGISTER

IC Type	Battery Type	Nominal / Rated Voltage	Charging Voltage	Number of the Parameter (0x1A)	Change of the Parameter (0x12)
LC709204FXE−01TBG	01	3.7 V	4.2 V	0x1001	0x00
	04	UR18650ZY (Panasonic)			0x01
	05	ICR18650−26H (SAMSUNG)			0x02
	06	3.8 V	4.35 V		0x03
	07	3.85V	4.4V		0x04

Alarm Low Cell Voltage (0x14)

The ALARMB pin will output low level and the bit 11 of BatteryStatus register (0x19) will be set to 1 if Cell Voltage (0x09) falls below this value. ALARMB pin will be released from low if VDD rises than this value. But the bit 11 keeps 1 until it is written or Power−on reset. Set this register to 0 to disable. Figure 16.

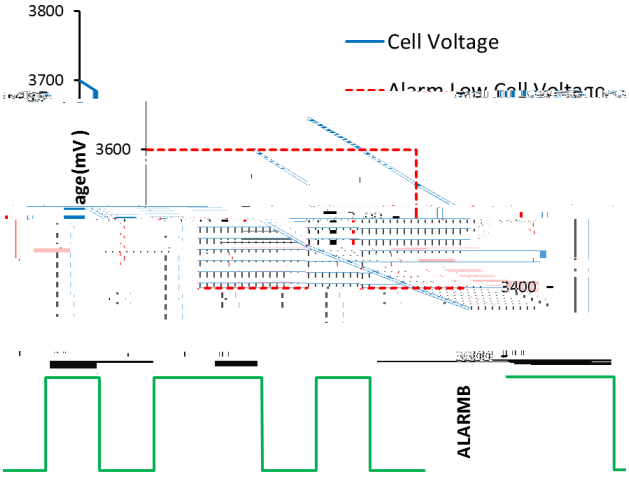


Figure 16. Alarm Low Cell Voltage

IC Power Mode (0x15)

The LSI has two power modes. Operational mode (0x15 = 01) or Sleep mode (0x15 = 02). In the Operational mode all functions operate with full calculation and tracking of RSOC during charge and discharge. In the Sleep mode only I^2C communication functions is enable and ALARMB pin is released from low. When it is switched from Sleep mode to Operational mode RSOC calculation is continued by using the data which was measured in the previous Operational mode.

Status Bit (0x16)

This register controls temperature measurement with external thermistors. Bit 0 of this register controls TSENSE1 thermistor and bit 1 controls TSENSE2. When the bits are set to 1 the LSI measures temperature with the 7.26.891350.6016 Tm0 Tw870 0 0 106Tw843Alarm Low Cell

BatteryStatus (0x19)

This register contains different alarm and estimated states of the battery. See Table 11. Each alarm bit is set to 1 when each alarm condition is satisfied. The bits which are set to 1 once will keep 1 even if the alarm conditions are resolved. Set the alarm bits to 0 after having confirmed the cause of the alarm.

Status bit 6 that is Discharging reports estimated state of the battery. It means that a battery is discharged for 1 and charged for 0.

Status bit 7 that is INITIALIZED helps that an application processor detects the power−on reset of LSI on battery insertion. The bit is set to 1 after power−on reset. Then the processor can detect the power−on reset if it has set the bit to 0 after previous power−on reset.

Table 11. BATTERY STATUS

	BIT	Function	ALARMB control	Initial value
ALARM	15	High Cell Voltage		

ITE Offset (0x1E)

This register is referred to transform ITE (0x0F) to RSOC (0x0D). RSOC will be rescaled so that it is 0% when ITE (0x0F) is equal to this register. See Figure 19. Refer to Termination current rate section about the Full charge offset in the figure.

There are two methods to update this register. One is to write it directly. The other is an automatic update by Empty Cell Voltage (0x1D). Refer to Empty Cell Voltage section about it.

Alarm High Cell Voltage (0x1F)

The ALARMB pin will output low level and the bit 15 of BatteryStatus register (0x19) register will be set to 1 when Cell Voltage (0x09) rises than this value. ALARMB pin will be released from low when Cell Voltage falls below this value. But the bit 15 keeps 1 until it is written or Power−on reset. Set this register to 0 to disable.

Alarm Low Temperature (0x20)

The ALARMB pin will output low level and the bit 8 of BatteryStatus register (0x19) will be set to 1 when Cell Temperature (0x08) falls below this value. ALARMB pin will be released from low when Cell Temperature rises than this value. But the bit 8 keeps 1 until it is written or Power−on reset. Set this register or Bit 0 of Status Bit (0x16)to 0 to disable.

Alarm High Temperature (0x21)

The ALARMB pin will output low level and the bit 12 of BatteryStatus register (0x19) will be set to 1 when Cell Temperature (0x18) rises than this value. ALARMB pin will be released from low when Cell Temperature falls below this value. But the bit 12 keeps 1 until it is written or Power−on reset. Set this register or Bit 0 of Status Bit (0x16) to 0 to disable.

TotalRuntime (0x24, 0x25)

This register contains an elapsed time of Operational mode after battery insertion in minutes. The LSI stops the counting when it reaches 0xFFFFFF. When this register is written it starts counting from the written value. It doesn't count in Sleep mode.

Accumulated Temperature (0x26, 0x27)

In Operational mode this register accumulates Cell Temperature (0x08) value per minute. It stops the accumulating when it reaches 0xFFFFFFFF. When this register is written it starts accumulating from the written value. It doesn't count in Sleep mode.

Accumulated RSOC (0x28, 0x29)

In Operational mode this register accumulates RSOC (0x0D) value per minute. It stops the accumulating when it reaches 0xFFFFFFFF. When this register is written it starts accumulating from the written value. It doesn't count in Sleep mode.

Maximum Cell Voltage (0x2A)

The maximum Cell Voltage (0x09) is stored. This register will be updated whenever the higher voltage is detected. If the lower voltage is written it can detect the higher voltage than the written voltage again.

Minimum Cell Voltage (0x2B)

The minimum Cell Voltage (0x09) is stored. This register will be updated whenever the lower voltage is detected. If the higher voltage is written it can detect the lower voltage than the written voltage again.

Maximum Cell Temperature (TSENSE1) (0x2C)

The maximum Cell Temperature (0x08) is stored. This register will be updated whenever the higher temperature is detected. If the lower temperature is written it can detect the higher temperature than the written temperature again.

Minimum Cell Temperature (TSENSE1) (0x2D)

The minimum Cell Temperature (0x08) is stored. This register will be updated whenever the lower temperature is detected. If the higher temperature is written it can detect the lower temperature than the written temperature again.

Ambient Temperature (TSENSE2) (0x30)

This register contains the ambient temperature from −30°C (0×0980) to +80°C (0×0DCC) measured in 0.1°C units. When Bit 1 of Status Bit (0x16) is 1 the LSI measures the attached thermistor and loads the temperature into the Ambient Temperature register. The operation is the same as TSENSE1.

Ambient Temperature is not used for battery gauging. Therefore a temperature measurement of any place is possible.

State of Health (0x32)

This register contains State of Health of a battery in 1% unit. After the battery insertion, this register is started at 100%. It decreases by deterioration of the battery.

User ID (0x36, 0x37)

This register contains 32bits data written in built−in NVM. It is usable for various purposes. Refer to an application note about how to write the NVM.

HG−CVR2

Hybrid Gauging by Current-Voltage Tracking with Internal Resistance

– is 's unique method which is used to calculate accurate RSOC. – first measures battery voltage and temperature. Precise reference voltage is essential for accurate voltage measurement. LC709204F has accurate internal reference voltage circuit with little temperature dependency.

It also uses the measured battery voltage and internal impedance and Open Circuit Voltage (OCV) of a battery for

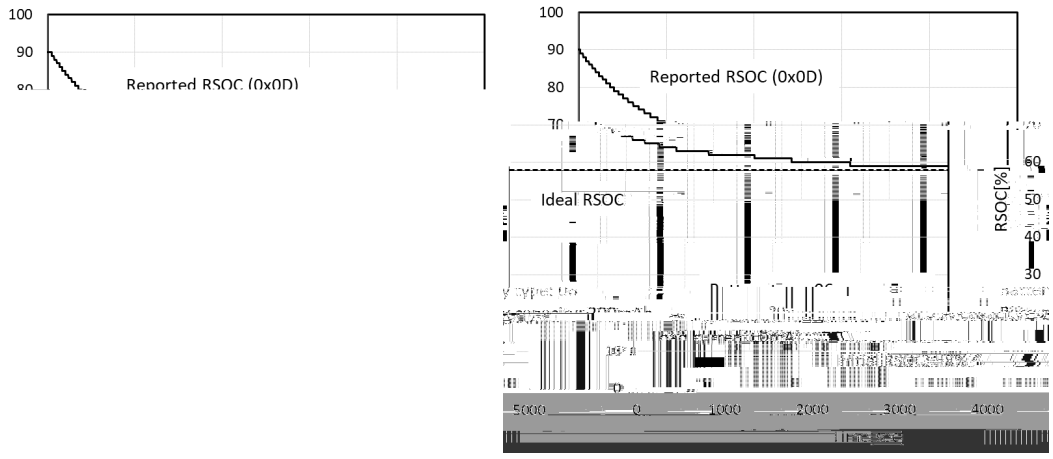
the current measurement. OCV is battery voltage without load current. The measured battery voltage is separated into OCV and varied voltage by load current. The varied voltage is the product of load current and internal impedance. Then the current is determined by the following formulas.

$$V(VARIED) = V(MEASURED) - OCV \qquad \text{(eq. 6.)}$$

$$I = \frac{V(VARIED)}{R(INTERNAL)} \qquad \text{(eq. 7.)}$$

Where *V(VARIED) i*s varied voltage by load current, *V(MEASURED)* is measured voltage, *R(INTERNAL)* is internal impedance of a battery. Detailed information about the internal impedance and OCV is installed in the LSI. The internal impedance is affected by remaining capacity,

TYPICAL CHARACTERISTICS



NOTE: This Graph is the example for starting point 90% (includes 30−32% error).

Figure 20. Convergent Characteristic from the Initialize Error

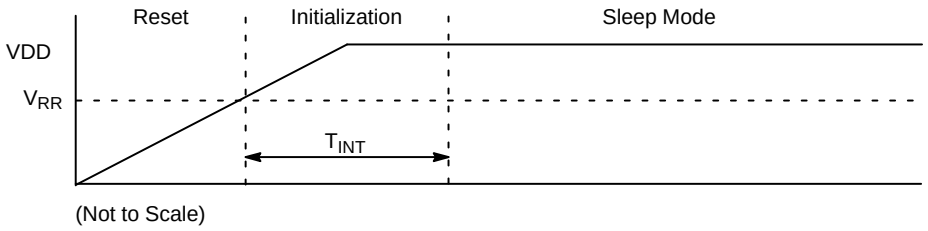


Figure 21. Power On Timing Diagram

Power-on Reset/Battery Insertion Detection

When this LSI detects battery insertion, it is reset automatically. Once the battery voltage exceeds over the V_{RR}, it will release RESET status and will complete LSI initialization within T_{INIT} to enter into Sleep mode. All registers are initialized after Power-on reset. Then I^2C communication can be started. Figure 21.

Measurement Starting Flow

After the initialization users can start battery measurement by writing appropriate value into the registers by following the flow shown in Figure 22−23. Figure 22 shows Thermistor mode that the LSI measures battery temperature with thermistors. Figure 23 shows I^2C mode that the LSI receives battery temperature from an application processor. In the figure Mandatory settings to measure RSOC are enclosed in sold line. Optional settings to use each required function are enclosed in dotted line.

Set some mandatory or optional parameters at the beginning. RSOC (0x0D) is updated to the value corresponding to a selected battery profile after Change of the Parameter command (0x12). Then set the LSI to Operational mode. At the end of starting flow set INITIALIZED bit to 0. An application processor can detect whether the LSI was reinitialized by reading the bit. (For example, for turn−off by Lib−protection IC) Repeat this starting flow again if this b66.166dDange to t1

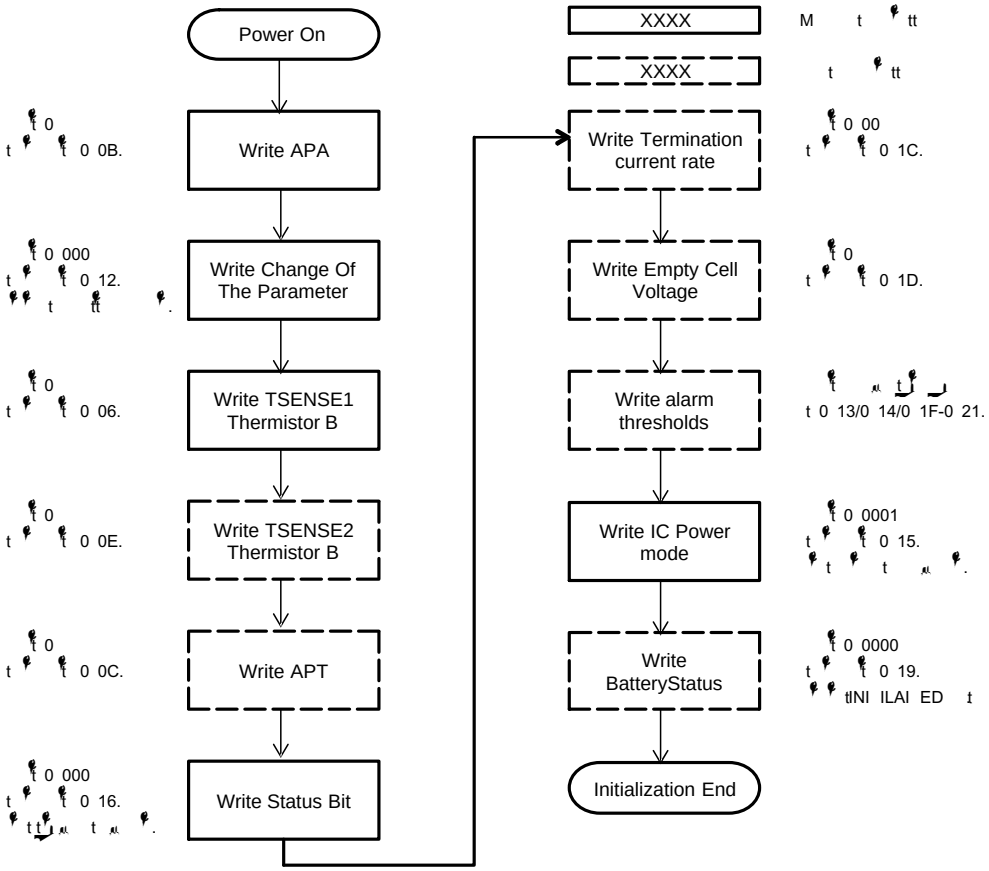


Figure 22. Starting Flow at Thermistor Mode

Layout Guide

Figure 24 shows the recommended layout pattern around LC709204F. Place CVDD and CREG capacitor near the LSI. Short−pin with TSENSE2 and NF1 to pull out TSENSE2 is permitted.

The resistance of the Power paths between Battery or Battery Pack and the LSI affects the gauging. Place the LSI to minimize the resistance. But the resistance of the paths which is connected to only this LSI doesn't affect it.

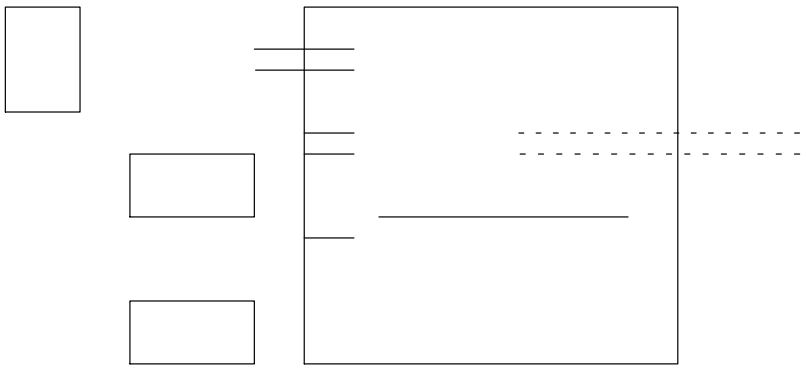


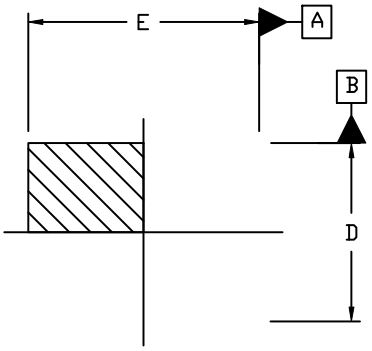
Figure 24. Layout Pattern Example Around LC709204F (Top View)

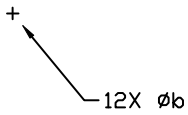
Table 12. ORDERING INFORMATION

Device	Package	Shipping†
LC709204FXE−01TBG	WLCSP12, 1.48x1.91x0.51 (Pb-Free / Halogen Free)	5,000 / Tape & Reel

WLCSP12, 1.48x1.91x0.51
CASE 567XE
ISSUE A

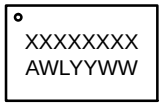
DATE 22 FEB 2019





BOTTOM

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.